ELECTRONIC DEVICES & CIRCUITS

B.Sc., Electronics - Paper - II

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Electronics

PAPER - II

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FOREWORD

Since its establishment in 1976, Acharya Nagarjuna University has been forging ahead in the path of progress and dynamism, offering a variety of courses and research contributions. I am extremely happy that by gaining a B++ (80-85) grade from the NAAC in the year 2003, the University has achieved recognition as one of the front rank universities in the state. At present Acharya Nagarjuna University is offering educational opportunities at the UG, PG levels apart from research degrees to students from over 285 affiliated colleges spread over the three districts of Guntur, Krishna and Prakasam.

The University has also started the Centre for Distance Education with the aim to bring higher education within reach of all. The Centre will be a great help to those who cannot join in colleges, those who cannot afford the exorbitant fees as regular students, and even housewives desirous of pursuing higher studies. With the goal of bringing education to the doorstep of all such people, Acharya Nagarjuna University has started offering B.A., and B.Com courses at the Degree level and M.A., M.Com., M.Sc., M.B.A. and L.L.M. courses at the PG level from the academic year 2003-2004 onwards.

To facilitate easier understanding by students studying through the distance mode, these self-instruction materials have been prepared by eminent and experienced teachers. The lessons have been drafted with great care and expertise in the stipulated time by these teachers. Constructive ideas and scholarly suggestions are welcome from students and teachers involved respectively. Such ideas will be incorporated for the greater efficacy of this distance mode of education. For clarification of doubts and feedback, weekly classes and contact classes will be arranged at the UG and PG levels respectively.

It is my aim that students getting higher education through the Centre for Distance Education should improve their qualification, have better employment opportunities and in turn facilitate the country's progress. It is my fond desire that in the years to come, the Centre for Distance Education will go from strength to strength in the form of new courses and by catering to larger number of people. My congratulations to all the Directors, Academic Co-ordinators, Editors and Lesson - writers of the Centre who have helped in these endeavours.

Prof. Y. R. Haragopal Reddy
Vice-Chancellor,
Acharya Nagarjuna University

B.Sc. II Year- Electronics Theory Syllabus

Paper-II Electronic Devices and Circuits

Unit - I

Semiconductor Physics - Classification of matter on the basis of i) resistivity ii) energy band theory of crystals, Formation of conduction band, Forbidden energy gap Valence band - Conductors, semiconductors and insulators.

Semiconductor crystal - Schematic diagrams - electrons and holes. Properties of holes, doped semiconductors- **p-type and n-type**, Fermi energy level representation, Position of Fermi energy level in **intrinsic and** extrinsic semiconductors. (Qualitative graphical treatment)

Conduction in semiconductors - Drift and diffusion currents, Carrier lifetime, Dependence of mobility on doping and temperature, Derivation of equation of continuity.

Diodes - PN junction, Depletion region and junction capacitance. Action of forward bias and reverse bias. Diode equation (derivation not necessary) and its interpretation. V-I characteristics, Explanation of diode as a non-linear element. Reverse saturation current of a diode as a function of temperature.

Types of diodes - Types of PN junctions, their construction, working and applications i) Junction diode ii) Zener diode iii) Varicap iv) Tunnel diode. v) Metal-semi-conductor diode for high frequency detection.

Unit –II

Bipolar Junction Transistor (BJT) - PNP and NPN transistors, current components in BJT (I_E, I_B, I_C, I_{CO}), α and β of a transistor.

BJT static characteristics - Input and output characteristics, CB, CE & CC configurations (explanation of cut off, active and saturation regions) and experimental arrangement to draw I/P & O/P characteristics in CE configuration.

Biasing - Biasing and load line analysis, Thermal runaway, fixed bias arrangement, collector to base bias arrangement and self-bias arrangement. BJT as an amplifier - load line analysis.

Low frequency model - CE configuration as a two-port network, 'h' parameters and h-parameter equivalent circuit. Transistor amplifier in CE configuration and analysis.

BJT high frequency model - Cut off frequency range f_α, f_β and f_T.

Amplifiers - Introduction- Concept of an amplifier, Classification of amplifiers: Voltage, current, trans conductance and trans resistance.

Classification based on method of analysis - small signal and large signal amplifiers; Classification based on frequency ranges; Classification based on conduction angle and coupling; Amplifier parameters – voltage gain, current gain, input resistance, out put resistance, efficiency and frequency response.

CE amplifier - equivalent circuit of RC - coupled CE amplifier and it frequency response.

Unit-III

Feed back amplifiers - Concept of feedback; different types of feedback; Gain of an amplifier with feedback. Effect of negative feedback feedback on i) gain ii) noise iii) bandwidth iv) input impedance v) output impedance.

Emitter follower and its equivalent circuit; expression for different parameters, concept of Darlington pair.

Oscillators -Sinusoidal oscillators, Barkhausen criterion; RC Oscillators - Phase shift and Wien bridge oscillators; LC Oscillators - Hartley and Colpitt's oscillators; Crystal oscillator and frequency stability.

Relaxation oscillators - Astable, Monostable and Bistable Multivibrators - Schmitt trigger circuit.

Unit – IV

Field Effect Transistor (FET) - Schematic representation of FET; N - and P - channel FETs, output and transfer characteristics; Biasing of JFET and MOSFET (enhancement and depletion modes); Small signal FET model; Application of FET and MOSFET and their advantages over transistors.

Uni Junction Transistor (UJT) - Structure and schematic representation of UJT; Characteristics and experimental determination of its parameters; Application of UJT as a relaxation oscillator.

Silicon Controlled Rectifier (SCR) - Construction of SCR. Two-transistor representation, characteristics of SCR. Experimental set up to study SCR characteristics; Application of SCR for power control.

Photoelectric Devices - Photoelectric effect; photoconductive cells - characteristics and spectral response; photo voltaic cells - construction and operation; Photo diodes, Photo transistors; LED, Solar cells and their characteristics.

BOOKS RECOMMENDED

1. Electronics II Electronic Devices and Circuits –
   SV Subrahmanyam and K.Malakondaiah
   HiTech Publishers
2. Integrated Electronics- Millman and Halkias, Tata McGraw Hill
3. Electronic principles - V.K.Mehata

REFERENCE BOOKS

1. Electronics devices and circuits-Allen Mottershed
2. Pulse, digital and switching wave forms - Millman and Taub
3. Basic Electronics and linear circuits - Bharghava U
4. Electronics devices EC circuits - Y.N.Bapat
5. Electronics devices EC circuits-Mittal
6. Electronic devices circuits - Millman and Halkias
7. Experiments in electronics- S.V.Subramanyam.

B.Sc. II YEAR Electronics

Practicals- Paper II

1. Volt-Ampere characteristics of a junction diode - To find the *cutin* voltage.
2. Zener diode characteristics- To study the action of Zener diode as a voltage regulator.
3. Clipping and clamping circuits- Observation of output waveform for sinusoidal input.
4. BJT input and output characteristics – Determination of h-parameters.
5. FET-Transfer and Drain characteristics.
6. (a) UJT Volt-Ampere characteristics- Determination of its parameters.
6. (b) As an oscillator for generating two frequencies.
7. a) Single stage RC-couple amplifier-frequency response. b) Effect of negative feedback in the above circuit and comparison of two circuits with respect to gain and bandwidth.
8. LDR characteristics.
9. Phase shift oscillator- Design and construction-determination of frequency.
10. Design and Construction of Colpitts/Hartley oscillator.
11. Astable Multivibrator- Design and determination of frequency.
12. Determination of energy gap of a junction diode using reverse saturation current.
13. Voltage doubler using diodes.
14. Simulation experiments.

(ANY TEN EXPERIMENTS)

B.Sc. DEGREE EXAMINATION

(Examination at the end of Second Year)

Electronics Model Question Paper

Paper II – **ELECTRONIC DEVICES AND CIRCUITS**

Part – II - Electronics

Time: Three hours Maximum marks: 100

PART - A – (4 x 14 = 56 marks)

Answer **ALL** questions.

1. (a) Classify the matter on the basis of

   (i) Rsistivity

   (ii) Energy band theory of crystals as conductors, semiconductors and insulators.

   Or

   (b) (i) Explain the construction and working of a Tunnel diode and

   (ii) Sketch the V-I characteristics and explain the negative resistance portion.

2. (a) Describe BJT and explain the working of NPN and PNP transistors.

   Or

   (b) Explain in detail classification of amplifiers. Derive the voltage gain, current gain, input and output resistances in amplifiers.

3. (a) Draw the circuit of Darlington pair and explain its operation, and write its merits and disadvantages.

   Or

   (b) Sketch the circuit diagram of a Colpitt's oscillator. Derive the condition for sustained oscillations and formula for frequency of oscillations.

4. (a) Explain construction, operation and V-I characteristics of UJT.

Or

(b) Explain construction, two-transistor representation and V-I characteristics of SCR.

PART B – (4 x 5 = 20 marks)

Answer any **FOUR** questions.

5. Explain how an N-type semiconductor is formed and also why a pentavalent impurity is known as Donor type impurity?
6. What is diode equation? Explain its forward bias and reverse bias conditions.
7. What are advantages, disadvantages and also applications of photo conductive cells?
8. Explain DC load line.
9. Explain the function of Astable multivibrator.
10. What are the advantages of FET over BJT?
11. Explain cut-off region, saturation region and active region in CB configuration.

PART C – (4 x 6 = 24 marks)

Answer any **FOUR** questions.

12. A Silicon diode has a saturation current of 0.1 pA at 20^0C. Find its current when it is forward biased by 0.55V. Find the current in the same diode when the temperature rises at 100^0C.

13. A certain transistor has $\alpha_{dc} = 0.98$ and a collector leakage current I_{CO} of 1μA. Calculate the collector and base currents when emitter current I_E =1 mA.

14. In an Astable multivibrator, the value of $R_1 = R_2 = 15$ KΩ and $C_1 = C_2 = 0.005$ μF. Calculate the frequency of oscillation.

15. Following readings were obtained experimentally for a FET. Determine the parameters of FET.

V_{GS}	0V	0V	0.3V
V_{DS}	5V	10V	10V
I_D	8 mA	8.2 mA	7.6 mA

16. State Barkhausen criterion. Derive Barkhausen criterion for sustained oscillations.
17. Explain the functions of circuit components of RC-couple amplifier.
18. Explain the principle, working and characteristics of Photo diode.

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CONTENTS

Practical Lab Manual

UNIT-1 **LESSON-1**

SEMICONDUCTOR PHYSICS

OBJECTIVES OF THE LESSON

This lesson explains the classification of matter on the basis of resistivity and on the basis of energy band theory of crystals. It also gives an idea about the formation of various bands in conductors, semiconductors and insulators. It also discusses about holes and their properties; Fermi energy level representation in intrinsic and extrinsic semiconductors; drift and diffusion currents, mobility, derivation of equation of continuity.

STRUCTURE OF THE LESSON

1.1 INTRODUCTION

Electronics has several applications in all walks of present day life. The main material used in present day electronic devices is the semiconductor. The field of electronics commenced with the development of vacuum tubes in 1906. However, the tubes are obsolete because of some drawbacks and the real development started with semiconductors. Semiconductor solidstate devices like transistors replaced vacuum tubes. Transistors, diodes became popular. They are smaller and more efficient. The semiconductor diodes are used as switches and the transistors are used as switches, amplifiers, and oscillators. With the development of Small Scale Integration (SSI), Large Scale Integration (LSI) and Very Large Scale Integration (VLSI) techniques and Nano-technology, both analog and digital integrated circuits are in wide use in communications, control, computer, radar and automobile applications. The devices like UJT, SCR, and MOSFET are made with semiconductor materials. So, to understand the operation of these devices, it is necessary to study the semiconductor materials in detail.

IMPORTANT TERMS

ENERGY BAND: The range of energies possessed by electrons. It is a large number of discrete by closely spaced energy levels.

VALENCE BAND: The range of energies possessed by the valence electrons is called Valence Band.

CONDUCTION BAND: The uppermost vacant band (next to the valence band) is called Conduction Band.

ELECTRON VOLT: It is the amount of energy that would be imparted to an electron on being accelerated through a potential difference of 1V.

$$1eV = \text{Charge of electron} \times \text{potential difference}$$

$$= 1.6\times10^{-19}\,C \times 1V = 1.6 \times 10^{-9}\,J$$

FORBIDDEN ENERGY GAP (E_G) or ENERGY BAND GAP

It is the difference in energy between the lower edge of the conduction band E_C and upper edge of the valence band E_V on an energy level diagram. It is shown in Fig.1.1. It is measured in electron volt eV.

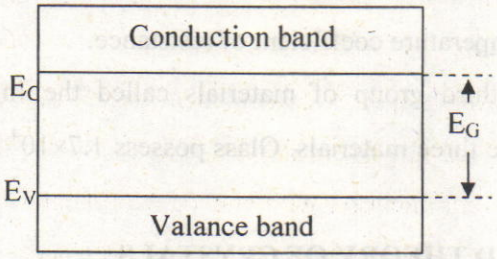

Fig 1.1 Band diagram

SPECIFIC RESISTANCE OR RESISTIVITY

The resistance offered by a conductor to the flow of direct current (DC) is Resistance. The resistance of a conductor depends on: (i) length of the conductor (ii) cross section area A of the conductor; and (iii) material of the conductor 'ρ'.

$$\therefore R = \frac{\rho\, l}{A}$$

Here, ρ is a constant of the material at any particular temperature. It is known as Specific Resistance or Resistivity. Hence, if l = 1; A = 1; then R = specific resistance.

Specific resistance is defined as the resistance offered by the opposite faces of a centimeter cube of the specimen of the material.

$$\therefore \rho = \frac{RA}{l} \text{ ohm.cm}^2 / \text{cm} = \text{ohm.cm}$$

1.2 CLASSIFICATION OF MATTER ON THE BASIS OF RESISTIVITY

Matter can be classified on the basis of resistivity into conductors, semiconductors and insulators. Conductors are the materials, which possess resistivity of the order 10^{-8} Ωm. When we increase the temperature of a metal conductor such as copper, its resistivity increases. Hence conductors possess positive temperature coefficient of resistance. The resistivity of silver is 1.6×10^{-8} Ωm, that of copper is 1.7×10^{-8} Ωm and that of aluminum is 2.6×10^{-8} Ωm.

There is another group of materials such as Germanium and silicon. These are neither good conductors nor good insulators. At room temperature, these materials have resistivities greater than that of conductors and less than that of insulators. Resistivities of pure Ge and Si are 6.5×10^{-1} and 2×10^{3} Ωm. When we raise

the temperature of a semiconductor, its resistivity decreases. Hence semiconductors possess negative temperature coefficient of resistance.

The third group of materials called the Insulators possess highest resistivity among the three materials. Glass possess 1.7×10^{4} Ωm, hard rubber possess 1.0×10^{16} Ωm.

1.3 ENERGY BAND THEORY OF CRYSTALS

X-rays studies reveal that most metals and semiconductors are crystalline in structure. A crystal consists of a space array of atoms or molecules built up in regular repetition in three dimensions of some fundamental structural unit. The electronic energy levels discussed for a single free atom (as in gas) do not apply to the same atom in a crystal.

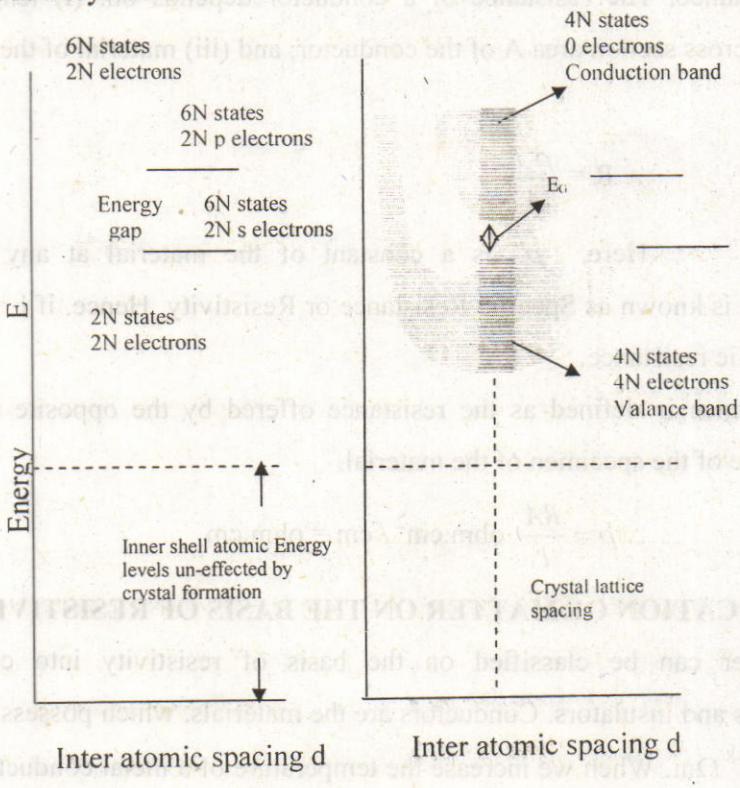

Fig.1.2a **Fig.1.2b**

Fig.1.2 Splitting of energy levels into energy bands when Atoms are brought together to form crystal

When atoms form crystals, it is found that the energy levels of the inner-shell electrons are not affected appreciably by the presence of the neighboring atoms. However, the levels of the outer-shell electrons are changed considerably since these

electrons are shared by more than one atom in the crystal. The new energy levels of the outer electrons can be determined by quantum mechanics. It is found that coupling between outer shell electrons of the atoms results in a band of closely spaced energy states, instead of the widely separated energy levels of the isolated atom. This is shown in Fig1.2.

Consider a crystal consisting of N atoms of one of the IV group elements (say Carbon with atomic number 6, its configuration is $1s^2 2s^2 2p^2$). Imagine that spacing between the atoms can be varied. If the atoms are so far apart and the interaction between tnem is negligible, then their energy levels will coincide with those of the isolated atom. The outer two sub-shells contain two s-electrons and two p-electrons. Ignoring the inner shell levels, there are 2N electrons completely filling the 2N possible s-levels, all at the same energy. The p-atomic sub shell has six possible states. The 2N electrons fill only one third of the 6N possible p-states.

If we now decrease the inter atomic spacing of our imaginary crystal (from right to left in Fig.1.2), an atom will exert an electric force on its neighbors. Because of coupling between atoms, the atomic wave functions overlap and the crystal becomes an electronic system, which must obey Pauli's exclusion principle. Hence 2N s-states must spread out in energy. The separation between levels is small. Since N is approximately 10^{23} cm^{-3}, the total spread between the minimum and maximum energy may be several eV. This large number of discrete but closely spaced energy levels is called an Energy Band as shown in Fig.1.2. The 2N states in this band are completely filled with 2N electros. Similarly, the upper showed region in Fig1.2 is a band of 6N states which has only 2N of its levels occupied by electrons.

There is an energy gap (forbidden band) between the two bands discussed above and that this gap decreases as atomic spacing decreases. For small enough distances (as shown in Fig.1.2b), these bands will overlap. Under these circumstances, the 6N upper states merge with the 2N lower states, giving a total of 8N levels, half of which are occupied by the 2N+2N = 4N electrons. At these spacing, each atom has given up four electrons to the band. These electrons belong to the crystal as a whole. The band these electrons occupy is called the *Valence Band.*

If the spacing between atoms is decreased below the distance at which the bands overlap, the interaction between atoms is large. At the crystal lattice spacing, (the dashed vertical line), the valence band filled with 4N electrons separated

by a forbidden band from an empty band consisting of 4N additional states. The upper vacant band is called the *Conduction Band.*

1.4 CLASSIFICATION OF MATTER ON THE BASIS OF ENERGY BAND THEORY OF CRYSTALS

On the basis of energy band theory, solids can be classified into three types (1) Conductors (2) Semiconductors (3) Insulators.

Conductors: In some substances, the valence band and conduction band overlap and there will be no forbidden gap (E_G = 0eV). Electrons are free to move leading to conduction phenomenon. Such materials are called Conductors. Conductors possess positive temperature coefficient of resistance. Ex. All metals (silver, gold, aluminum, etc.). Under the influence of electric field, the electrons may acquire additional energy and move. These mobile electrons constitute current.

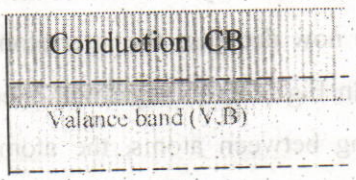

Fig.1.3 Band diagram of metal

Semi Conductors: A substance, which possess relatively small (E_G =1eV) forbidden energy gap is called a Semiconductors.

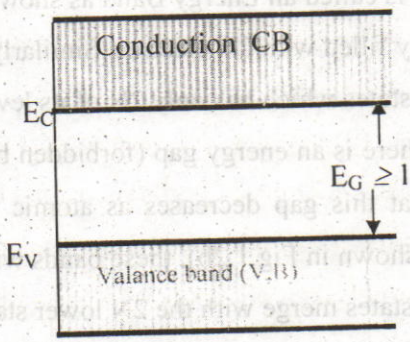

Fig.1.4 Band diagram of semiconductor

In a semiconductor, the valence band and conduction band are separated by a small energy gap. The valence band remains full and the conduction band remains empty at 0K. Semiconductors possess negative temperature coefficient of resistance. As the temperature increases, electrons gain energy, cross the energy gap and enter into

conduction band and leads to conductivity. Ex Si, Ge, GaAs, GaAsP. The energy band diagram is shown in Fig.1.4

Insulators: A substance which possess large forbidden energy gap ($E_G \geq 5$ eV) is called an Insulator. In an insulator, the conduction band and valence band are separated by very large forbidden energy gap. Any energy, which can be supplied to an electron in an insulator, is too small to lift the electron from the filled valence band into the conduction band. Hence conduction is impossible. The energy band diagram is shown in Fig.1.5. Ex: Diamond, ebonite, plastic etc.

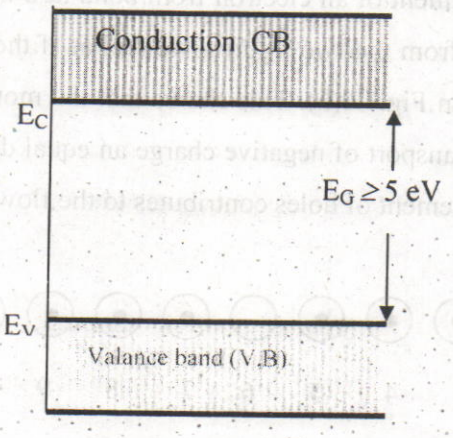

Fig.1.5 Band diagram of insulator

1.5.1 PROPERTIES OF HOLES

(i) Hole behaves like a positive charge equal in magnitude to the electronic charge.

(ii) The movement of a hole constitutes a flow of electric current.

(iii) Just like electrons, holes are deflected by electric and magnetic fields.

(iv) The direction of deflection of hole is opposite to that of electron.

(v) In an intrinsic semiconductor, the number of holes is equal to number of electrons.

(vi) Holes are less mobile. Sometimes they behave like particles with mass larger than electron mass.

(vii) They exhibit Hall effect opposite to that of electrons.

1.5.2 MECHANISM OF HOLE CONTRIBUTION TO THE ELECTICAL CONDUCTION

Consider that there exists an incomplete covalent bond in a semiconductor crystal. It is equivalent to a hole in valence band. Now, it is relatively easy for a valence electron in a neighboring atom to leave its covalent bond to fill this hole. When an electron comes out of a bond to fill a hole, it leaves a hole in its initial position. It (the hole) moves in the direction opposite to that of the electron. This hole, in its new position, may now be filled by an electron from another covalent bond. So, we have a mechanism for the conduction of electricity which does not involve free electron. In the Fig.1.6(a), a circle with a dot in it represents a complete bond and an empty circle designates a hole. Due to the movement of an electron from bond at 6 into the hole at bond 5, the Fig.1.6(b) results from the two figures, we feel as if the hole in Fig1.6(a) has moved towards right in Fig.1.6(b). This shows that the motion of the hole in one direction means the transport of negative charge an equal distance in the opposite direction. Hence, movement of holes contributes to the flow of electric current.

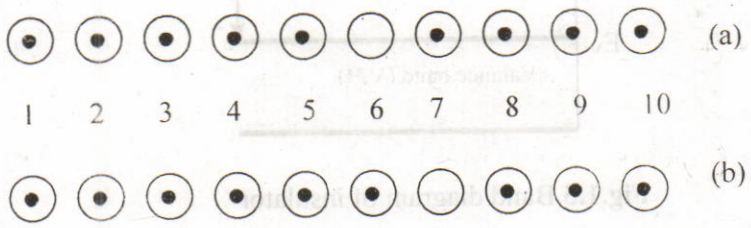

Fig.1.6 Hole shifting

1.6 TYPES OF SEMICONDUCTORS

There are two types of semiconductors.

1) Intrinsic (pure) and

2) Extrinsic (Doped or Impure)

1.6.1 INTRINSIC SEMI CONDUCTORS

A Semiconductor in an extremely pure form is known as *Intrinsic semiconductor.*

Ex: pure Germanium (Ge) and Pure Silicon (Si)

CONFIGURATION

Germanium atomic number: 32

Electronic configuration: $1s^2\ 2s^2 2p^6\ 3s^2\ 3p^6 3d^{10}\ 4s^2 4p^2$

At very low temparature (0K), the Germanium crystal behaves as an insulator since no free carriers of electricity are available. However, at room temparature,

some of the covalent bonds will be broken because of the thermal energy absorbed from the surroundings and conduction is possible. This is shown in Fig.1.7.

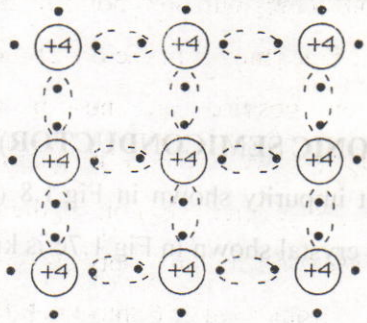

Fig.1.7a

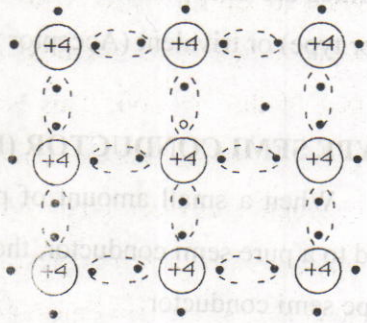

Fig.1.7b

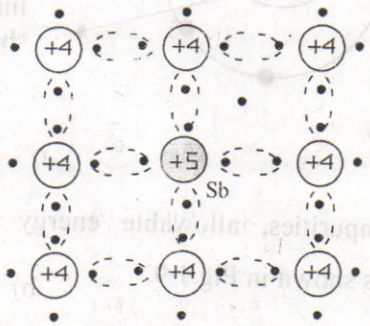

Fig.1.7c

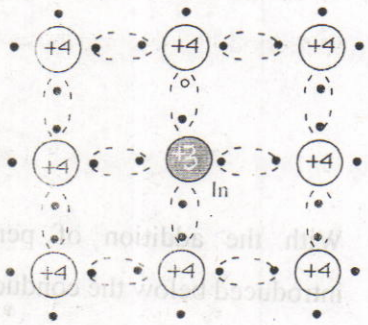

Fig 1.7d

1.6.2 EXTRINSIC SEMICONDUCTORS (or) DOPED SEMICONDUCTORS

Whenever impurities (foreign atoms) are introduced into a pure Si or Ge like crystals, their conductivity increases. These partially doped semiconductors are called *Extrinsic Semiconductors.*

PENTAVALENT			TRIVALENT		
Element	Symbol	Atomic number	Element	Symbol	Atomic number
Antimony	Sb	51	Indium	In	49
Arsenic	As	33	Gallium	Ga	31
Phosphorous	P	15	Boron	B	5

The addition of controlled amounts of impurities to a pure crystal is called *Doping*. The added impurity is called *Dopant* or *Foreign atom*. These impurities are added about one part in 10^8parts. Impurities can be either pentavalent (donor type) or trivalent (Acceptor type).

N-TYPE SEMI CONDUCTOR (ELECTRONIC SEMICONDUCTOR)

When a small amount of pentavalent impurity shown in Fig.1.8 (Ex: As) is added to a pure semi conductor, the resulting crystal shown in Fig.1.7c is known as an N-type semi conductor.

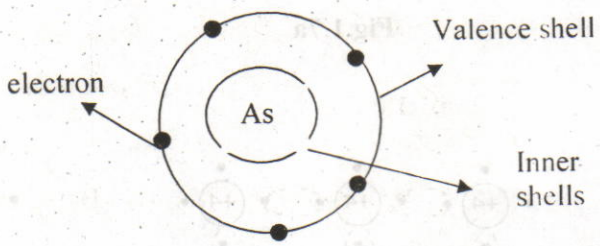

Fig 1.8a

With the addition of pentavalent impurities, allowable energy levels are introduced below the conduction band as shown in Fig.1.9.

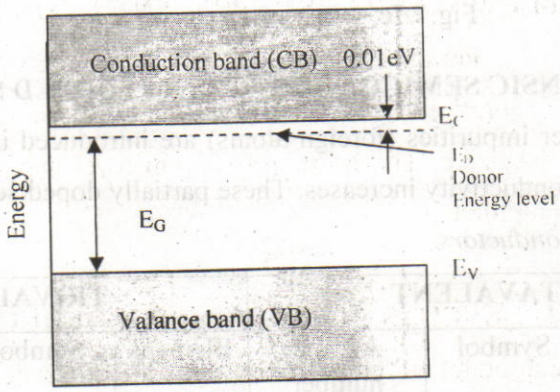

Fig 1.9 Band diagram of n-type semiconductor

In the case of Si, the new discrete allowable energy level is only 0.05 eV below the conduction band and in the case of Ge, it is at 0.01eV. In an N-type semi conductor, majority carriers are electrons. A small number of holes are also

present in the N-type semiconductor, when compared to electrons. So, the holes are called *Minority carriers.*

P-TYPE SEMICONDUCTOR

When a small amount of trivalent impurity, shown in Fig.1.10, is added to a pure semiconductor, we get P-type semiconductor.

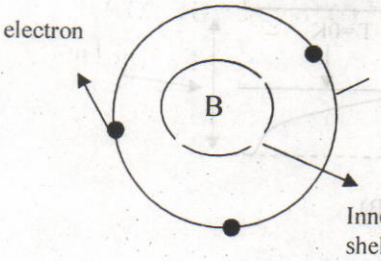

Fig.1.10

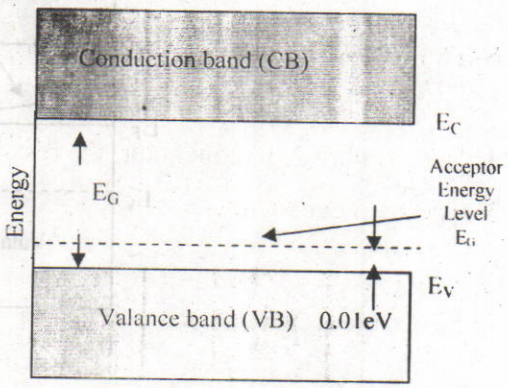

Fig 1.11 Band diagram of P-type semiconductor

With the addition of trivalent impurities, allowable energy levels are introduced above the valency band as shown in Fig.1.11. In case of Silicon, new discrete allowable energy level is only 0.05 eV. In a p-type semiconductor, majority carriers are holes and minarity carriers are electrons.

1.7 FERMI LEVEL AND IT'S REPRESENTATION

Fermi level is a measure of probability of occupancy of allowed energy states. Fermi energy (E_F) is the maximum energy that any electron may posses at absolute zero. The position of Fermi level depends on temperature and impurity concentration.

1.7.1 FERMI LEVEL IN INTRINSIC SEMICONDUCTORS

The product of electron and hole concentrations (n, p), for a given material is constant at a given temparature. If an impurity is added to increase 'n' there will be corresponding decrease in' p' such that product n×p remains constant. For an intrinsic semiconductor n = p = n_i , we can write an important relationship called "Law of Mass Action ".

$$np = n_i^2 = AT^2 e^{\frac{-E_g}{kT}}$$

where n_i is the intrinsic density of either carrier; T Absolute temperature

A is a constant; E_g Energy band gap; K Boltzman constant

The above equation is true for a semiconductor regardless of the donor or acceptor concentrations. Mathematically, we can prove that for an intrinsic semiconductor,

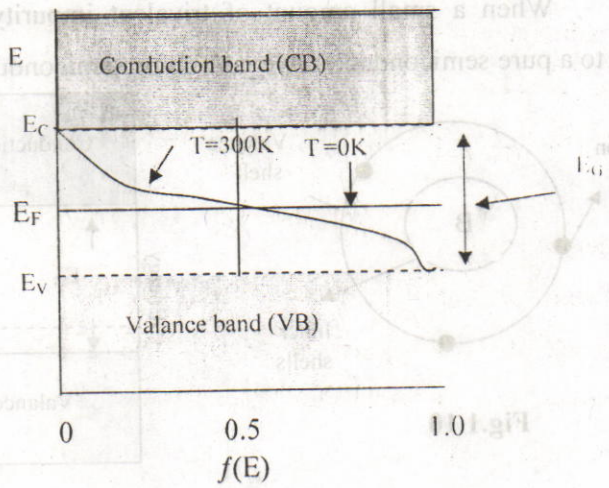

Fig.1.12 Band diagram of intrinsic semiconductor

the Fermi level lies exactly in the center of the forbidden energy gap as shown in Fig.1.12 i.e if the E_f is the Fermi level, E_C is the conduction band energy then we can write

$$E_F = \frac{E_C + E_V}{2}$$

1.7.2 FERMI LEVEL IN EXTRINSIC SEMICONDUCTORS

(1) N-type semiconductor

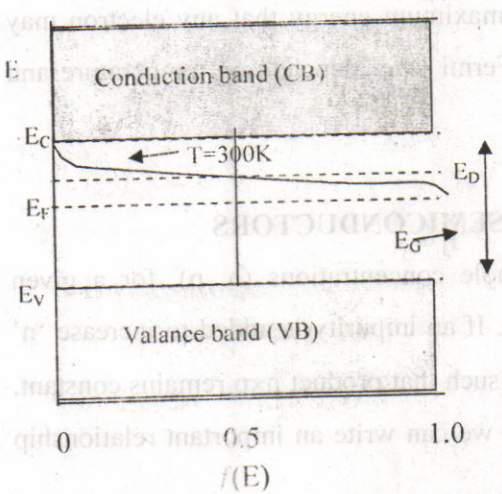

Fig.1.13 Fermi level in N- type semiconductor

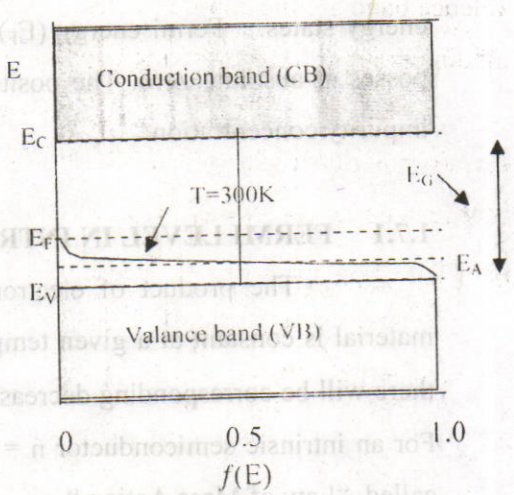

Fig.1.14 Fermi level in P- type semiconductor

When donor impurity atoms are added to the crystal, the donor atoms being ionized, the N electrons from N donor atoms will occupy the first N states near the bottom of the conduction band. Hence it will be more difficult for the electrons from the valence band to cross the energy gap by thermal agitation. Consequently, the number of electron-hole pairs thermally generated for that temperature will be reduced. Since the Fermi level is a measure of the probability of occupancy of the allowed energy states, E_f for N-type semiconductor must move closer to the conduction band as shown in Fig.1.13.

(2) P-Type semiconductor

When acceptor impurity atoms are added to the crystal, they modify the energy level diagram of the semiconductor and making it easy for conduction. The presence of impurities creates new energy levels which lie in the energy band gap near the top of the valence band of energies as in Fig.1.14. The energies for the holes are highest near the valency band.

When an intrinsic semiconductor is doped with acceptor type impurity, the concentration of holes in the valence band is very much larger than the concentration of the electrons in the conduction band and the Fermi level shifts towards the valence band as shown in Fig.1.13.

1.8 CONDUCTION IN SEMICONDUCTORS

1.8.1 Mobility and conductivity

In a semiconductor, electrons in the conduction band and holes in the valence band are the charge carriers. Due to thermal agitation, they move randomly in all directions and hence the net current in any direction is zero.

When an electric field is applied across the semiconductor, every charge carrier experiences a force and drifts in the direction of the force. Thus a charge carrier acquires an average velocity and is called Drift Velocity. It gives rise to drift current.

The average drift velocity per unit electric field is called the *Mobility* (μ) of a charge carrier.

$$\therefore \mu = \frac{v}{E}$$

where v-Drift velocity

E-electric field appear

Drift current density

Consider a cylindrical semiconductor root of length 'l' area of cross section 'A' as shown in Fig.1.15.

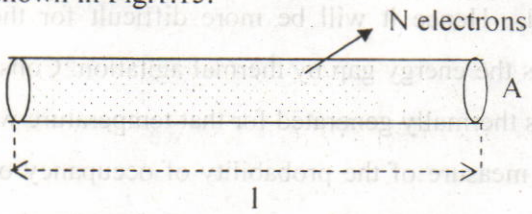

Fig. 1.15

Let an electric field E be applied along the length of the cylinder. As a result of this electric field E, the charge carriers acquire a drift velocity 'v'. Then time taken by the carrier to travel the length 'l' is

$$t = \frac{l}{v} \qquad \text{---------- (1.8.1.1)}$$

Let the carrier concentration i.e no. of carrier per unit volume be n_c

Total no. of carriers inside the cylinder of volume (Al) = n_c Al ------ (1.8.1.2)

$\therefore$ Charge inside the cylinder = n_c.Al.e

where e - charge of the carrier

$\therefore$ Current following through the semiconductor = $I = \frac{n_c . A . l . e}{t}$

$$= \frac{n_c A l . e}{l/v}$$

$$\therefore \quad I = n_c A.e.v$$

$\therefore$ Current density i.e current per unit area of crossection

$$J = \frac{I}{A} = n_c.e.v \qquad \text{---------- (1.8.1.3)}$$

The mobility of the charge carrier μ is given by

$$\mu = \frac{v}{E} \quad \text{or} \quad v = \mu.E$$

Hence Eq.(1.8.1.3) becomes

$$J = n_c .eE \qquad \text{---------- (1.8.1.4)}$$

Conductivity of a semiconductor

If σ is the conductivity (current density per unit applied electric field) then

$$\sigma = \frac{J}{E} \qquad \text{or} \qquad J = \sigma.E \qquad \text{------ (1.8.1.5)}$$

Comparing Eq.(1.8.1.4) & (1.8.1.5), we get

$$\sigma.E = n_c e \mu E$$

or $$\sigma = n_c \mu.E \qquad \text{---------- (1.8.1.6)}$$

In a semi conductor, two types of charge carriers present. Electrons with mobility μ_n and holes with mobility μ_p. The particles move in opposite direction in the presence of electric field E. Hence overall conductivity of the semiconductor containing electrons and holes is

$$\sigma = \sigma_n + \sigma_p$$

$$\sigma = n.e.\mu_n + p.e.\mu_p \qquad \text{---------- (1.8.1.7)}$$

where σ_n , σ_p are the conductivity of semiconductor due to holes and electrons respectively,

'n' is the electron concentration

'P' is the hole concentration.

For a Intrinsic semiconductor

Therefore conductivity of Intrinsic semiconductor

$$\sigma = e.n_i(\mu_n + \mu_p) \qquad \text{---------- (1.8.1.8)}$$

1.8.2 Dependences of Mobility on Doping concentration and Temperature

Mobility μ does not depend upon the doping concentration. It is a property of semiconductor. But μ is influenced by scattering. With increase in temparature, thermal vibrations of the lattice increase which scatter the moving electrons and holes. Hence, the mobility of an electron or hole decreases with increasing temperature.

1.8.3 Diffusion current

Diffusion is a process whereby the charge carriers move in a semiconductor independent of electric field. Diffusion occurs only when there is non-uniform carrier density in the material. (i.e if there exists concentration gradient).The effect of diffusion is to bring the carrier density back to uniformity in the material. So,

Diffusion is the flow of carriers from the regions of high carrier density to the regions of low carrier density.

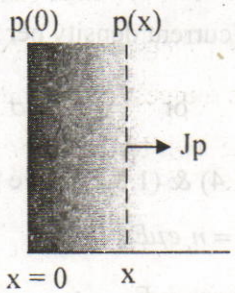

Fig.1.16

EXPLANATION

Consider a semiconductor material with non-uniform concentration of particles as shown in Fig.1.16. The concentration of holes varies with distance 'x' and hence there exist a concentration gradient $\frac{dp}{dx}$ in the density of carriers. This means the density of holes on one side of the imaginary surfaces is larger than the density on the other surface. The holes will continue to move back and forth across the imaginary surface b[illegible] of thermal energy. Hence in a given time interval, more holes will across the surface from the side of greater concentration. This net transport of holes across the surface contribute diffusion current in the positive X-direction .The diffusion of whole current density J is given by

$$J_p = -e.D_p \frac{dp}{dx}$$

where J_p is in A/m^2.

D_p is the diffusion coefficient for holes in m^2 / sec.

$\frac{dp}{dx}$ is concentration gradient.

The negative sign is used as the concentration decreases with increase in distance.

1.8.4 Carrier Life Time (τ)

The average time that an electron spends in the conduction band before recombining via a trap (recombination center) is known as *Life Time* represented by τ_n. Similarly the average lifetime of hole in the valence band is τ_p. Lifetime depends upon

(1) Purity of the material

(2) Temperature

(3) Surface conditions

(4) Shape of the specimen

Carrier life time ranges from nano seconds to hundreds of micro seconds. The life time indicate the time required to return to their equilibrium conditions (n_o, p_o).

Equilibrium values (n_o, p_o)

Both generation and recombination are random processes which are continuously occurring. When the temperature and external conditions are constant, a balance is setup between the generation and recombination. The resultant hole and electron densities are known as *Thermal Equilibrium* values.

Generation of an electron – hole pair involves the passage of an electron from the valance band to the conduction band. Similarly, recombination involves the movement of an electron from the conduction band to the valence band.

1.8.5 EQUATION OF CONTINUITY

Statement: The differential equation which governs the behaviour of charge carriers in a semiconductor under various disturbing conditions is called the *Continuity Equation.*

Explanation

The continuity equation is also known as the Equation of Conservation of Charge as it is based on the fact that charge can neither be created nor destroyed.

The continuity equation is formed by adding three rates of delivery or removal of charge in a given volume of semiconductor and equating this to the rate of change of charge density in the material. The continuity equation is extremely important in the understanding the properties of semiconductor devices.

Let length of the element shown in the Fig.1.17 be dx meters

Volume of the element = dx × area = dx ×1 = dx m^3

Density of holes at any time = p/ m^3

Current density entering the element = J

Current density leaving the element = J + dJ

Therefore number of holes removed from the element in every second = $\frac{dJ}{e}$

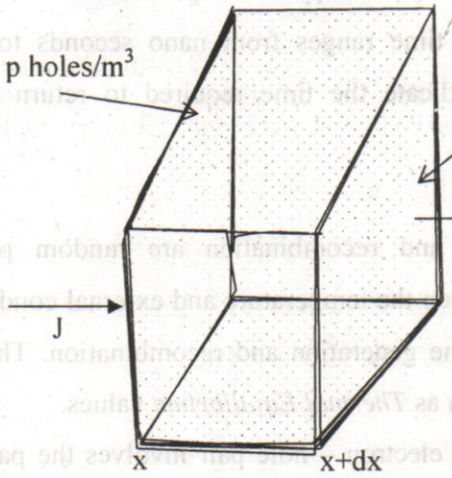

Fig.1.17

Consider

(1) **Generation and recombination**

The rate of change of hole density with time is

$$\frac{dp}{dt} = \frac{p_o - p}{\tau_p} \qquad \text{---------- (1.8.5.1)}$$

where

p_0/τ_p, p/τ_p are the generation rate, recombination rate

τ_p - mean life time of the holes

p_0 - Equilibrium concentration of holes at particular time

p - Concentration of holes at any time.

(2) **Drift of charge in an electric field**

Drift current density due to the flow of charge is given by

$$J_{Dr}^{+} = p.e.v$$

$$\text{or } J_{Dr}^{+} = p.e.v = p.e.\mu_p E \qquad \text{---- (1.8.5.2)}$$

where μ_e - Hole mobility.

E - Electric field.

e - Charge of carrier

(3) **Diffusion of charge**

The diffusion current density given by

$$J_{Di}^{+} = -e.D_p.\frac{dp}{dx} \quad \text{-------- (1.8.5.3)}$$

Here

J_{Di}^{+} = Diffusion current density in A/m^2 due to holes

D_p = Diffusion coefficient for holes m^2/sec

$\therefore$ Total current density due to holes is

$$J^{+} = J_{Dr}^{+} + J_{Di}^{+} = p.e.\mu_p.E - eD_p\frac{dp}{dx}$$

$$J^{+} = e\left[p\mu_p E - D_p\frac{dp}{dx}\right] \quad \text{------ (1.8.5.4)}$$

Net flow of current from the element = dJ

The rate of increase of total number of holes = $\frac{dp}{dt}.dx$

$$\text{But } \frac{dp}{dt}.dx = -\frac{dJ}{e}$$

(Negative sign is because a net current dJ is out of the volume element)

$$\text{or } \frac{dp}{dt} = -\frac{1}{e}\frac{dJ}{dx}$$

$$= -\frac{1}{e}\frac{d}{dx}\left(e\left[p\mu_p E - D_p\frac{dp}{dx}\right]\right)$$

$$= -\mu_p\frac{d}{dx}(pE) + D_p\frac{d^2p}{dx^2} \quad \text{---------- (1.8.5.5)}$$

Taking generation and recombination also into consideration, we can write

$$\frac{dp}{dt} = \frac{p_0 - p}{\tau_p} - \mu_p\frac{d}{dx}(pE) + D_p\frac{d^2p}{dx^2} \quad \text{------- (1.8.5.6)}$$

Similarly for electrons, we can write,

$$\frac{dp}{dt} = \frac{n_0 - n}{\tau_n} + \mu_n\frac{d}{dx}(n.E) + D_n\frac{d^2n}{dx^2} \quad \text{--------- (1.8.5.7)}$$

1.9 SUMMARY

Electronics has grown into a vast subject covering various fields. Present day electronics is based on semiconductor devices. Semiconductor physics is a branch of science which mainly deals with semiconductor devices like diodes, transistors etc. The solids can be classified according to the resistivity or energy band gap, into conductors, semiconductors and insulators .Conductors possess almost zero resistivity

and no forbidden energy gap. Semiconductors possess partial resistivity less than insulators and possess very large forbidden energy gap (>5eV). A pure Ge or Si in their purest form (99.999999% purity) is called an *Intrinsic semiconductor*. But when group III or group V elements are added to them, their conductivity increases. Impurity semiconductors may be either P-type or N-type. As the charge carriers are generated due to the doped impurities, these impurity semiconductors are also called *Extrinsic Semiconductors*. The P- and N-type semiconductors are useful to fabricate semiconductor devices like diode, transistor, U J T, J FET etc.

In a conductor the conduction of current is due to electrons only whereas in a semiconductor, the conduction of current is due to two charge carriers i.e an electron and a hole. In a semiconductor, flow of current may take place due to

(1) Generation and recombination

(2) Drift of charge carriers in the presence of electric field. and

(3) Diffusion of charge as a result of concentration gradient.

The behaviour of charge carriers in a semiconductor under various disturbing conditions is governed by a differential equation known as the *Equation of Continuity*. This equation is based on the law of conservation of charge.

1.10 KEY TERMINOLOGY

Semiconductor, Fermi level, Energy band gap, Electron volt, Conduction band ,Valency band, Donor and Acceptor impurity levels, pentavalent and trivalent impurities, Drift, Diffusion, Mobility, Carrier life time, Equation of continuity, Generation and recombination.

SOLVED NUMERICAL PROBLEMS

Example (1)

Find the density of impurity atoms that must be added to intrinsic Silicon crystal to convert it into

(1) 10^{-1} Ohm meter P-type Silicon

(2) 10^{-1} Ohm meter N-type Silicon.

Given for Silicon $\mu_n = 0.13\ m^2/Vs$, $\mu_p = 0.05\ m^2/Vs$

Solution:

Given $\rho_p = 10^{-1}\ \Omega$ m, $\rho_n = 10^{-1}\ \Omega$ m.

$e = 1.6 \times 10^{-19}$ C

$\mu_n = 0.13\ m^2/Vs$

$\mu_p = 0.05\ m^2/Vs$

To find $N_a = ?$; $N_d = ?$

(1) No. of acceptor electrons in P- type Si is

$$N_a = \frac{\sigma}{e.\mu_p} = \frac{1}{e.\mu_n\rho_p}$$

$$= \frac{1}{1.6\times10^{-19}\times0.05\times10^{-1}}$$

$$= 1.25 \times 10^{21}\ m^{-3}$$

(2) No. of donor atoms in N-type Si is

$$N_d = \frac{\sigma}{e.\mu_n} = \frac{1}{e.\mu_n\rho_n}$$

$$= \frac{1}{1.6\times10^{-19}\times0.13\times10^{-1}}$$

$$= 4.8\times10^{20}\ m^{-3}.$$

Example (2)

Germanium is doped with aluminium so that the concentration of acceptor atoms is 2×10^{21} atoms/m^3. Determine at room temperature (i) Hole concentration (ii) Conductivity (Given $\mu_p = 17\ m^2/V.s$

Solution:

Given $n_p = N_a = 2\times10^{21}$ atoms/m^3 ; $\mu_p = 0.17\ m^2/Vs$

To find: N_a , N_d

Doping of Ge with Al will result in a P- type semiconductor in which hole concentration is roughly equal to the acceptor atoms concentration i.e

$$n_p = N_a = 2\times10^{21}\ \text{atoms/}m^3.$$

Conductivity $\sigma = (n_p\mu_p + n_e\mu_e).e$

Since holes are majority carriers,

$$\sigma = n_p.\mu_p.e = (2\times10^{21})(0.17)(1.6\times10^{-19})$$

$$= 5440\ \Omega^{-1}m^{-1}.$$

Example (3)

The resistivity of a sample of n-type germanium at 300K is 0.15 Ω.m. If mobility of electron is 0.39 m^2/Vs, calculate the value of donor atoms concentration.

Solution:

Given $e = 1.6 \times 10^{-19}$ C ; $\rho = 0.15\ \Omega m$; $\mu_n = 0.39\ m^2/Vs$

To find N_a

Density of donor atoms in N-type Ge is

$$N_a = \frac{\sigma}{e.\mu_n} = \frac{1}{e.\mu_n \rho}$$

$$= \frac{1}{1.6\times10^{-19}\times0.39\times0.15}$$

$$= 1.07 \times 10^{20}\ m^{-3}.$$

1.11 SELF ASSESMENT QUESTIONS

(I) Long answer questions

1. Classify the solids on the basis of energy band theory of solids.
2. Discuss about energy band theory.
3. Classify the solids on the basis of resistivity.
4. Derive the continuity equation.
5. Explain P- and N-type semiconductors with energy band diagram. Give the concept of hole.

(II) Short answer questions

1. Explain how an N-type semiconductor is formed with the help of energy band diagram.
2. Discuss briefly about diffusion mechanism.
3. Discuss about mobility and carrier life time
4. What is a Fermi level? Indicate its position along with acceptor and donor impurity levels in N-type and P-type semiconductors.
5. What is a continuity equation? How it is formed? Give its significance.
6. Obtain an expression for the conductivity of a semiconductor.

(III) Numerical Problems

(1) Calculate the conductivity of an intrinsic Germanium from the data.

$n_i = 2..4 \times 10^{19}\ m^{-3}$; $\mu_n = 0.39\ m^2/V.s$; $\mu_p = 0.19\ m^2/V.s$

Ans: $2.22 \Omega^{-1} m^{-1}$

(2) Calculate the density of donor atoms to be added to an intrinsic semi conductor to produce n-type semi conductor of conductivity 5

mhos/cm. Given that the mobility of electrons in n-type semi conductor is 0.385 m^2/Vs. **Ans:**

1.12 REFERENCES

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UNIT I **LESSON- 2**

SEMICONDUCTOR DEVICES -I

OBJECTIVES OF THE LESSON

This lesson explains the formation of junction diode. capacitance effects possessed by diode, diode V-I characteristics, Diode equation and its interpretation. Discussion of diode as a non-linear element, reverse saturation current and its variation with temperature; few applications of diode like clipping and clamping.

STRUCTURE OF THE LESSON

2.1 INTRODUCTION

If a junction is formed between p-type and n-type semi conductors, this combination is called a junction diode. It possesses the properties of a rectifier. It is a two terminal device. The two terminals are called anode and cathode .This terminology is borrowed from vacuum tube diodes. As rectifiers diodes play a very important role in providing DC power in almost all the electronic equipment. It forms the basis for a variety of devices like Varactor diode, Schottky diode, Photo diode; Transistor, SCR, UJT etc.

Diode can be used as a wave shaping circuit, based on the non linearity of its I-V characteristic. Understanding the working of diode under forward and reverse bias conditions make it easier to understand the action of transistor. The depletion region of an unbiased diode creates a potential barrier inside diode at the junction. This region exhibits capacitance property; whole value can be changed electrically by changing the bias. This property is used in the design of varactor diodes which can be used like a variable capacitor in tuned circuits for producing oscillations. Special diode like tunnel diode is used to produce oscillations at microwave frequencies.

2.2. DIODE FORMATION

Two types of diodes were developed in the early days. These methods are still being used in producing diodes as discrete components. These two types are 1) Junction diode and 2) Point contact diode. Point contact diodes cannot handle large power. Grown junction diodes are suitable for carrying large currents. So, in this lesson we study the features of junction diodes. A pure Silicon or Germanium crystal is grown first with P-type impurities added to it. After growing a sufficiently thick P-type semiconductor crystal, the impurity is changed to N-type and the growth process is continued to grow N-type semiconductor crystal. After growing N-type semiconductor crystal, impurity is changed to P-type. Thus alternating P and N layers are formed in a Silicon or Germanium crystal. The

crystal is cut in to slices consisting of P-and N-type materials. At the interface of P- and N-type materials, a P-N junction is formed as shown in Fig.2.1. Away from the junction in P-type material, each acceptor atom is associated with a hole and each donor atom in the N-region is associated with a free electron. The free electrons on the N-side diffuse to the P-side and holes on the P-side diffuse into N-side. In this process, very close to the junction, electrons recombine with holes in P-region leaving

bare ions. Consequently, mobile charges are neutralized over a small region of width about 10^{-4} cm to 10^{-6} cm around the junction. This region is called the "*Depletion Region* ", "Space Charge Region "or "Transition Region". In this region, the acceptor atoms on the left side of the junction become negative ions and the donor atoms on the right side of the junction become positive ions. The depletion region is limited to a small region as an electric potential difference appears across the depletion region and this acts as a barrier. It prevents all the electrons in N-region from crossing over the junction. Likewise, holes in P-region are prevented from crossing the potential barrier.

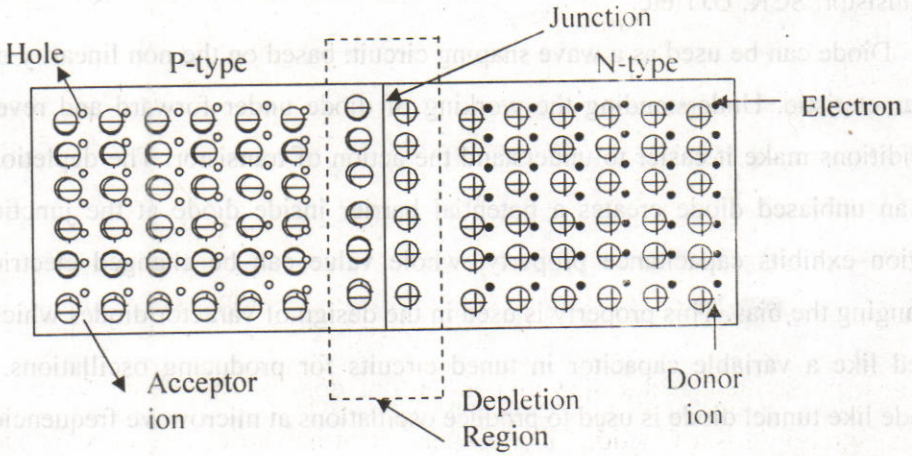


Fig.2.1 P-N junction formation

The combined crystal acts as if a small equivalent battery were placed across the junction, thereby establishing a small voltage across it (V_0). This potential is called the *Barrier Potential* or *Contact Potential*, or *Diffusion Potential*. If the current carriers are to pass the barrier, they must be raised in potential to overcome the barrier.

The barrier potential is given by

$$V_0 = \frac{KT}{q} \ln \frac{N_A N_D}{N_i^2}$$

where K - Boltzmann constant $=8.625 \times 10^{-5}$ eV/K

T - Absolute temperature of the junction.

N_A - No. of acceptor impurity atoms per unit volume.

N_D - No. of donor impurity atoms per unit volume.

N_i - No. of electrons or holes per unit volume in an intrinsic semiconductor.

At 25^0 C, $V_0 = 0.7$V for Si ; 0.3V for Ge.

2.2a DERIVATION OF EXPRESSION FOR BARRIER POTENTIAL (V_0)

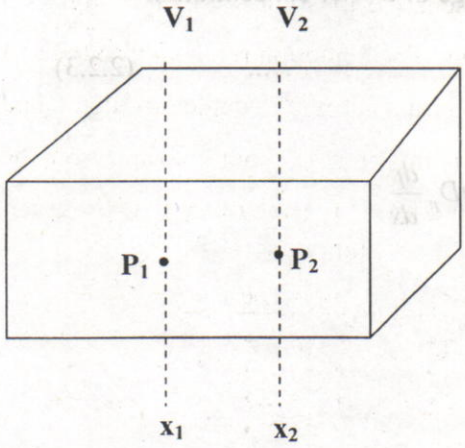


Fig.2.1a

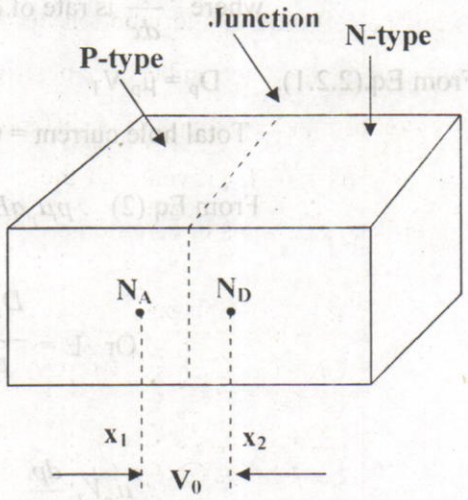


Fig.2.1b

Consider a semiconductor bar with non-uniform doping. This means that the hole concentration p is a function of 'x'. Assume that no carriers are injected and there is no excitation. With no excitation, there can be no steady movement of charge, even if the carriers possess random motion due to thermal agitation. Hence the total current (may be electron or hole current) must be zero.

Since 'p' is a function of x (distance), there can be a non-zero hole diffusion current. To notice a zero hole current, there must be hole drift current which is equal and opposite to the diffusion current. We can conclude that as a result of non-uniform doping, an electric field **E**

is generated with in the semi conductor. We can find this field and the corresponding potential.

Einstein relationship between diffusion D and mobility 'μ' is

$$\frac{D_P}{\mu_P} = \frac{D_n}{\mu_n} = V_T \qquad \text{.....(2.2.1)}$$

where D_p, D_n are the diffusion constants for holes and electrons

μ_p, μ_n are the mobilities of hole and electron

$$V_T = \frac{KT}{q} = \frac{T}{11{,}600}$$

Total hole current in a semi conductor $J_p = p\mu_p E - qD_p \frac{dp}{dx}$ .....(2.2.2)

where $\frac{dp}{dx}$ is rate of change of carrier concentration

From Eq.(2.2.1), $D_p = \mu_p V_T$ ..... (2.2.3)

Total hole current = 0

$\therefore$ From Eq.(2) $p\mu_p qE = qD_p \frac{dp}{dx}$

$$\text{Or } E = \frac{D_p \frac{dp}{dx}}{p\mu_p}$$

$$= \frac{\mu_p V_T \frac{dp}{dx}}{p\mu_p} = \frac{V_T}{p}\frac{dp}{dx} \qquad \text{.....(2.2.4)}$$

If doping concentration p(x) is known, we can calculate E(x)

$$\text{We know that } E = -\frac{dV}{dx}$$

$$\text{Or } dV = -E\,dx = -\frac{V_T}{p}\frac{dp}{dx}dx$$

$$dV = -V_T \frac{dp}{p} \qquad (2.2.5)$$

Integrating this equation between two distances x_1 where concentration is p_1, potential is V_1 and x_2 where concentration is p_2, potential is V_2 : we get

$$\int_{V_1}^{V_2} dV = -V_T \int_{p_1}^{p_2} \frac{dp}{p}$$

$$V_{21} \equiv V_2 - V_1 = -[V_T(\ln p_2 - \ln p_1)]$$

$$\text{or } V_{21} \equiv V_T \ln\left(\frac{p_1}{p_2}\right) \qquad (2.2.6)$$

$$\text{or } p_1 = p_2 e^{\frac{V_{21}}{V_T}} \qquad (2.2.7)$$

This is Boltzmann relationship of kinetic gas theory. Similarly, for electrons

$$n_1 = n_2 e^{\frac{-V_{21}}{V_T}} \qquad \text{.....(2.2.8)}$$

Multiplying Eq.(2.2.7) and Eq.(2.28)

$$n_1 p_1 = n_2 p_2 \quad \ldots\ldots \quad (2.2.9)$$

or n p is constant.

For intrinsic semiconductor, $n = p = n_i$

$$\therefore n\,p = n_i^2 \quad \text{----------(2.2.10)}$$

This is called *Mass Action Law*.

Consider Fig.2.1b. The left half of the bar is P–type with a concentration N_A (acceptor impurity atoms) and the right half at the bar is n-type with a uniform density N_D. The dashed line is a junction (P-N) separates the two sections with different concentrations. Based on above theory, there is a built-in potential between these two sections (called *Contact differenced of potential* (V_0)). We can write by using Eq,(2.2.6), V_0 as

$$V_0 = V_{21} = V_T \ln \frac{p_{p_o}}{p_{n_o}} \quad \text{----------(2.2.11)}$$

Because $p_1 = p_{p0}$ = thermal equilibrium concentration in P-side.

$p_2 = p_{no}$ = thermal equilibrium hole concentration in N-side

But $p_{p0} = N_A$; $p_{n0} = N_i^2 / N_D$ so that

$$V_0 = V_T \ln \frac{N_A N_D}{N_i^2}$$

$$\text{Or } V_0 = \frac{KT}{q} \ln \frac{N_A N_D}{N_i^2} \quad \text{-------(2.2.12)}$$

2.3 WORKING OF DIODE

The working of diode can be understood in two configurations.

i) Forward bias ii) Reverse bias

i) FORWARD BIAS

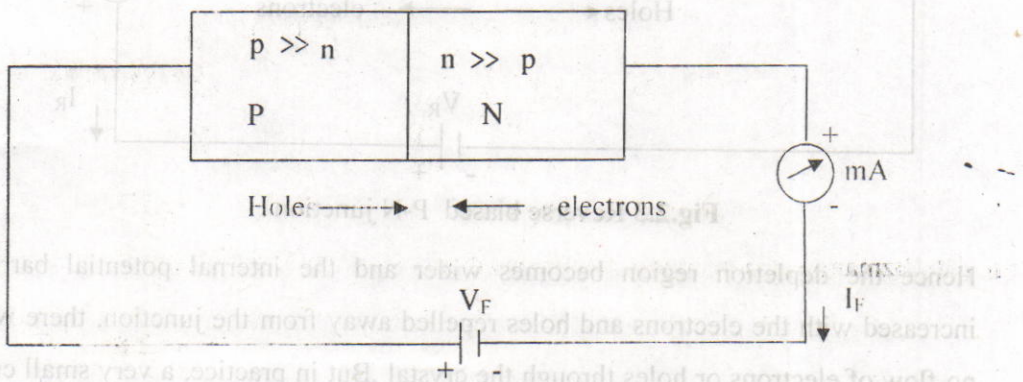


Fig.2.2 Forward biased P-N junction

When the positive terminal of the battery is connected to P-region and negative terminal of the battery is connected to N- region, so that the applied potential difference (V_F) of the battery acts in opposition to the internal barrier potential, the junction is said to be *Forward Biased.* This is shown in Fig.2.2. Under the forward bias condition, the positive terminal of the battery repels the holes in the P- region towards the junction and negative terminal of the battery repels the electrons in the N-region towards junction.

In this process if the applied potential (V_F) is greater than the internal potential barrier (V_0). Under the action of forward potential difference V_F, the majority carriers (electrons in N-region, holes in P-region) flow across the junction in opposite direction and result in a relatively large forward current I_F (of the order of mA). Hence in forward bias, the external battery voltage lowers the junction barrier and also reduces the depletion region width.

ii) REVERSE BIAS

When the positive terminal of the battery is connected to n–region and negative terminal of the battery to the p-region so that the applied potential difference (V_R) acts in the same direction as that of the internal potential barrier, the junction is said to be *Reverse Biased.* This is shown in Fig 2.3. Under the reverse bias condition, majority carriers (electrons in N- region and holes in P-region) are attracted away from the junction. This action effectively increases the no. of negative and positive ions in the depletion region respectively.

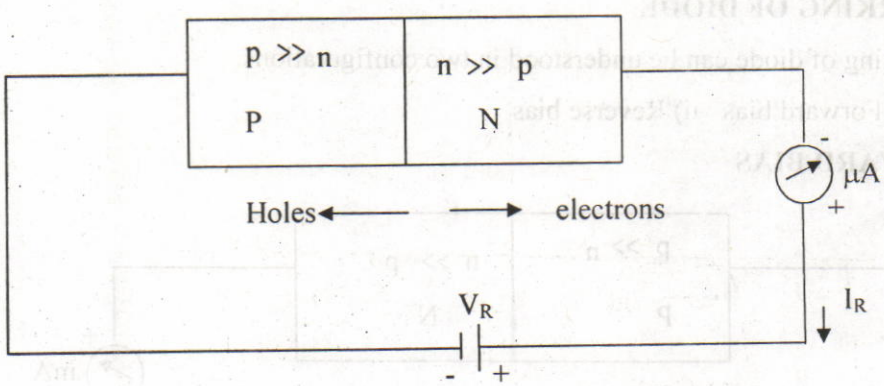


Fig.2.3 Reverse biased P-N junction

Hence the depletion region becomes wider and the internal potential barrier is increased with the electrons and holes repelled away from the junction, there will be no flow of electrons or holes through the crystal .But in practice, a very small current

I_R (of the order of few micro Amperes) flows in the reverse direction. This current is due to minority carriers in both regions. This is small because the number of minority carriers is small. It will be in μA or nA. This reverse current caused by minority carriers is called *saturation current* (I_S or I_0). Hence in reverse bias. the external battery voltage V_R raises the junction barrier. It results in increase of the width of the junction barrier and increases the width of the depletion region.

2.4. I-V CHARACTERISTICS OF A DIODE

Fig 2.4 shows the I-V characteristics of a junction diode.

Forward Characteristics

When the diode is forward biased and the applied voltage V_F is increased from zero, no current flows through the diode in the beginning. It is so because the external voltage is being opposed by the internal barrier potential (V_0 = 0.7V for Si, 0.3V for Ge). As soon as internal barrier potential is overcome, current through the diode increases rapidly with increasing applied voltage.

Reverse Characteristics

When the diode is reverse biased majority carriers are blocked and only a small current (due to minority carriers) flows through the diode. As the reverse voltage V_R increased from zero, reverse current very quickly reaches its saturation value (I_0). It is of the order of nano Amperes (nA) for Si and micro Amperes (μA) for Ge. When the reverse voltage exceeds a breakdown voltage, the saturation current I_0, suddenly and sharply increases indicating very low resistance at this point.

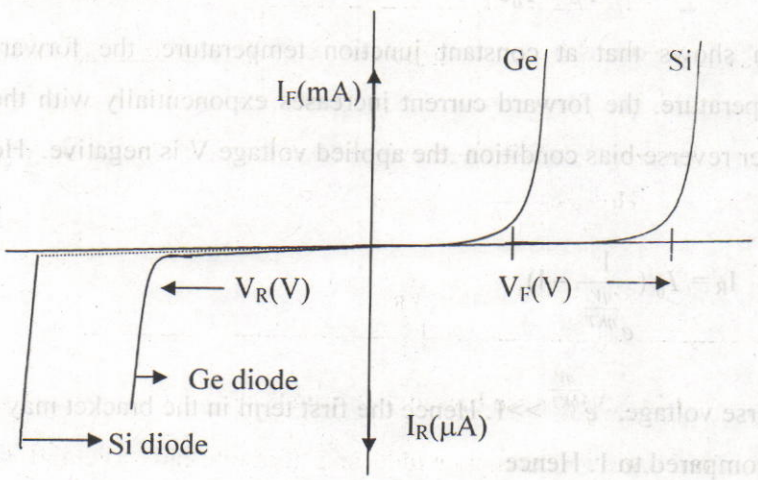


Fig.2.4 I-V characteristics of junction diode

2.5. DIODE EQUATION AND ITS INTERPRETATION:

The current voltage equation of a pn-junction diode is represented theoretically by the relation

$$I = I_0[e^{\frac{qV}{\eta KT}} - 1] \qquad \text{.....(2.5.1)}$$

Where

I_0 = reverse saturation current at T K

I= diode current in amperes

V=Applied voltage in volts

η = constant: η =1 for Ge and η = 2 for Si

q = charge of an electron

K= Boltzmann constant = 8.6×10^{-5} eV/K

This equation is valid for all values of V upto a certain voltage. It gives forward current for positive values of V and reverse current for negative values of V.

For large forward voltage,

$e^{\eta \cdot}$ >>1, hence 1 can be neglected

Hence Eq.(2.5.1) becomes

$$I_{F} = I_0 e^{\frac{qV}{\eta KT}} \qquad \text{..... (2.5.2)}$$

This equation shows that at constant junction temperature, the forward current increases temperature, the forward current increases exponentially with the forward voltage. Under reverse bias condition .the applied voltage V is negative. .Hence from Eq.(2.5.1),

$$I_R = I_0 \left(\frac{1}{e^{\frac{qV}{\eta KT}}} - 1\right)$$

For large reverse voltage, $e^{\frac{qV}{\eta KT}} >> 1$. Hence the first term in the bracket may be neglected as compared to 1. Hence

$$I_R = -I_0 \qquad \text{---------- (2.5.3)}$$

This shows that magnitude of reverse current is I_0 and is independent of applied voltage.

2.6 REVERSE SATURATION CURRENT (I_0)

When a diode is reverse biased, a small amount of current flows through the diode. This current is called *Reverse Saturation Current*. This current is due to the flow of minority carriers across the junction. These minority carriers are generated due to thermal energy. So the current due to minority carriers I_0 is extremely temperature dependent. The dependence of I_0 on temperature is given by

$$I_0 = KT^m e^{\frac{-V_G}{\eta V_T}}$$

Where K is constant,

T is absolute temperature; qV_{Go} is forbidden energy gap in Joules.

For Ge, $m = 2$; $\eta = 1$; $V_{G0} = 0.785V$

For Si, $m=1.5$; $\eta = 2$; $V_{GO} = 1.212V$

$V_T = KT/q$ is the volt equivalent of temperature. From experimental data, it is found that the reverse saturation current approximately doubles for every 10°C rise in temperature.

2.7 CAPACITANCE EFFECTS OF PN - JUNCTION

In many applications of PN-junction, the capacitance is a limiting factor in the usefulness of the device. These capacitances must be considered in designing PN-junction devices for use with time varying signals. Capacitance effects are exhibited by a PN-junction when it is either forward or reverse biased. In reverse bias region, we have the *Transition* or *Depletion Region Capacitance* (C_T); while in the forward bias region, we have *Diffusion Capacitance* (C_D) or *Charge Storage Capacitance*.

i) DIFFUSION or STORAGE CAPACITANCE

This capacitance effect is present when the junction diode is forward biased. It is called Diffusion capacitance to account for the time delay in moving the charges across the junction by diffusion process. This capacitance varies directly with the magnitude of forward current.

It is given by $C_D = \frac{dq}{dV} = \frac{\tau e I}{\eta KT}$

Where

τ - mean life-time of the minority carriers

e - Electronic charge.

I - diode current

η -1 for Ge; 2 for Si

K - Boltzmann constant.

T - Temperature in Kelvin.

Explanation : When a forward biased PN- junction is suddenly reverse biased, a reverse current flows which is large initially but gradually decreases to the level of saturation current I_0. This effect can be linked to the discharging current of a capacitor called *Diffusion Capacitance* (C_D). Since the number of charge carriers left in the depletion layer is proportional to forward current, C_D is directly proportional to the forward current. [$C_D = 0.02\ \mu F$].

TRANSITION CAPACITANCE

This capacitance effect is present when the PN- junction is reverse biased. Here the depletion region acts like a dielectric material. Since the thickness of the depletion layer depends on the amount of reverse bias, C_T can be controlled with the help of applied reverse voltage. The dependence of C_T on voltage is given by

$$C_T = \frac{K}{(V_K + V_R)^n}$$

Where V_K- knee voltage or barrier potential.

V_R - Applied reverse voltage.

K – Constant for a given semiconductor material,

n = 1/2 or 1/3

C_T can also be expressed as $C_T = \frac{\varepsilon A}{W}$

where A - Junction cross-section area.

W - Total space charge or depletion layer width.

Since with increase in reverse voltage, the width or thickness of depletion layer increases, the transition capacitance decreases with increases in reverse voltage. This property of a PN – junction is used in the construction of special type of diode called a " Varactor diode". Its typical value is 40pF.

2.8 DIODE AS A CIRCUIT ELEMENT

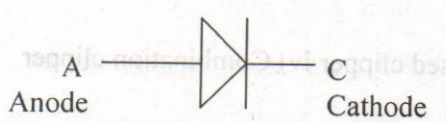
The basic diode circuit consists of the diode in series with a load resistance R_L and an input signal source V_i. The circuit is analysed to find the instantaneous current "i" and the instantaneous diode voltage V when the instantaneous input voltage is V_i

Applying KVL to the input side of circuit in Fig.2.5, we get

$$V_i = V + iR_L$$

Or $$V = V_i - IR_L \quad \text{.....(2.8.1)}$$

where R_L Is the magnitude of load resistance.



Diode Symbol

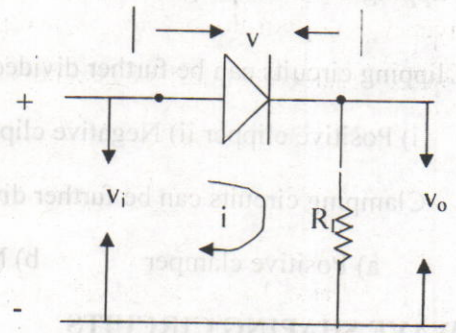


Fig.2.5

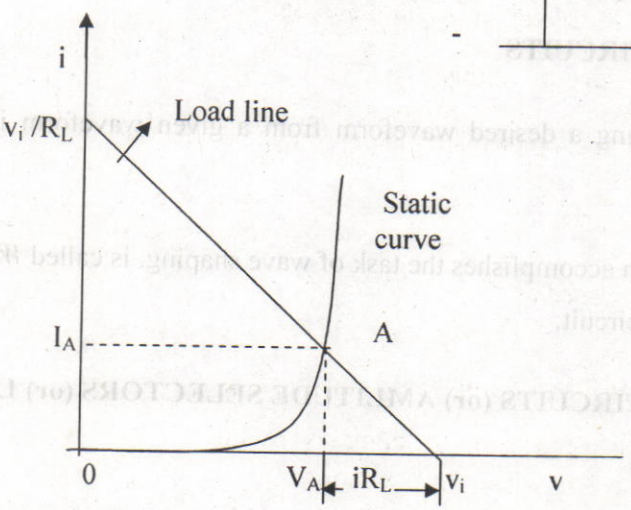


Fig.2.6

The Eq.(2.8.1) is not sufficient, to determine the unknowns V and I. However, a second relation between these two variables is given by the static characteristic of the diode. The straight line represented by Eq.1 is called the *Load Line*. This load line passes through the points ($I = 0$, $v = v_i$) and ($i = v_i/R_L$, $v = 0$). Here v_i and v_i/R_L are the intercepts. The slope of this line is determined by R_L. The point of intersection A of the load line and the static curve gives the current i_A that will flow under these conditions. This construction determines the current in the circuit when the instantaneous input voltage is v_i. From the curve shown in Fig.2.6, we can conclude that the diode is a non-linear circuit element. This is because its I-V characteristic is not a straight line. Diode behaves in different ways in forward and reverse bias conditions.

2.9 APPLICATIONS OF DIODE

Diodes can be used to clip and clamp waveforms. Clip means to remove or to eliminate, and clamp means to fix at a fixed voltage level. These circuits are called *Clipping* and *Clamping circuits*.

Clipping circuits can be further divided into

i) Positive clipper ii) Negative clipper iii).Biased clipper iv) Combination clipper

Clamping circuits can be further divided into

a) Positive clamper b) Negative clamper

WAVE SHAPING CIRCUITS

The process of deriving a desired waveform from a given waveform is termed as Wave Shaping.

The circuit, which accomplishes the task of wave shaping, is called *Wave-shaping* circuit. Ex: Clipping circuit.

2.9.1 CLIPPING CIRCUITS (or) AMLITUDE SELECTORS (or) LIMITERS (or) SLICERS

A circuit, which removes (or clips) a portion of the applied wave, is known as *Clipping Circuit*. Clippers are used in various electronic systems. Various

types of clippers are i) Positive clipper ii) Negative clipper iii) Biased clipper iv) Combination clipper.

i) POSITIVE CLIPPER

A positive clipper removes the positive half cycles of the input voltage by taking the advantage of the nonlinear v-I characteristic of semiconductor diode.

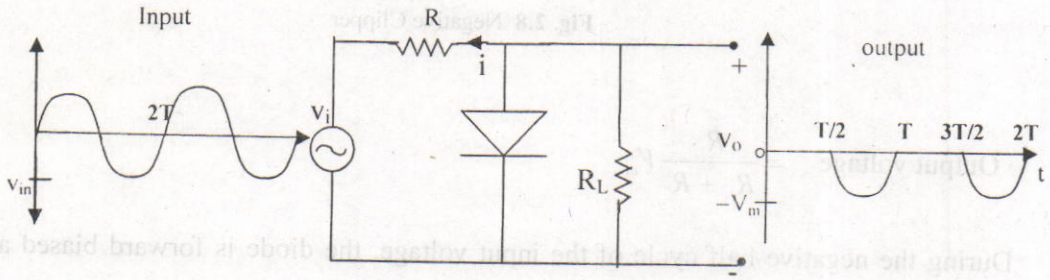


Fig. 2.7 Positive clipper

Fig.2.7 shows the circuit of a positive clipper. As shown in figure, the output voltage has only negative half cycles i.e positive half cycles are clipped.

Working: During the positive half cycle of the input, the diode is forward biased and hence conducts heavily. So no voltage appears across the diode or load i.e the output is zero. During the negative half cycle of the input, diode is reverse biased and behaves as an open circuit. So the voltage appears across the load. In this condition, the circuit behaves as a voltage divider with an output of given by

$$\text{Output voltage} = \frac{R_L}{R_L + R} V_m$$

ii) NEGATIVE CLIPPER

A negative clipper removes the negative half cycles of the input voltage. Fig.2.8 shows the circuit of a negative clipper. As shown in figure, the output has only positive half cycles i.e negative half cycles have been clipped. Note the way diode is connected across the voltage source. During the positive half cycle of the input voltage, the diode is reverse biased and hence does not conduct. It acts as an open-circuit, voltage appears across the load during positive half cycles. given by

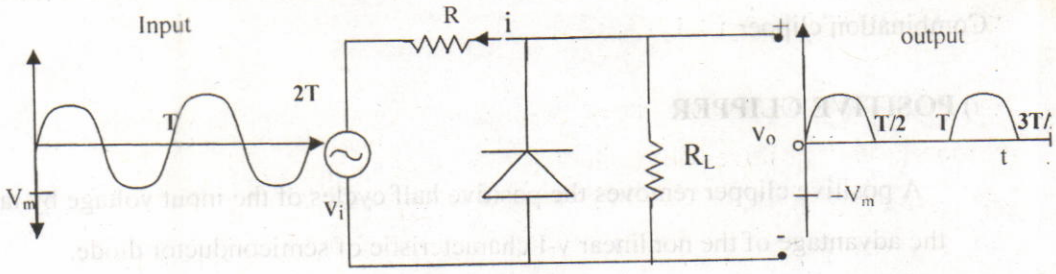


Fig. 2.8 Negative Clipper

$$\text{Output voltage} = \frac{R_L}{R_L + R} V_m$$

During the negative half cycle of the input voltage, the diode is forward biased and hence conducts heavily. Now the diode behaves as a short-circuit. Hence no voltage appears across the load.

iii) BIASED CLIPPER

It is also a clipper circuit, but an extra voltage source is to be connected in series with the diode. This clipper is used to remove a small portion of positive or negative half cycle of the signal.

Working: Fig.2.9 shows the circuit of a biased positive clipper. The diode will conduct heavily as long as the input voltage is greater than the battery voltage V .When this happens; the diode behaves as a short circuit and the output equals +V. During the period when the input voltage is less than +V, the diode is reverse biased and behaves as an open-circuit. Therefore, most of the input voltage appears across the output. In this way the biased positive clipper removes the input voltage above +V.

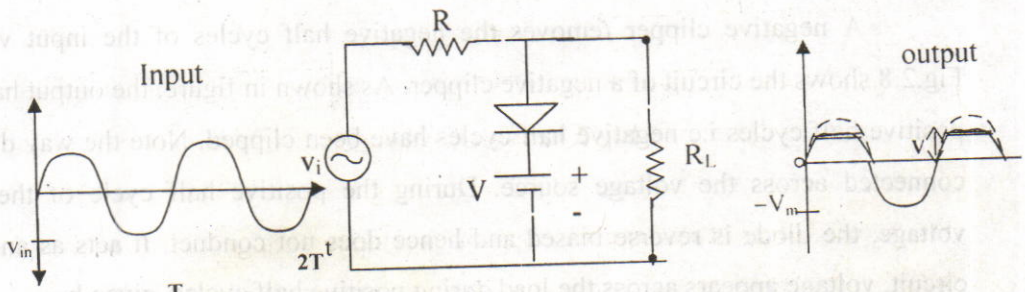


Fig.2.9 Biased clipper

iv) COMBINATION CLIPPER

It is a combination of biased positive and negative clipper. With this clipper, a portion of both positive and negative half cycles of input voltage can be removed as shown in Fig.2.10.

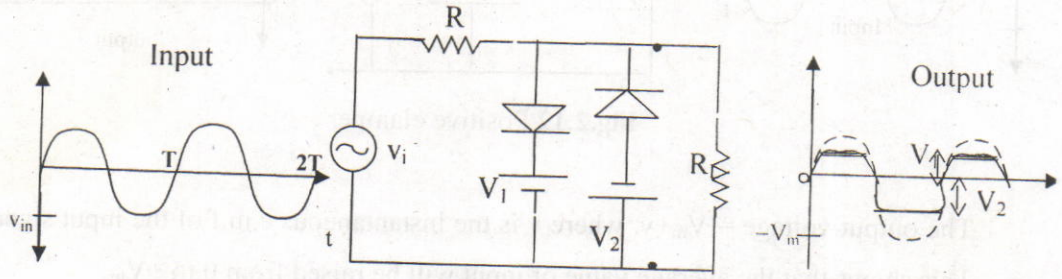


Fig.2.10 Combination clipper

2.9.2 CLAMPING CIRCUITS

Clamping: The process of introducing a d.c level into an a.c signal is known as Clamping. A circuit that places either the positive or negative peak of a signal at a desired d.c level is known as a *Clamping Circuit*. In a clamping circuit, the shape of original signal will not change.

a) POSITIVE CLAMPER

The positive clamper adds the d.c component and pushes the signal upwards so that negative peaks fall on the zero level. Fig.2.12 shows the circuit of a positive clamper. It consists of a diode and a capacitor.

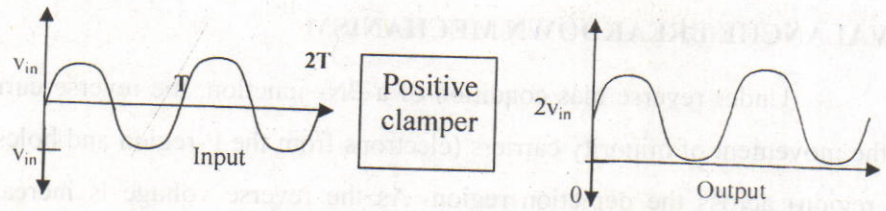


Fig.2.12 Positive clamper

Working: During the negative half of the input voltage, the diode conducts heavily and behaves as a short circuit .At the negative peak the capacitor is

charged to V_m with the polarities as shown in Fig.2.12. This capacitor acts as a battery. During the positive half cycle of the signal, the diode is reverse biased and

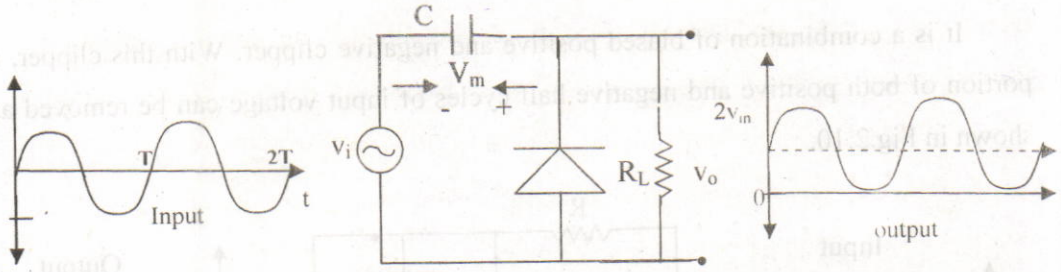


Fig.2.12 Positive clamper

The output voltage = V_m+v, where v is the instantaneous e.m.f of the input signal. This shows that the average value of input will be raised from 0 to +V_m.

b) NAGATIVE CLAMPER

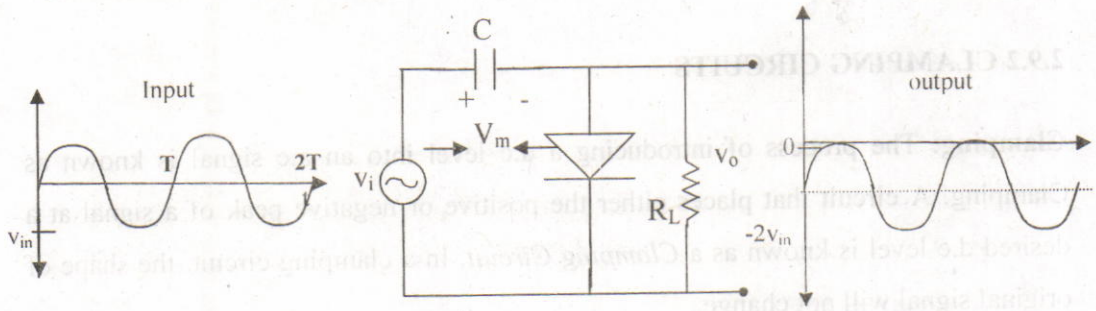


Fig.2.13 Negative clamper

For negative clamper the anode and cathode leads of the diode are to be inverted .the output voltage becomes: output voltage = V-V_m. the working is same as that of positive clamper.

2.10 AVALANCHE BREAKDOWN MECHANISM

Under reverse bias condition of a PN- junction, the reverse current is due to the movement of minority carriers (electrons from the P-region and holes from the N- region) across the depletion region. As the reverse voltage is increased, a minority electron passing through the depletion region gains large kinetic energy from the applied voltage. When this electron collides with a crystal atom, an electron in a covalent bond may acquire sufficient energy to become free from the bond. In this process, the covalent bond is broken and an electron-hole pair is generated. Thus one

electron, on collision with a crystal atom, generates a pair of an electron and a hole. By the same process, each of the carriers, in turn, generates a pair of an electron and a hole. Thus in the process of collision and subsequent breaking up of covalent bonds, the number of free electrons and holes goes on increasing. This cumulative phenomenon is called *Avalanche Multiplication*. Consequently a large reverse current flows through the junction and the diode is said to be in the avalanche breakdown region.

2.11. ENERGY –BAND DIAGRAM OF A PN- JUNCTION

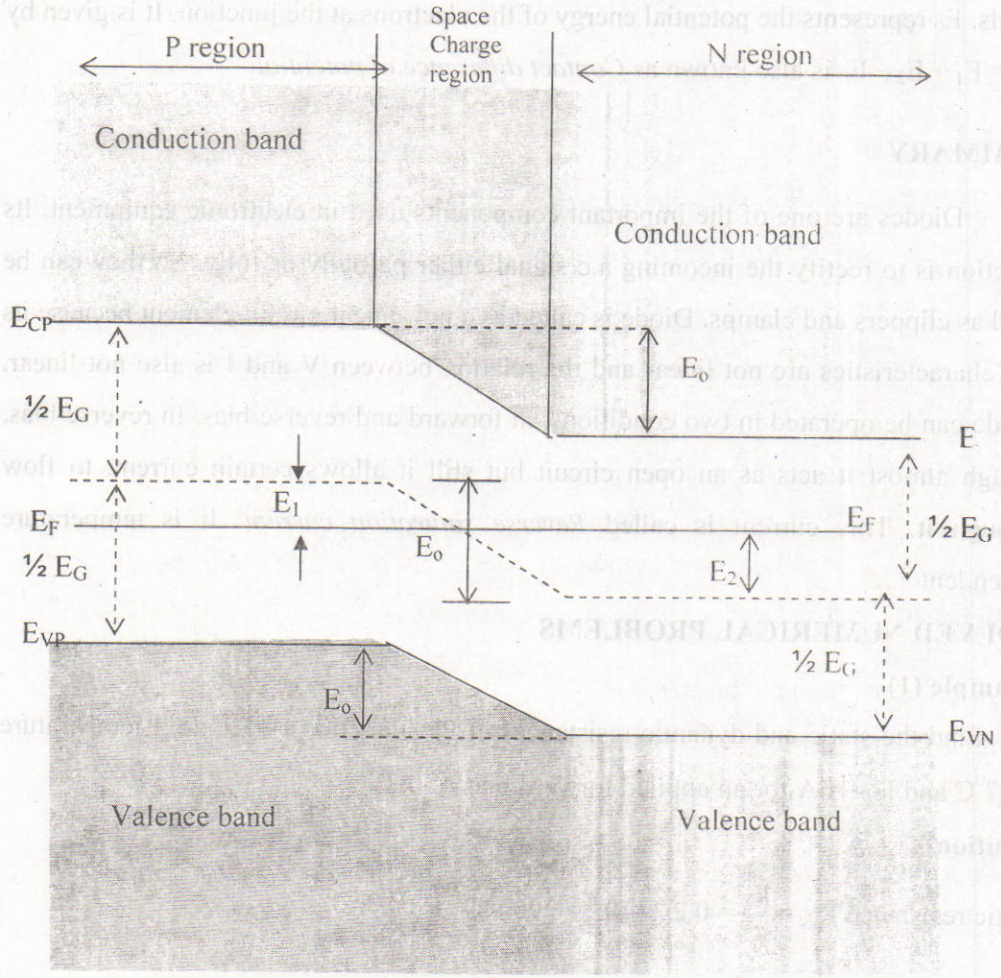


Fig.2.14 Band diagram of P-N junction under open circuit conditions.

Consider that a PN - junction is formed by placing P-and N-type materials in intimate contact on an atomic scale. Under these conditions, the Fermi level must remain

constant throughout the specimen at equilibrium. If this does not happen, electrons on one side of the junction would have an average energy higher than those on the other side. Also, there would be a transfer of electrons and energy until the Fermi levels in the two sides did line up.

We know that the Fermi level E_F is closer to the conduction band edge (E_{CN}) in an N-type material and closer to the valance band edge (E_{VP}) in the P-type material. Clearly the conduction band edge E_{CP} in P-material can not be at the same level as E_{CN} and the energy band edge E_{VN} in the n-side line up with E_{VP}. Hence the energy band diagram for a P-N junction appear as shown in Fig.2.14.In the figure, E_0 is the shift in energy levels. E_0 represents the potential energy of the electrons at the junction. It is given by $E_0 = E_1 + E_2$. E_0 is also known as *Contact difference of potential*.

SUMMARY

Diodes are one of the important components used in electronic equipment. Its function is to rectify the incoming a.c signal either partially or fully. So they can be used as clippers and clamps. Diode is called as a non-linear circuit element because its I-V characteristics are not linear and the relation between V and I is also not linear. Diode can be operated in two conditions, in forward and reverse bias. In reverse bias, though almost it acts as an open circuit but still it allows certain current, to flow through it. This current is called *Reverse saturation current*. It is temperature dependent.

SOLVED NUMERICAL PROBLEMS

Example (1)

Find the static and dynamic resistances of PN- junction Ge diode if temperature is 27^0C and $I_0 = 1\mu$A for an applied forward bias of 0.2V.

Solution

Static resistance $R_{dc} = \frac{V}{I} = 0.2/1x10^{-6} = 200\ K\Omega$.

The dynamic resistance $R_{ac} = \frac{26}{I}$ when I is in mA ; Hence I=1000 mA

$$V_T = \frac{KT}{e} = \frac{1.38x10^{-23}x300}{1.6x10^{-19}}$$

Since I = 1000mA

$$\therefore R_{ac} = \frac{26}{I} = \frac{26}{1000} = 0.26\Omega$$

Example (2)

A PN- junction silicon diode conducts 240mA current when a forward voltage 0.8V is applied. Find (i) Current for forward voltage of 0.7V (ii) Reverse saturation current

Solution:

Given: V = 0.8V; η=2 for Si

(i) From diode equation ,

$$I = I_o\left[e^{qV/\eta KT} - 1\right] \qquad T = 27^oC = 300\ K$$
$$= I_o\left[e^{V/\eta KT} - 1\right]$$

$$V_T = \frac{KT}{q} = \frac{1.38x10^{-23}x300}{1.6x10^{-19}} = 0.026V$$

$$\eta = 2\ for Si$$

$$I = I_o\left[e^{0.8/(2x0.026)}\right]$$

$$I^1 = I_o\left[e^{0.7/(2x0.026)}\right]$$

$$\frac{I^1}{I} = \exp\left[\frac{0.7-0.8}{2x0.026}\right]$$

$$I^1 = 240x10-3\exp\left[\frac{0.7-0.8}{0.052}\right] = 35mA$$

(ii) From diode equation

$$240x10^{-3} = I_R\left[e^{0.8/0.052}\right]$$

$$I_R = \frac{240x10^{-3}}{4.8x10^6} = 50x10^{-9}A = 50nA$$

3.6 SELF ASSESSMENT QUESTIONS

(I) Long answer questions

(1) Explain how a diode is forward biased. Discuss its action in forward bias and reverse bias.

(2) Explain the applications of diode in clipping circuits.

(3) Explain the applications of diode in clamping circuits.

(4) Explain the energy band diagram of an intrinsic semiconductor.

(II) Short answer questions

(1) Write the diode equation and give its interpretation.

(2) What is reverse saturation current? How it varies with temperature?

(3) Discuss action of clipping circuits.

(4) Explain the diode action as a circuit element.

(5) Draw the circuit diagram of a positive clipper circuit.

(6) Draw the circuit diagram of a negative clipper circuit.

(7) Draw the circuit diagram of a positive clamping circuit.

(8) Draw the circuit diagram of a negative clamping circuit

(III) Numerical problems

1) Under large reverse bias voltage, the current flowing through a P-N junction diode at room temperature is 40μA. Calculate the current when 0.1V is applied. Ans: 18.32 μA

3.7 REFERENCES

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UNIT I **LESSON 3**

SEMICONDUCTOR DEVICES -II

OBJECTIVES OF THE LESSON

Details of construction and applications of special purpose diodes like Zener diode, Varactor diode, tunnel diode, metal-semi conductor diode are given. It also gives you the basic idea of Tunneling mechanism in tunnel diode.

STRUCTURE OF THE LESSON

3.1 ZENER DIODE

Zener diode is a heavily doped Silicon or Germanium PN-junction diode with a sharp breakdown voltage. This is operated in the breakdown region where current is limited by both external resistance and power dissipation of diode. Zener breakdown occurs due to the breaking of covalent bonds by strong electric field setup in the depletion region by the reverse voltage. Fig.3.1 shows symbol and equivalent circuit of Zener diode.

3.1.1 I-V CHARACTERISTICS

Fig 3.2 shows the I-V characteristics of a Zener diode. Under forward bias condition, it acts like an ordinary junction diode and the characteristics are similar to junction diode forward characteristic.

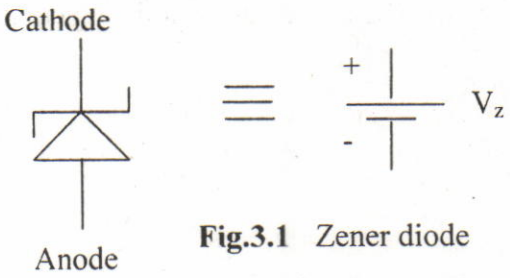

Fig.3.1 Zener diode

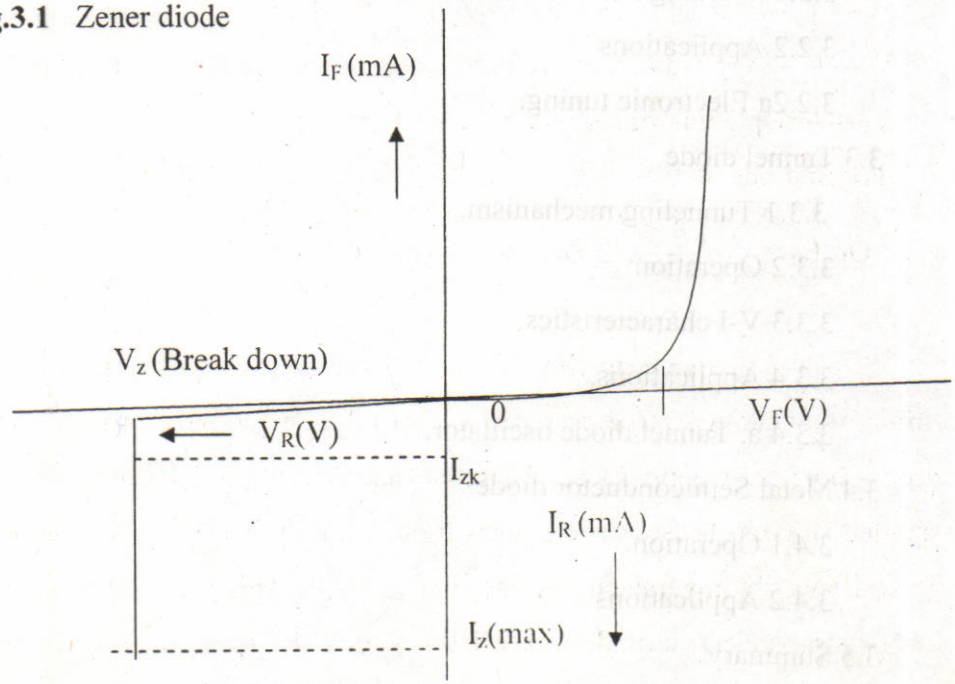

Fig 3.2 Zener diode I-V characteristic

Under reverse bias condition, as the reverse voltage V_R is increased, the reverse current I_R remains extremely small up to the knee of the curve. At this point, the breakdown begins the Zener resistance begins to decrease and the current increases rapidly. From the bottom of the knee, the breakdown voltage $V_{Z(Br)}$ remains essentially constant. This regulating ability is the key feature of the Zener diode. There is a maximum current $I_{Z\,(MAX)}$ above which the diode will be damaged. For ordinary diode, the breakdown due to reverse bias voltage is irreversible .The diode gets permanently damaged. In the case of Zener diode, the breakdown is reversible i.e., even after exceeding the breakdown voltage, the diode will not get damaged.

3.1.2 ZENER BREAKDOWN MECHANISM

In a PN - junction diode in which P- and N- regions are heavily doped. the width of the depletion region is very small. It is of the order of 5×10^{-8} m. The electric field at the junction is given by

$$E_0 = \frac{2(V_0 - V)}{d} \qquad \text{---------- (3.1.1)}$$

V_0--------Internal potential barrier 0.7V for Si : 0.3V for Ge.

V ---------Applied reverse voltage across the junction and is negative

d--------depletion region width = 5×10^{-8} m

For Si diode, if V = -5 V then

$$\text{Or } E_0 = \frac{11.4}{5 \times 10^{-8}} = 2.28 \times 10^8 \ \frac{V}{m}$$

An electric field of such high magnitude exerts a large force on valance electrons of Si atoms. Consequently the covalent bonds are broken and a large number of electron – hole pairs is produced. These carriers are then accelerated away from the junction by the applied voltage. These carriers break more covalent bonds producing more number of charge carriers. .Hence the reverse current increases rapidly. This process by which covalent bonds are broken by strong electric field, is called *Zener breakdown* and the reverse voltage at which break down takes place is called *Zener breakdown voltage*.

3.1.3 APPLICATIONS OF ZENER DIODE

1. It can be used as a voltage regulator
2. It can be used as a fixed reference voltage source in a network for biasing.
3. it can be used for calibrating voltmeters.
4. It can be used as a peak clipper
5. It can be used for meter protection against damage.

3.1.3a VOLTAGE REGULATOR

Regulation: It is a measure of circuit's ability to maintain a constant output voltage even when either the input voltage or load current varies. A Zener diode when working in the breakdown region can serve as a voltage regulator.

ZENER DIODE AS A VOLTAGE REGULATOR

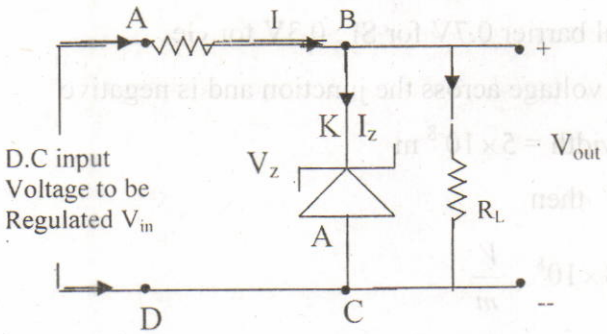

Fig 3.3 Zener voltage regulator

In Fig.3.3, V_{IN} is the DC input voltage whose variations are to be regulated. R is a series limiting resistor. The Zener diode, with a breakdown voltage V_Z, is reverse connected across V_{IN}. When potential across the circuit is greater than V_Z, it conducts and draws relatively large current through the series resistance R. The load resistance R_L across which voltage (V_{OUT}) is required, is connected in parallel with the diode.

Applying Kirchhoff's Voltage Law to the loop ABCDA, we get

$V_{IN} = IR + V_Z$ ---------- (3.1.2.1)

Similarly applying Kirchhoff's Current Law to the node 'B', we get.

$I = I_L + I_Z$ ---------- (3.1.2.2)

But $V_Z = V_{OUT}$

Eq.(3.1.2.1) becomes

$$V_{IN} = IR + V_{OUT}$$

or $$V_{OUT} = V_{IN} - IR$$

Case (1): when V_{IN} is varied and R_L is fixed

(a) When V_{IN} increases

When V_{IN} is increased slightly above the breakdown voltage V_Z. The total current I will increase. This increase in I will be absorbed by the zenor diode without affecting I_L. The increase in V_{IN} will be dropped across R, thereby keeping V_{OUT} constant.

(b) **When V_{IN} decreases** : (Let V_{IN} be slightly greater than V_Z)

If $V_{IN} < V_Z$ (breakdown voltage) the diode will not be in breakdown region and a part of the input voltage will appear across the load. So no regulation action will take place. When V_{IN} is decreased slightly (but still greater than V_Z), the total current I will decrease. This decrease in I will be compensated by the Zener diode without affecting I_L. The decrease in V_{IN} will appear as a fall in voltage across R, there by keeping V_{OUT} constant.

Case (2): When V_{IN} is constant, R_L is varied

(a) When R_L increases

When R_L increases, load current I_L decreases. Hence I_Z increases but IR drop across the load remains constant. So V_{OUT} remains unchanged.

(b) When R_L decreases

When R_L is decreased, the load current I_L increases and hence I_Z decreases, there by keeping IR drop (voltage drop) across the load constant. In this way, V_{OUT} remains unchanged.

3.2 VARACTOR DIODE

The Varactor is a shortened form of variable reactor, referring to the voltage variable capacitance of reverse biased PN – junction. It is also called varicap diode, or voltage variable capacitance diode.

Definition: A Varactor diode is a reverse biased PN – junction diode whose mode of operation depends on its junction capacitance C_J.

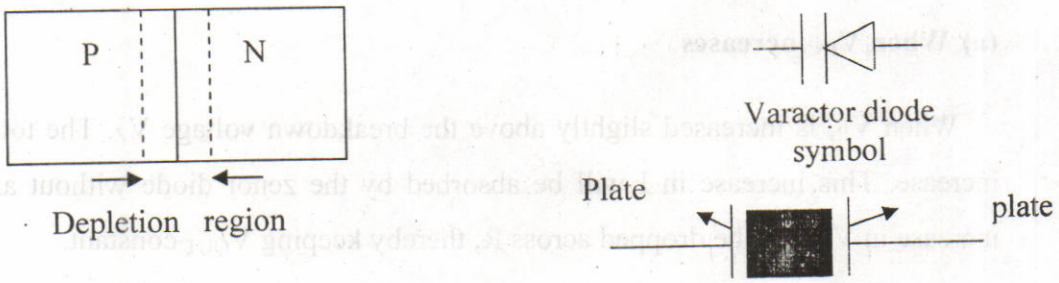

Fig.3.4 Varactor diode

3.2.1 WORKING and C-V CHARACTERISTICS

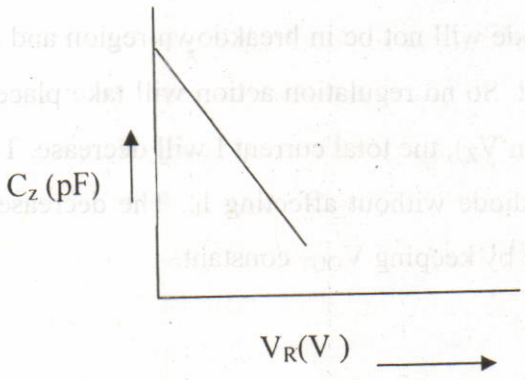

Fig.3.5 C-V Characteristics

As Varactor diode is similar to an ordinary diode, its V-I characteristics have no importance. Hence, we discuss its capacitance – voltage characteristic to understand its working. This curve

[C-V characteristics] can be drawn by taking the reverse voltages applied to the diode along X-axis and the noticed junction capacitance values along Y-axis.

A diode with a reverse bias has an arrangement similar to a capacitor. The P-type and N-type materials semi conduct and forms two parallel plates. The depletion region is an insulator and forms the dielectric. By adjusting the reverse bias, the width of the depletion region (dielectric) is changed and hence the capacitance of the diode changes with a high reverse bias, the capacitance will be low because the depletion region widens. With a little reverse bias. the depletion region is narrow and this makes the diode capacitance to increase. The junction capacitance (C_J) varies with reverse voltage as $C_J = V_R^{-n}$ where n varies from 1/3 to 1/2. The variation of junction capacitance with applied reverse voltage is shown in Fig.3.5.

3.2.2 APPLICATIONS OF VARACTOR DIODE

i) Automatic frequency control device.

ii) FM modulator.

iii) Adjusting band pass filter.

iv) Parametric amplifier.

v) Mixer

3.2.2 (a) ELECTRONIC TUNING

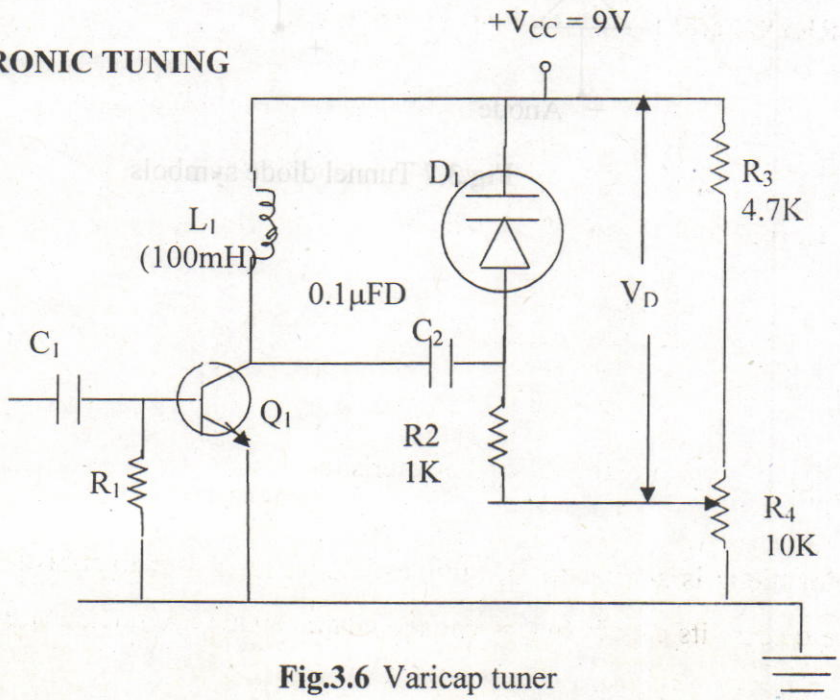

Fig.3.6 Varicap tuner

The major application Varactor diode is as tuning capacitor to adjust the frequency of resonance circuits. An example of this is the circuit shown in Fig 3.6 which is an amplifier with a tuned circuit load. The amplifier produces an output at the resonance frequency of the tuned circuit. The Varactor diode provides the capacitance (C_T) of the resonance circuit. and this can be altered by adjusting the diode (reverse) bias voltage (V_D). So the resonance frequency of the circuit can be varied. C_1 is a coupling capacitor with a capacitance much larger than that of the Varactor diode and R_2 limits the Varactor diode forward current in the event that it becomes forward biased.

3.3 TUNNEL DIODE

This diode was developed by Dr. Leo Esaki in 1958. It is a high conductivity two terminal P-N junction diode having doping density about 1000 times higher as compared to an ordinary junction diode. Th :e diodes are made from Ge , Ga As, Ga Pb.

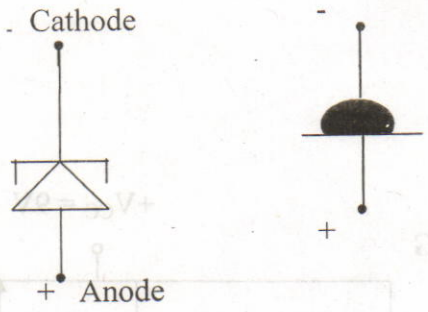

Fig.3.7 Tunnel diode symbols

CONSTRUCTION

It is basically a P-N junction diode in which both P and N regions are heavily doped. i.e the concentration of impurity atoms is greatly increased (about 1 part in 10^3). Because of this heavy doping, the width of the depletion layer becomes very small (≈100Å) (10^{-8}m). Due to the extremely thin depletion layer, electrons are capable of tunneling through from one side of the junction to the other at relatively low forward bias voltage, even less than 0.5V. The symbols are shown in Fig.3.7.

3.3.1 TUNNELING PHENOMENON

In a normally doped P-N junction, the depletion layer is relatively wide and a potential barrier exists across the junction. The charge carriers on either side of the junction cannot cross over unless they possess sufficient energy to overcome this barrier. We know that the width of the depletion region depends directly on the doping density of the semiconductor.

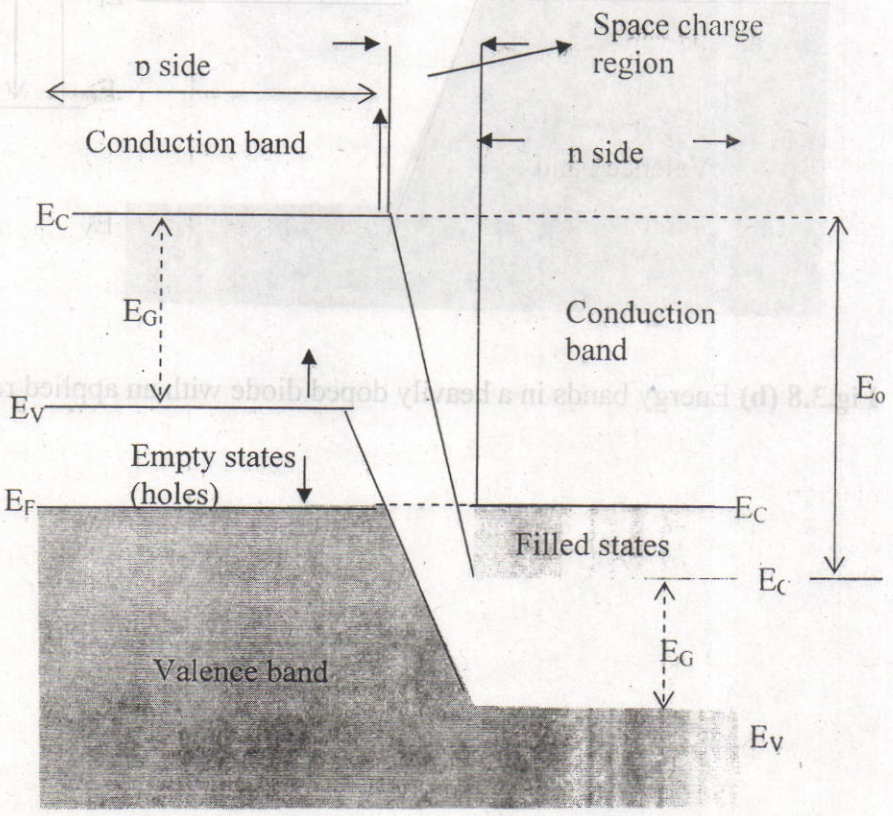

Fig.3.8 (a) Equilibrium (zero bias) conduction, no net tunneling

If a P-N junction is doped very heavily (1000 times or more) its depletion layer becomes extremely thin (about 0.00001mm).under such conditions; many carriers can '*punch through*' the junction with speed of light even when they do not possess enough energy to over come the potential barrier. Hence, large forward current is produced even when the applied voltage is much less than 0.5V.

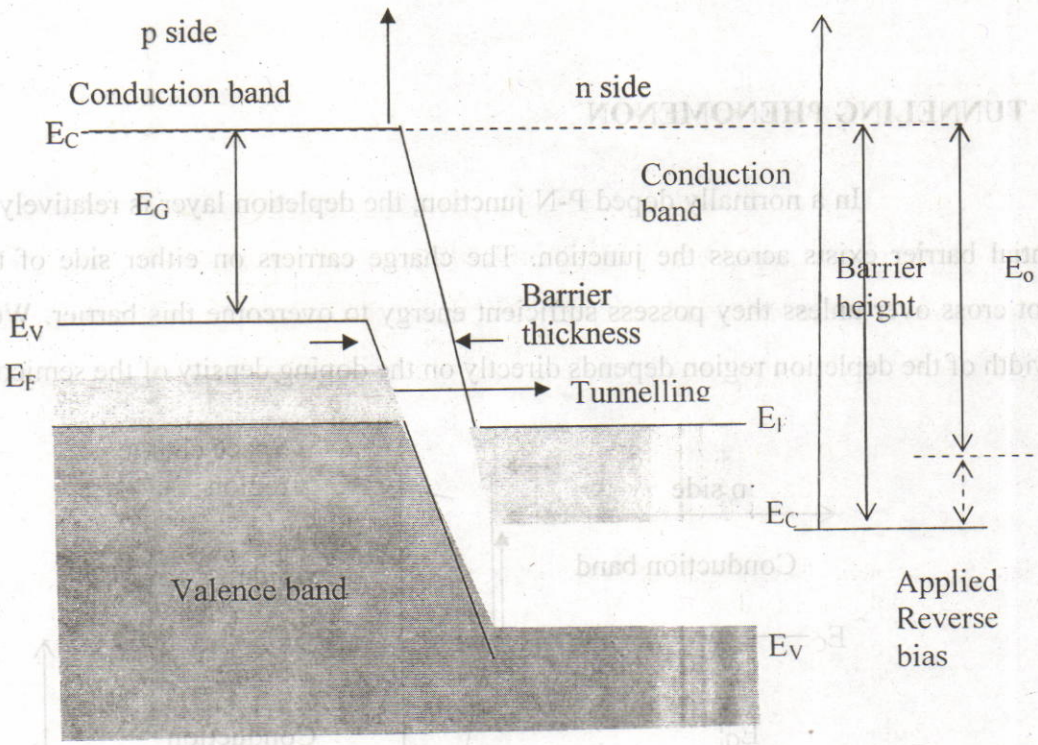

Fig.3.8 (b) Energy bands in a heavily doped diode with an applied reverse bias

The conduction mechanism in which charge carriers, possessing very little energy, bore through a barrier directly instead of climbing over it is called TUNNELING.

3.3.2 TUNNEL DIODE OPERATION

In a tunnel diode, Fermi level is constant through out the junction in equilibrium condition. i.e E_{fp} lies below the valence band edge on the p-side and E_{fn} is above the conduction band edge on the N-side.

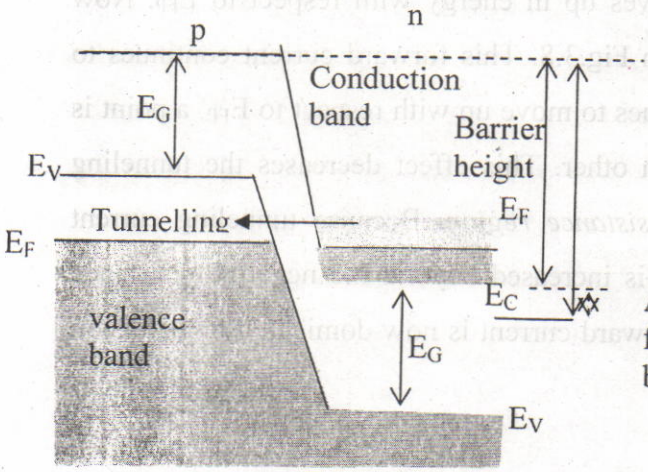

Fig.3.9a The energy band diagram of a heavily biased diode for a small forward bias

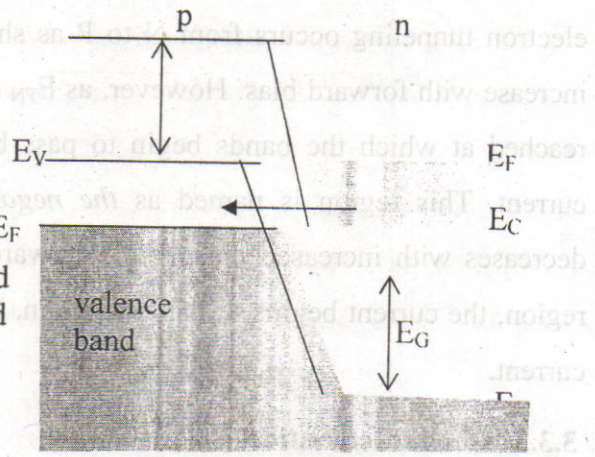

Fig3.9b The energy band diagram of a heavily biased diode for an increased forward bias

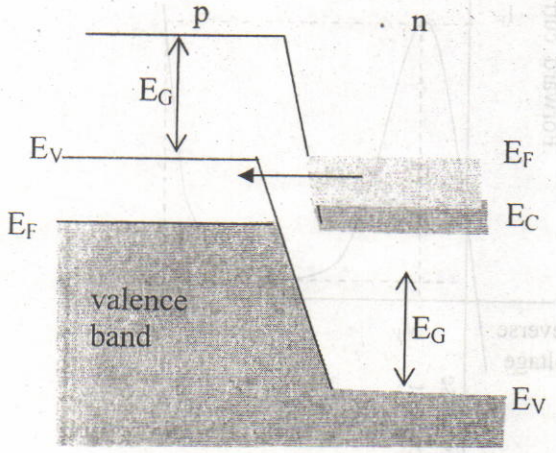

Fig.3.9c The energy band diagram of a heavily biased diode for an increased forward bias

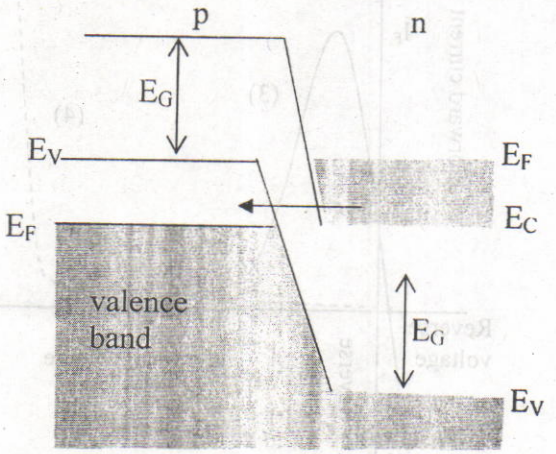

Fig.3.9d The energy band diagram of a heavily biased diode for an heavy forward bias

A small reverse bias allows **electrons tunneling** from P to N. As the reverse bias is increased. E_{Fn} continues to move down with respect to E_{FP}, thereby increasing the tunneling of electrons from P to N.

When a small forward bias is applied, E_{FN} moves up in energy with respect to E_{FP}. Now electron tunneling occurs from N to P as shown in Fig.3.8. This forward current continues to increase with forward bias. However, as E_{FN} continues to move up with respect to E_{FP}, a point is reached at which the bands begin to pass by each other. This effect decreases the tunneling current. This region is named as *the negative resistance region*. Because tunneling current decreases with increased bias. If the forward bias is increased beyond the negative resistance region, the current begins to increase again. The forward current is now dominated by diffusion current.

3.3.3 V-I characteristics

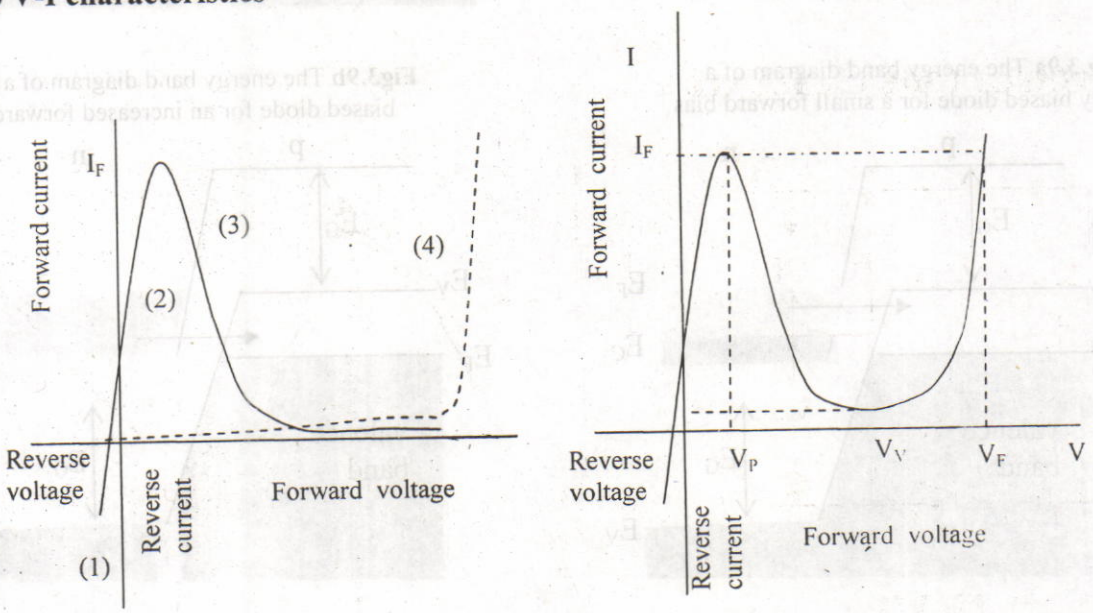

Fig.3.10 Tunnel diode V-I characteristic

From I-V characteristics of tunnel diode we see that the tunnel diode is an excellent conductor in the reverse direction. For small forward voltages (up to 50mV for Ge), the resistance remains small (of the order of 5Ω). At the peak current I_P, corresponding to the voltage V_P. The slope dI/ dV of the characteristic is zero. If the forward voltage is increased beyond V_P, then current decreases. Hence the dynamic conductance g = dI/dV is negative. The tunnel diode exhibits a negative resistance characteristic between the peak current I_P and valley current I_V .Beyond the valley point, the resistance becomes and remains positive. At the peak forward voltage V_F, the current again reaches the value I_P. For larger voltages, current increases beyond this value.

3.3.4 APPLICATIONS

(1) Tunnel diode is used as an ultra high speed switch.

(2) It is used as logic memory storage device.

(3) As a microwave oscillator at a frequency of about 10GHZ.

(4) It is used in relaxation oscillator circuits.

(5) It is used as an amplifier.

3.4a TUNNEL DIODE OSCILLATOR

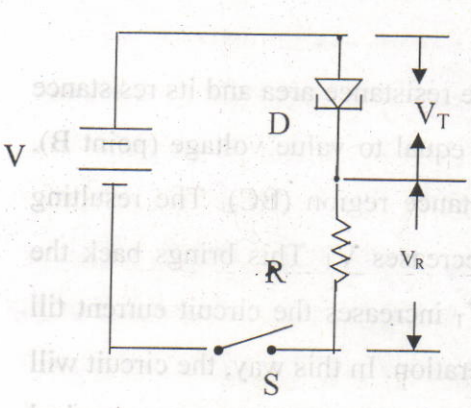

Fig.3.11

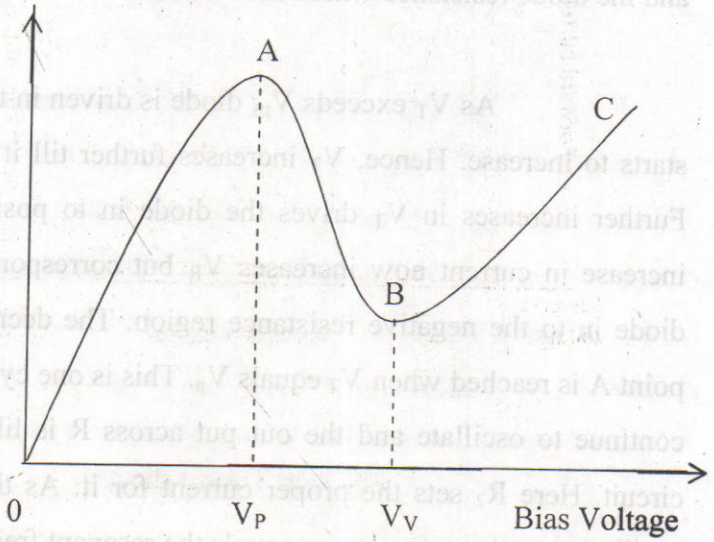

Fig.3.12

The negative resistance region of the I-V Characteristic of tunnel diode produces power. By offsetting losses in L and C components of a tank circuit, such a negative resistance permits oscillations.

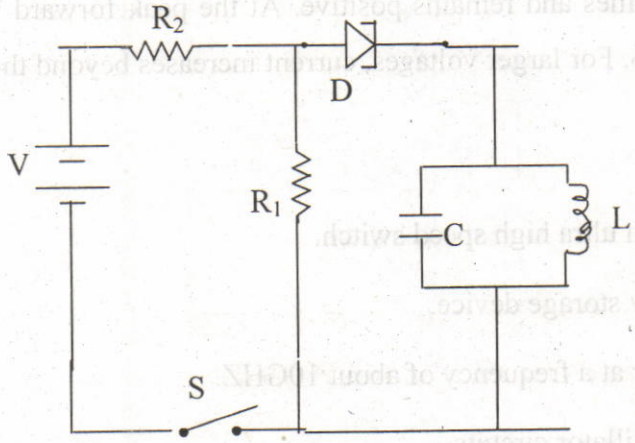

Fig.3.13 Tunnel diode oscillator

In the circuit of Fig.3.11, the value of R is so selected as to bias the diode D in the negative resistance region AB. When S is closed, the current immediately rises to a value determined by R and the diode resistance which are in series.

As V_T exceeds V_p, diode is driven in to negative resistance area and its resistance starts to increase. Hence, V_T increases further till it becomes equal to value voltage (point B). Further increases in V_T drives the diode in to positive resistance region (BC). The resulting increase in current now increases V_R but correspondingly decreases V_T. This brings back the diode in to the negative resistance region. The decrease in V_T increases the circuit eurrent till point A is reached when V_T equals V_p. This is one cycle of operation. In this way, the circuit will continue to oscillate and the out put across R is like a sine wave. Fig.3.13 shows a practical circuit. Here R_2 sets the proper current for it. As the switch S is closed, the diode is set into oscillations, whose frequency equals the resonant frequency of the tank.

3.4 SCHOTTKY DIODE / METAL – SEMICONDUCTOR DIODE

This is also known as Schottky –barrier, surface-barrier, or hot-carrier diode or hot-electron diode

CONSTRUCTION

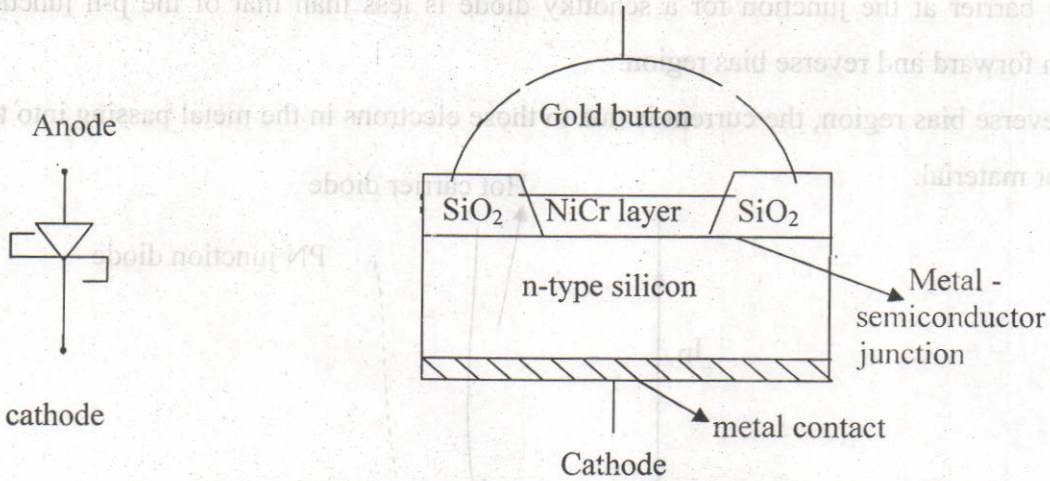

Fig.3.14 Schottky diode

Fig.3.14 shows a typical Schottky diode. The N-type silicon and a metal (such as Ni Cr) form the Schottky junction. The surface of the semiconductor is passivated (protected) by a layer of SiO_2 against outside contaminations. The semiconductor is a solid state diode in which the junction is formed by metal – semiconductor-contact. Thick gold wafer (called gold button due to its shape) acts as the anode and the semiconductor material acts as the cathode. These passivated Schottky diodes have small junction areas, have low junction capacitance and are suitable for operation up to 18GHZ.($18 \times 10^9 H_Z$); they have rapid switching capability.

3.4.1 OPERATION

In metal as well as semiconductor, the electron is the majority carrier. But the level of minority carriers (holes) in the metal is insignificant. When the materials are joined, the electron in the lightly doped n-type silicon semiconductor material establishes a heavy flow of majority carriers (these injected carriers have high K.E compared to the electrons of the metal and hence they are called "hot carriers") The heavy flow of electrons into the metal creates a region near

the junction surface depleted of carriers in the silicon. The additional carriers in the metal establish a "negative wall" in the metal. This results in a "surface barrier" between two materials, preventing any further current.

When the diode is forward biased, the positive potential attracts the electrons and reduces the strength of the negative barrier. This results in a heavy flow of electrons across the junction. The barrier at the junction for a schottky diode is less than that of the p-n junction device in both forward and reverse bias region.

In the reverse bias region, the current is due to those electrons in the metal passing into the semiconductor material.

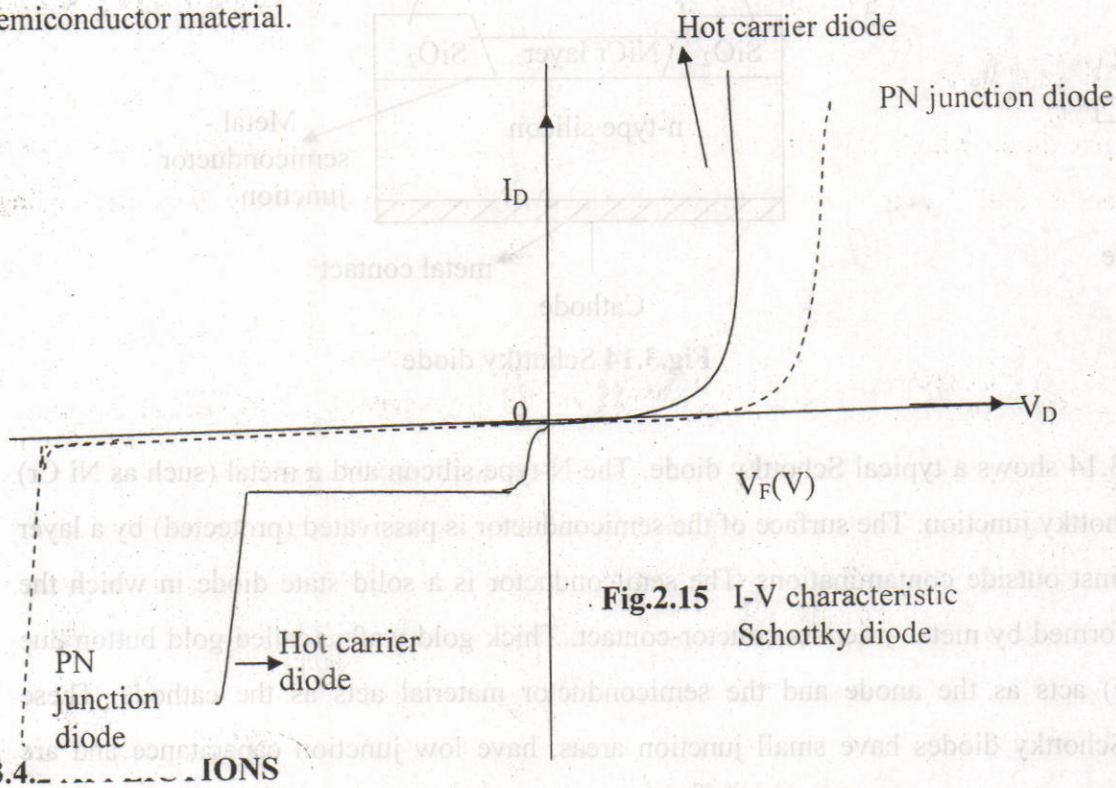

Fig.2.15 I-V characteristic Schottky diode

3.4 APPLICATIONS

(1) It can be used to rectify signals of frequencies exceeding 300KHZ.

(2) It is used in clipping and clapping circuits.

(3) It is used in mixing and detecting networks used in communication systems.

(4) In radar systems.

(5) Schottky TTL logic for computers

3.5 SUMMARY

The reverse biased diode can exhibit the properties of a capacitor. The capacitance can be varied with applied reverse voltage. Such a property is used in varactor diode. These diodes are used for

tuning purpose. If doping concentration is increased the depletion region may become thin, such a diode can be used a voltage regulator (Zener diode).

If doping density is further increased 1 out of 10^3 atoms, the depletion region may became extremely thin allowing the charge carriers to penetrate the junction barrier, This tunnel diode can be used as an ultra fast switch. Even a metal-semiconductor junction can work as a diode, known as Schottky diode. This diode has lower cut-in voltage compared to ordinary diodes. Hence they can be used in low power logic integrated circuits as they consume

SOLVED NUMERICAL PROBLEMS

Example (1)

A 15V Zener diode which can dissipate maximum power 0.5W is connected in series with a resistor R across a 40V supply. Find the minimum value of R that prevents the diode from being destroyed.

Solution:

Given $V_Z = 15V = V_0$; $P_{MAX} = 0.5W$

To find : R_{MIN} = ?

We can write $V_{IN} = V_0 + IR_{MIN}$

$$\text{Or } R_{MIN} = \frac{V_{IN} - V_O}{I}$$

But $V_Z I = 0.5$

$$\therefore I = \frac{0.5}{15V} = \frac{1}{30} A$$

$$\therefore R_{MIN} = \frac{40 - 15}{\frac{1}{30}} = 25 \times 30 = 750\Omega$$

Example (2)

A 10V Zener diode along with a series resistance is connected across a 40V supply. Calculate the minimum value of resistance required; if the maximum Zener current is 50mA.

Solution:

Given: $V_{IN} = 40V$; $I_Z = 50mA$; $V_O = V_Z = 10V$;

To find: R = ?

$I = I_L + I_Z = 0 + 50mA = 50mA.$

$\therefore$ I is maximum, the minimum value of R is

$$R = \frac{V - V_O}{I} = \frac{40 - 10}{50 \times 10^{-3}} = 600\Omega.$$

Example (3)

Calculate the transition capacitance of a Si pn junction of cross sectional area $0.1mm^2$, if the thickness of the depletion region is 0.5 micron.

Solution:

Given: $\varepsilon_o = 8.85x10^{-12}$ F/m; K for Si = 12 ;

To find: C_T = ?

Transition capacitance

$$C_T = \frac{\varepsilon A}{\omega}$$

$\varepsilon = K\varepsilon_o = 12x8.85x10^{-12}$ $A = 0.01mm^2 = 1x10^{-8}\,m^2$ $\omega = 0.5micron = 5x10^{-7}\,m$

$$C_T = \frac{8.85x10^{-12}\,x12x10^{-8}}{5x10^{-7}}$$

$$= 21.24x10^{-13}\,F$$

$$212.3pF$$

3.6 SELF ASSESSMENT QUESTIONS

(I) Long answer questions

1. Describe the construction and working of a Varactor diode. Draw its C-V characteristics and explain.
2. Explain the Zener breakdown mechanism. Draw its characteristics and explain. Mention its uses.

3. List the applications of Zener diode. Explain the action of Zener diode as a voltage regulator.

4. What is a tunnel diode? Explain the tunneling mechani w its I-V characteristics and explain.

5. Explain the construction, working and characteristics of metal-semi conductor diode.

(II) Short answer questions

1) List out the applications of Zener diode.
2) Draw the characteristics of metal semi conductor diode and explain.
3) Give an idea about diffusion and transition capacitances.
4) Explain the action of tunnel diode as an oscillator.
5) Draw the I-V characteristics of Zener diode and explain.
6) Explain how a Varactor diode is used for electronic tuning?
7) Discuss the tunneling mechanism in detail.
8) Explain the Zener breakdown mechanism.
9) Discuss the action of Zener diode as a regulator.

(III) Numerical problems

1) A Zener diode has a breakdown voltage of 9.1V with a maximum power dissipation Of 364 mW. What is the maximum current the diode can handle?

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UNIT-II **LESSON-4**

SEMICONDUCTOR DEVICES-III

OBJECTIVES OF THE LESSON

This lesson explains you the concepts of a transistor, types, working, current amplification factors, their interrelationships, various modes of connection of a transistor in a circuit, experimental determination of characteristics. It also explains qualitatively the characteristics and their use.

STRUCTURE OF THE LESSON

INTRODUCTION

The term transistor was derived by contracting the words '*TRANSFER*' and '*RESISTOR*'. The invention and the development of first transistor was done by the three scientists namely John Bardeen, Walter Brattain and William Shockley in 1948. The prefix "Trans" means the signal transfer property of the device while "istor" classifies it as a solid element in the same family with resistors.

A Transistor is a single semiconductor crystal which contains two P-N junctions formed back-to-back. It has three sections of doped semiconductors, named emitter, base and collector. The section of one side that supplies charge carriers (electrons or holes) is called the *Emitter*. It is heavily doped so that it can inject a large number of charge carriers into the base region and then on to the collector. The section on the other side that collects the carriers is called the *Collector*. It is very lightly doped. The middle section which forms two P-N junctions between emitter and collector is called the *Base*. The base is also very lightly doped. A transistor may be either of PNP or NPN type as shown below in Fig. 4.1 and Fig. 4.2.

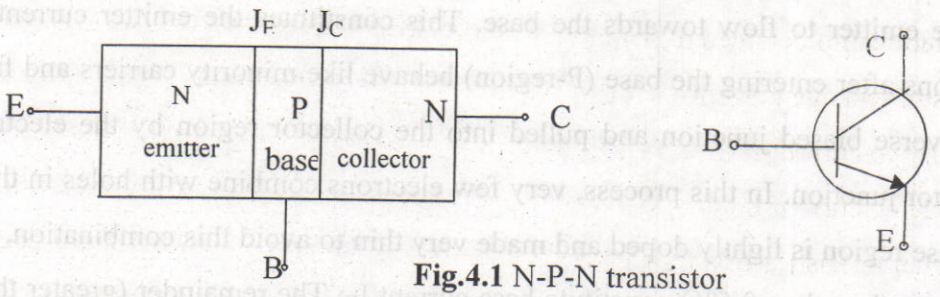

Fig.4.1 N-P-N transistor

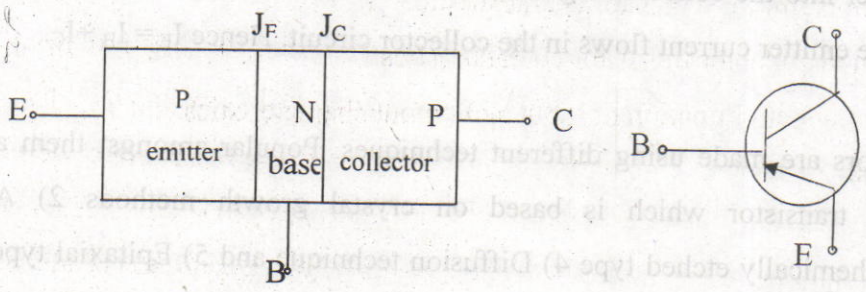

Fig.4.2 P-N-P transistor

In a PNP transistor, the arrow on the emitter lead points towards the base, because when the emitter base junction (J_E) of a transistor is forward biased, the direction of the conventional emitter circuit is towards the base. For an NPN transistor, the arrow on the emitter lead points away from the base, because the emitter-base junction is forward biased, the direction of the conventional emitter current in this case is out of the emitter. The emitter lead in both the types is always the one with the arrow. If the arrow is Not Pointing iN, the transistor is an NPN type, otherwise it is PNP type. Arrow on emitter always indicates the direction of the conventional current.

The transistor is a ***bipolar device*** because both holes and electrons will take part in the current flow through the device. The N-type region contains excess free electrons which are negative carriers. The P-type region contains free holes which are positive charge carriers. Two (bi) polarities of carriers are present. Also there are two PN junctions in the transistor. Hence it is called ***Bipolar Junction Transistor*** (BJT).

Working of an NPN transistor

Fig.3.3 shows an NPN transistor with emitter-base junction forward biased and collector-base junction reverse biased. The forward bias causes the electrons in the N-type emitter to flow towards the base. This constitutes the emitter current I_E. These electrons after entering the base (P-region) behave like minority carriers and fall through the reverse biased junction and pulled into the collector region by the electric field of collector junction. In this process, very few electrons combine with holes in the base. As the base region is lightly doped and made very thin to avoid this combination, only a few electrons (less than 0.5%) constitute base current I_B. The remainder (greater than 99.5%) cross over into the collector region to constitute collector current I_C. In this way, almost the entire emitter current flows in the collector circuit. Hence $I_E = I_B + I_C$.

Transistors are made using different techniques. Popular amongst them are: 1) Grown junction transistor which is based on crystal growth methods 2) Alloy type 3) Electrochemically etched type 4) Diffusion technique and 5) Epitaxial type. Whatever is the fabrication method, the basic principle of working is same and in this lesson, we refer to transistor with grown junction.

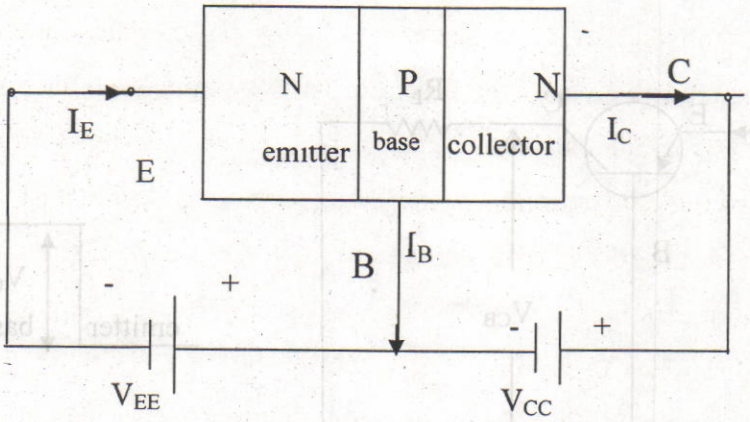

Fig.4.3 Biasing an NPN - transistor

Working of PNP transistor

Fig.4.4 shows PNP transistor with emitter-base junction forward biased and collector-base junction reverse biased. The forward bias causes the holes in the P-type emitter to flow towards the base. This constitutes the emitter current I_E. These holes when flowing through the base tend to combine with electrons in the base. As the base is lightly doped and thin, only a few holes (less than 0.5%) combine with the electrons. The remainder (greater than 99.5%) cross over into the collector region to constitute collector current I_C. In this way, almost the entire emitter current flow in the collector circuit. Hence $I_E = I_B + I_C$.

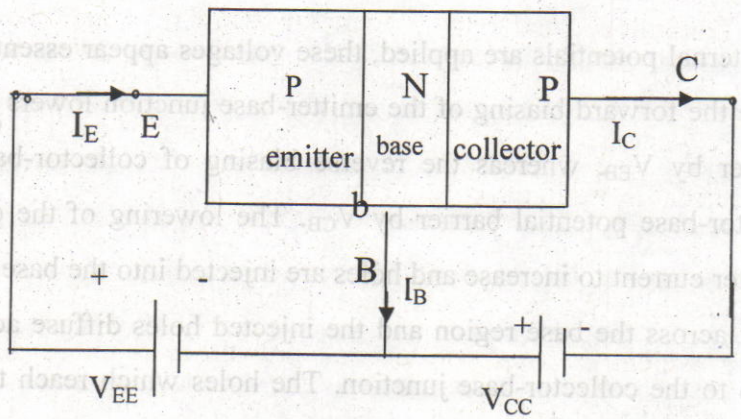

Fig.4.4 Biasing PNP transistor

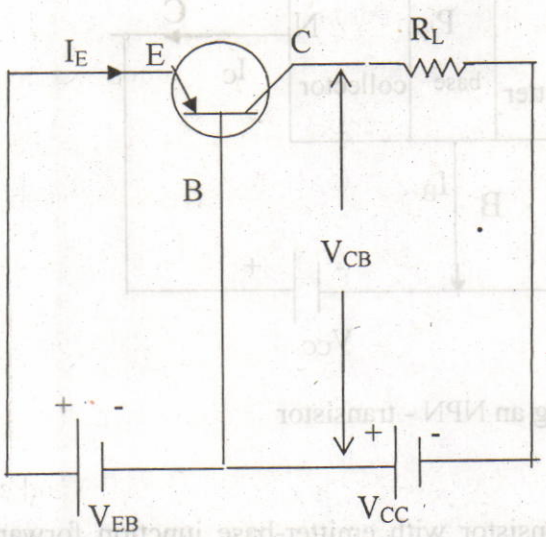

Fig.4.5 PNP transistor with biasing voltages

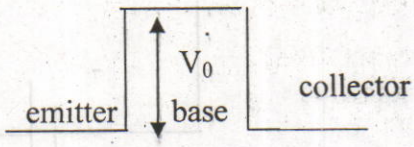

Fig.4.6 Potential barrier at one junction of transistor (unbiased)

4.2. POTENTIAL DISTRIBUTION THROUGH A TRANSISTOR

In Fig.4.5, PNP transistor is shown with voltage sources to bias emitter-base and collector-base junctions. The dashed curve applies to the case before the application of external biasing voltages. The solid curve to the case after the biasing voltages is applied. In the absence of applied voltage, the potential barriers at the junctions adjust themselves to the height V_o required so that no current flows across each junction.

If now external potentials are applied, these voltages appear essentially across the junctions. Hence the forward biasing of the emitter-base junction lowers the emitter-base potential barrier by V_{EB}, whereas the reverse biasing of collector-base junction increases the collector-base potential barrier by V_{CB}. The lowering of the emitter-base barrier permits emitter current to increase and holes are injected into the base region. The potential is constant across the base region and the injected holes diffuse across the N-type material (base) to the collector-base junction. The holes which reach this junction being minority carriers in base region, see a potential well instead of a hill and fall down. These are collected by the collector.

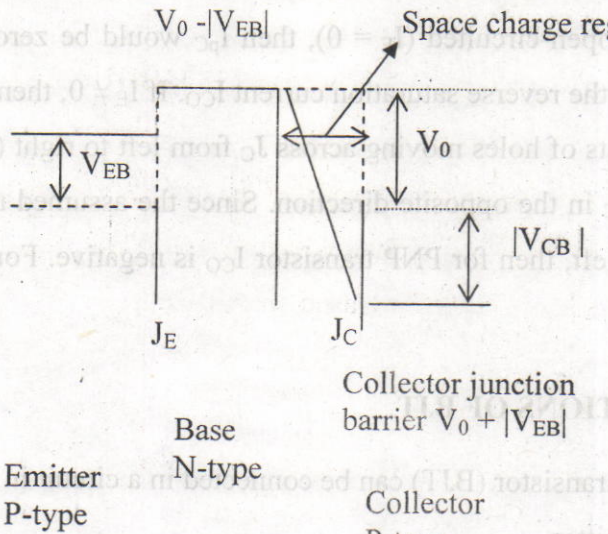

Fig.4.7 Potential variation in a transistor under biased conditions

4.3 TRANSISTOR CURRENT COMPONENTS

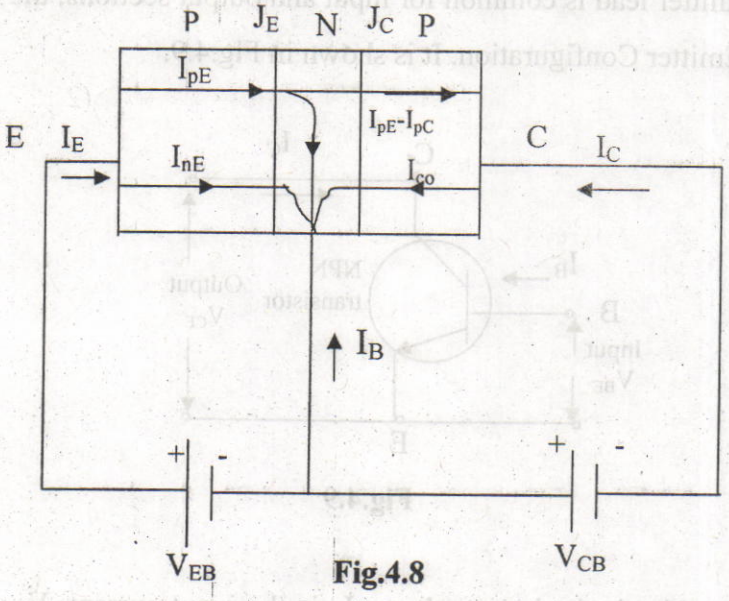

Fig.4.8

In Fig.4.8, the emitter current I_E consists of hole current I_{pE} (holes crossing from emitter into base) and electron current I_{nE} (electrons crossing from base into the emitter). Due to recombination of some holes with electrons in base region, all holes

crossing the emitter junction J_E can not reach the collector junction J_C. If I_{pC} is the hole current at J_C, then the recombination current leaving the base is $(I_{pE}-I_{pC})$.

If the emitter were open-circuited ($I_E = 0$), then I_{pC} would be zero. Hence the collector current would equal the reverse saturation current I_{CO}. If $I_E \neq 0$, then $I_C = I_{CO}-I_{pC}$. For PNP transistor, I_{CO} consists of holes moving across J_C from left to right (base to collector) and electrons crossing J_C in the opposite direction. Since the assumed reference direction for I_{CO} is from right to left, then for PNP transistor I_{CO} is negative. For an NPN transistor, it is positive.

4.4. CONFIGURATIONS OF BJT

A Bipolar junction transistor (BJT) can be connected in a circuit in three ways:

(i) Common Emitter

(ii) Common Base

(iii) Common Collector

i) **Common Emitter** configuration (CE)

When the emitter lead is common for input and output sections, the configuration is called Common Emitter Configuration. It is shown in Fig.4.9.

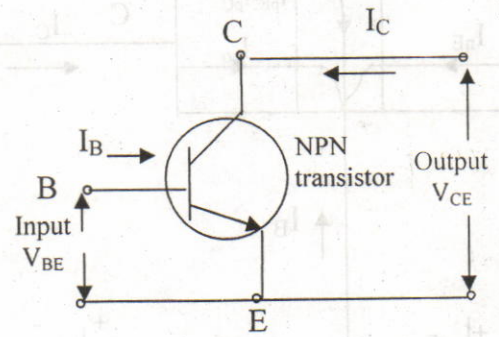

Fig.4.9

In this configuration, V_{BE} is the input voltage, I_B is the input current, V_{CE} is the output voltage and I_C is the output current. It is a convention to indicate the common terminal in place of second subscript for voltage representation. Ex: V_{CE}, V_{BE}.

(ii) **Common Base** configuration (CB)

When the base lead is common for input and output sections, the configuration is called Common Base Configuration. It is shown in Fig.4.10.

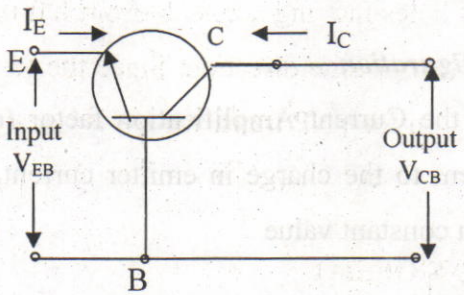

Fig.4.1

In this configuration, V_{EB} is the input voltage, I_E is the input current, V_{CB} is the output voltage and I_C is the output current.

(iii) **Common Collector** configuration (CC)

When the collector lead is common for input and output sections, the configuration is called Common Collector Configuration. It is shown in Fig.4.11.

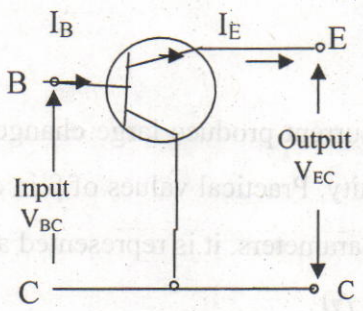

Fig 4.11

In this configuration, V_{BC} is input voltage, I_B is the input current, V_{EC} is the output voltage and I_E is the output current.

4.5. CURRENT AMPLICATION FACTORS

Transistor is basically a current amplifying device. Hence it posses different current amplification factors in various configurations.

(i) ***Common Base Configuration***

In CB mode, the Current Amplification factor (α) is defined as the ratio of charge in collector current to the charge in emitter current, when the collector to base voltage is maintained at a constant value

$$\alpha = \left[\frac{\delta I_C}{\delta I_E}\right]_{V_{CB}}$$

Since the collector current is slightly less than the emitter current, α is slightly less than unity. Practical values of α in commercial transistors lie between 0.95 and 0.995. In terms of h-parameters, it is h_{fb}.

(ii) ***Common Emitter Configuration***

The current amplification factor (β) in CE mode is defined as the ratio of change in collector current to the change in the base current, when the collector to emitter voltage is maintained at a constant value.

$$\beta = \left[\frac{\delta I_C}{\delta I_B}\right]_{V_{CE}}$$

Since small changes in base current produce large changes in collector current, the value of β is always greater than unity. Practical values of β in commercial transistors lie between 20 and 500. In terms of h-parameters, it is represented as h_{fe}.

(iii) Common Collector Configuration (γ)

The current amplication factor γ in CC mode is defined as the ratio of change in emitter current to the change in base current when the emitter to collector voltage is maintained at a constant value.

$$\gamma = \left[\frac{\delta I_E}{\delta I_B}\right]_{V_{EC}} = \left[\frac{\delta I_B + \delta I_C}{\delta I_B}\right]_{V_{EC}} = 1+\beta$$

The value of γ is always greater than 1 because δI_E is greater than δI_B.

4.5.1 RELATIONSHIP BETWEEN α, β, γ

α, β and γ are characteristics of a particular transistor. Hence, they are related to each other through some relations. In a transistor, emitter current is related to collector current and base current as follows.

i.e. $I_E = I_B + I_C$

For small changes in currents, we have

$$\delta I_E = \delta I_B + \delta I_C \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.5.1)$$

Dividing throughout by δI_C, we get

$$\frac{\delta I_E}{\delta I_C} = \frac{\delta I_B}{\delta I_C} + \frac{\delta I_C}{\delta I_C}$$

or $\quad \frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad \left(\because \frac{\delta I_C}{\delta I_E} = \alpha \; ; \; \frac{\delta I_C}{\delta I_B} = \beta\right)$

or $\quad \frac{1}{\alpha} = \frac{1+\beta}{\beta}$ or $\alpha = \frac{\beta}{1+\beta}$ .....(4.5.2)

or $\quad \alpha + \alpha\beta = \beta$ or $\gamma = 1 + \beta = \frac{\beta}{\alpha}$ -------- (4.5.3)

or $\quad \alpha = \beta(1-\alpha)$

or $\quad \beta = \frac{\alpha}{1-\alpha}$ .....(4.5.4)

4.6. TRANSISTOR LEAKAGE CURRENTS

When the emitter-base junction is forward biased and collector-base junction is reverse biased, whole of emitter current does not reach the collector. Part of it is converted as base current. Since base-collector junction is reverse biased, a small current also flows due to minority carriers. It is known as ***Transistor Leakage current***. The two types of leakage currents are explained below.

4.6.1 Leakage current I_{CBO}

It is the current that flows in the reverse biased collector-base junction, with emitter lead open in CB configuration. It is shown in Fig.4.12.

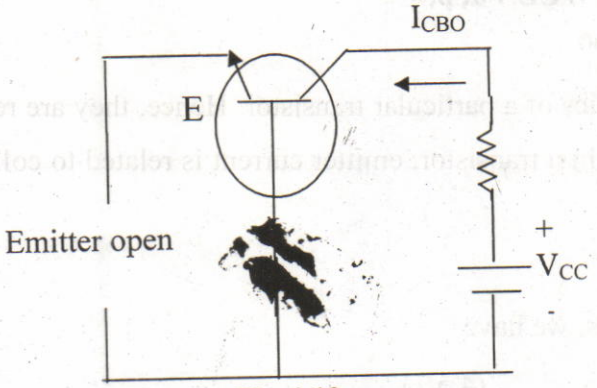

Fig.4.12

In CB configuration, with emitter open, the collector current is made of two parts.

(i) Part of emitter current, which reaches collector i.e. αI_E

(ii) Collector to base leakage current I_{CBO}.

Thus $I_C = \alpha I_E + I_{CBO}$

In I_{CBO}, the subscript 'O' indicates the third lead status. i.e., the emitter lead is open.

4.6.2 LEAKAGE CURRENT I_{CEO}

I_{CEO} is the current that flows through the emitter in CE configuration with base lead open. It is shown in Fig.4.13.

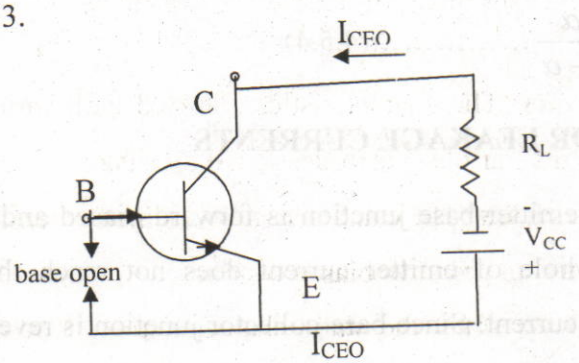

Fig.4.13

In a transistor,

$$I_E = I_B + I_C \quad \text{.....(4.6.2.1)}$$

$$\text{But } I_C = \alpha I_E + I_{CBO} \quad \text{.....(4.6.2.2)}$$

Here I_{CBO} is the leakage current that flows in the reverse biased collector-base junction.

Now Eq.(4.6.2.2) becomes

$$I_C = \alpha (I_B + I_C) + I_{CBO}$$

$$I_C = \alpha\ I_B + \alpha\ I_C + I_{CBO}$$

or $I_C = (1-\alpha) = \alpha\ I_B + I_{CBO}$

or $$I_C = \frac{\alpha}{1-\alpha}(I_B) + \frac{1}{1-\alpha}(I_{CBO})$$

or $I_C = \beta\ I_B + (\beta+1)\ I_{CBO}$ .....(4.6.2.3)

If base is open, $I_B=0$ and $I_C = I_{CEO}$

Hence Eq.(3) becomes

$I_{CEO} = [\beta+1]\ I_{CBO}$ ....(4.6.2.4)

Thus in CE mode, the leakage current is $(1+\beta)$ times the leakage current in CB mode.

Hence Eq.(4.6.2.3) becomes,

$I_C = \beta I_B + I_{CEO}$ ..... (4.6.2.5)

4.7 STATIC CHARACTERISTICS OF A TRANSISTOR

The complete electrical behaviour of a transistor can be described by stating the interrelation of various currents and voltages. The relationships between voltages and currents can be conveniently displayed graphically and the curves thus obtained are known as the *Characteristics of a transistor*. The transistor characteristics can be either static or dynamic.

Static Characteristics: The characteristics obtained with variation in D.C. voltages and currents applied to the various electrodes of the transistor.

Dynamic Characteristics: The characteristics obtained when AC signal is applied to the input of the transistor, in properly biased condition.

In this lesson we study the static characteristics of transistor in CB, CE and CC configurations.

4.7.1. Common Base Transistor characteristics

Fig.4.14.shows the circuit of common Base NPN transistor. We describe the behaviour of transistor by the following two relations, which give the input voltage V_{EB} , output current I_C in terms of the output voltage V_{CB} and Input current I_E.

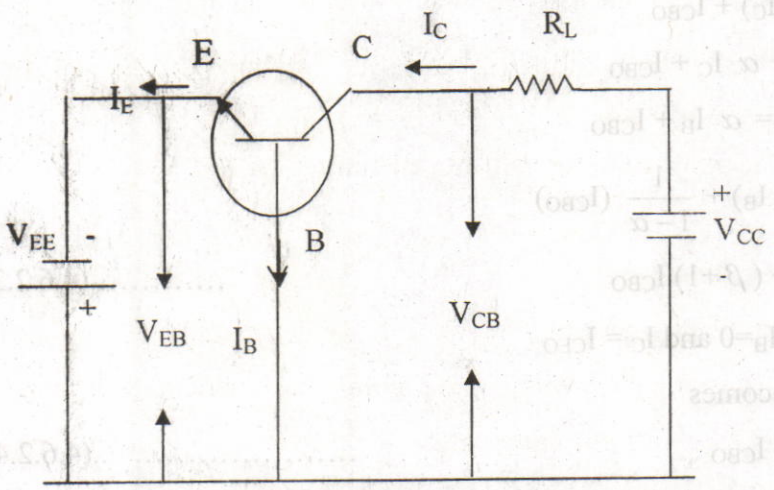

Fig 4.14

$$V_{EB} = f_1(V_{CB}, I_E) \quad \text{.....(4.7.1.1)}$$

$$I_C = f_2(V_{CB}, I_E) \quad \text{... (4.7.1.2)}$$

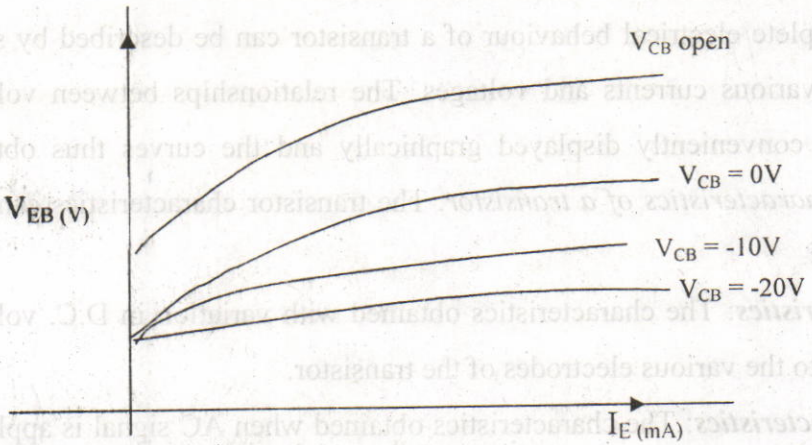

Fig.4.15 CB input Characteristics

The relation of Eq.(4.7.1.1) is given in Fig.4.15. Input characteristics are a plot of emitter current I_E verses Emitter to Base voltage V_{EB} with collector to base voltage V_{CB} as a parameter. These are known as *Input Static Characteristics* or *Emitter Static Characteristics*. Consider the fact that the transistor consists of two diodes placed in series "back-to-back". The Input characteristics represent the forward characteristics of

emitter-to-base diode for various collector voltages. An important feature of input characteristics is that there exists a *cutin* or *threshold* voltage below which the emitter current is very small. From the curves, we notice that an increase in magnitude of collector voltage will cause the emitter current I_E to increase, with V_{EB} held constant. Thus the curves shift downward as V_{CB} increases. The curve with the collector open represents the characteristic of the forward-biased emitter diode.

The Output Characteristics;

The relation of Eq.(4.7.1.2) is given in Fig.4.16. It is a plot of collector current I_C verses collector-to base voltage drop V_{CB}, with emitter current I_E as parameter. These curves are known as *Output* or *Collector Static Characteristics*. If $I_E = 0$, collector current $I_C = I_{CO}$. For other values of I_E, the collector junction diode reverse current is augmented by the fraction of the input diode forward current, which reaches the collector.

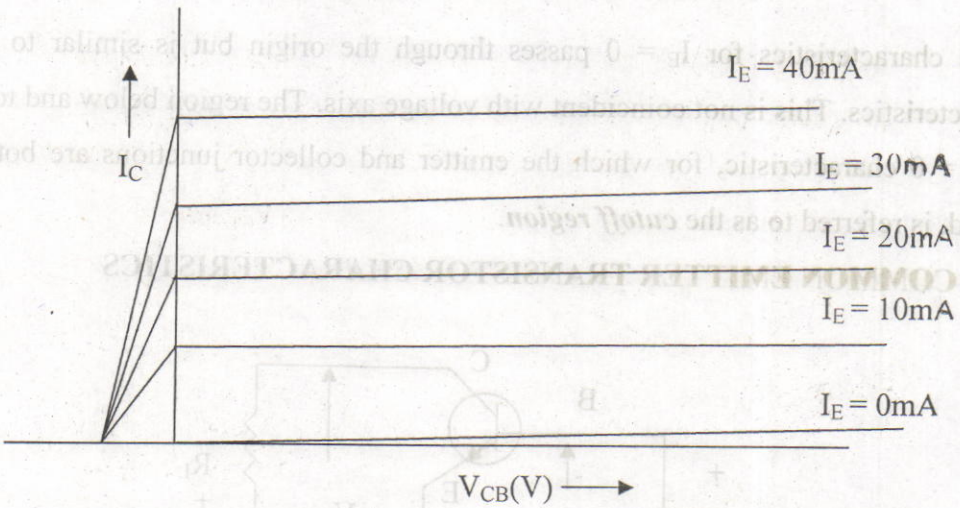

Fig 4.16 CB output characteristics

The output characteristics can be divided into three regions:

(1) ***ACTIVE REGION***

In this region, collector junction is biased in the reverse direction and emitter junction in the forward direction. If I_E = 0mA, I_C is small and equals the reverse saturation current I_{CO} (μA for Ge and nA for Si transistor) of the collector junction. Now, if $I_E \neq 0$, than a fraction αI_E of this current will reach the collector. In this region, I_C is

independent of collector voltage V_{CB} and depends only on emitter current I_E. As α is less than unity, I_C is less than I_E.

(2) ***SATURATION REGION***

The region to the left of the ordinate, $V_{CB} = 0$ and above the $I_E = 0$ characteristic, in which both emitter and collector junctions are forward biased is called ***Saturation Region***. Actually, V_{CB} is slightly positive in the region when $V_{CB} = 0V$. This forward biasing of collector accounts for large change in collector current with small changes in collector voltages. For a forward bias, I_C increases exponentially with voltage.

(3) ***CUT OFF REGION***

The characteristics for $I_E = 0$ passes through the origin but is similar to the other characteristics. This is not coincident with voltage axis. The region below and to the right of $I_E = 0$ characteristic, for which the emitter and collector junctions are both reverse biased, is referred to as the ***cutoff region***.

4.7.2 COMMON EMITTER TRANSISTOR CHARACTERISTICS

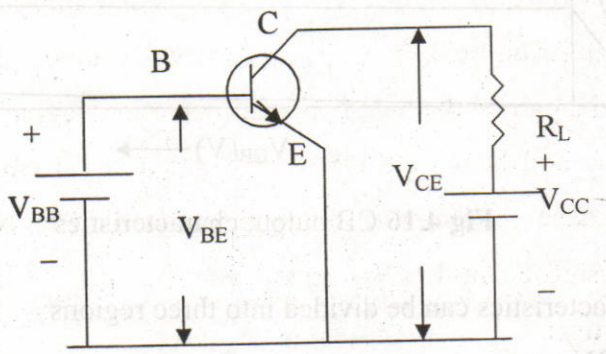

Fig 4.17

Fig 4.17 shows the circuit of common emitter NPN transistor. We describe the behaviour of the transistor by the following two relations, which give the input voltage V_{BE} and output current I_c of the output voltage V_{EE} and input current I_B.

$$V_{BE} = f_1(V_{CE}, I_B) \qquad \text{--------- (4.7.2.1)}$$

$$I_B = f_2(V_{CE}, I_B) \qquad \text{-------- (4.7.2.2)}$$

Input Characteristics

The relation of equation (4.7.2.1) is given in Fig.4.18. The input characteristics is a plot of base current I_B verses Base to emitter voltage to emitter voltage V_{CE} as a parameters. These are known as ***Input static characteristics*** or ***Base static characteristics***.

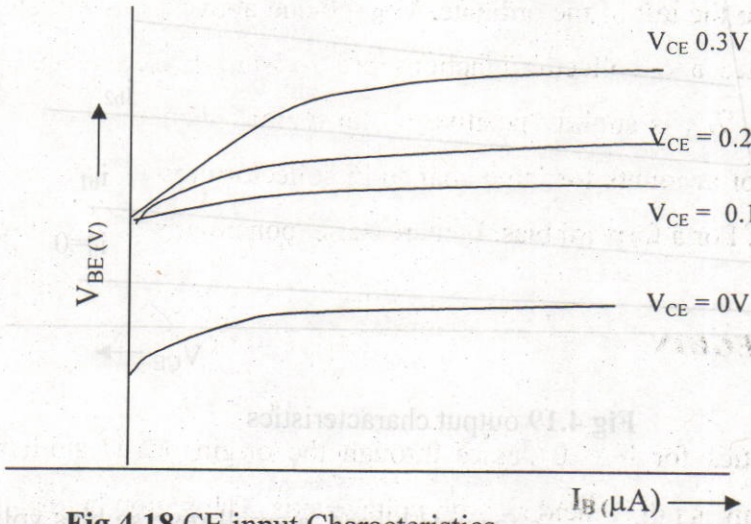

Fig 4.18 CE input Characteristics

Consider the fact that the transistor consists of two diodes placed in series "back – to-back" The input characteristics represent the forward characteristics of base to emitter diode for various collector voltages. When V_{CE} = 0 and the emitter-base junction is forward biased, the junction behaves as a forward biased diode. At a constant value of V_{BE}, when V_{CE} is increased, the width of the depletion region at the collector-base junction will increase and hence the effective width of the base will decrease. [Early effect]. The effect causes a decrease in the recombination current (base current I_B). Therefore the curves shift upward as V_{CE} increases.

Output Characteristics:

The relation of Eq.(4.7.2.2). is given in Fig.4.19. It is a plot of collector current I_C verses collector-to-emitter voltage V_{CE} with base current I_B as a parameter. These curves are known as ***Output*** or ***Collector Static Characteristics***.

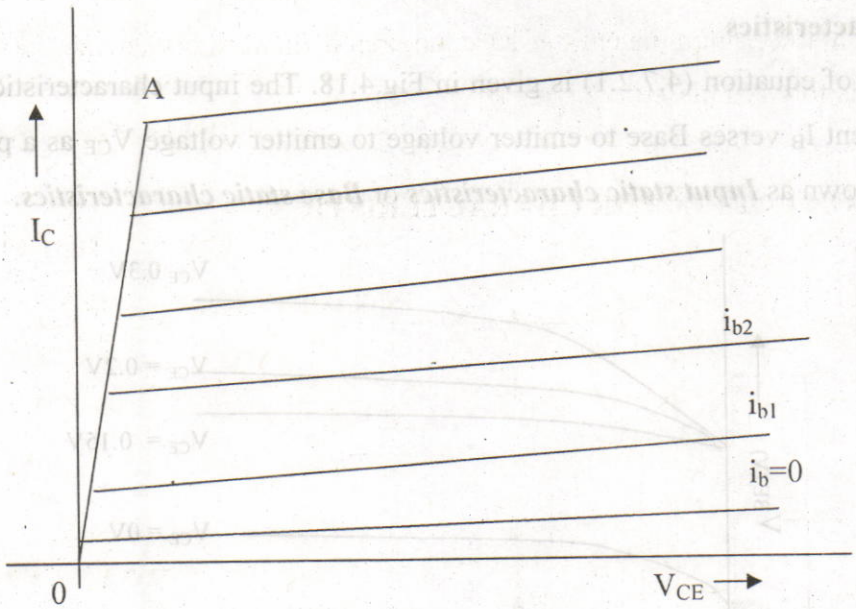

Fig 4.19 output characteristics

When the emitter-base jui 's forward biased, a small reverse bias voltage across the collector-base junction is sufficient to draw all the majority carriers from the emitter which diffuses into the base. But when V_{CE} is increased, the effective width of base will decrease. Hence the number of majority carriers from the emitter, recombining with the majority carriers in the base will decrease. This effect will slightly increase the value of I_C. This is the reason why the output characteristics are not horizontal but slope upward.

The output characteristics are divided into three regions.

(1) **SATURATION REGION**

The region of the curves to the left of the line OA is called the *Saturation region* and the line OA is called *Saturation line*. In this region, both junctions are forward biased. In this region, an increase in the base current does not causes the corresponding large change in I_C.

(2) ***CUT OFF REGION***

The region below the curve for $I_B=0$ is called the cutoff region. In this region both junctions are reverse biased and only leakage current flows.

(3) ACTIVE REGION

The central region where the curves are uniform in spacing and slope, is called the *active region*. In this region the emitter-base junction is forward biased and the collector-base junction is forward biased.

4.7.3. COMMON COLLECTOR CHARACTERISTICS:

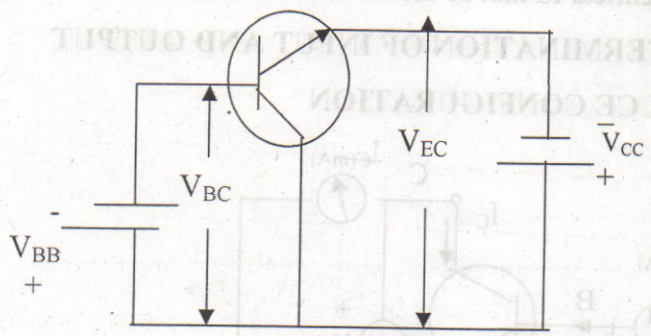

Fig 4.20

Fig.4.20.shows the circuit of common collector configuration, which is also called *Grounded collector* configuration. Here the base is the input terminal, the emitter is the output terminal and the collector is the common terminal.

We describe the behaviour of above transistor by the following two relations which give the input voltage V_{CB} and output current I_E in terms of the output voltage V_{CE} and input current I_B.

$$V_{CB} = f_1(V_{CE}, I_B) \quad \text{.....(4.7.3.1)}$$

$$I_E = f_2(V_{CE}, I_B) \quad \text{.....(4.7.3.2)}$$

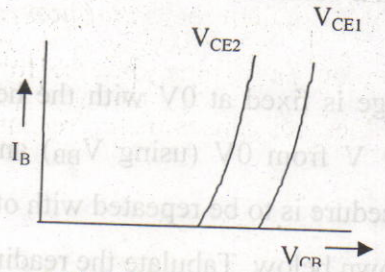

Fig.4.21 CC input characteristics

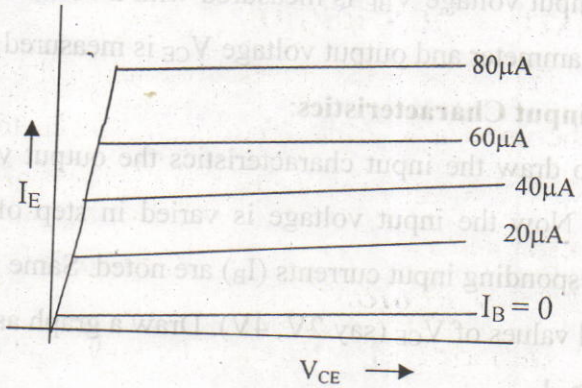

Fig.4.22 CC output characteristics

Relation (4.7.3.1) is plotted in Fig.4.21. It is a plot of V_{CB} verses I_B for different values of V_{CE} and is shown in Fig.4.21. It is quite different from those for CB or CE circuits. This difference is due to the fact that input voltage V_{CB} is largely determined by the value of V_{EE}. As V_{CB} is increased, V_{BE} is reduced, thereby reducing I_B.

The output characteristics are shown in Fig.4.22. Relation (4.7.3.2) is plotted in Fig.4.22. It is a plot of V_{CE} verses I_E for several fixed values of I_B. Since $I_C \cong I_E$, their characteristics are practically identical to that of the CE transistor circuit.

4.8. EXEPERIMENTAL DETERMINATION OF INPUT AND OUTPUT CHARACTERISTICS IN CE CONFIGURATION

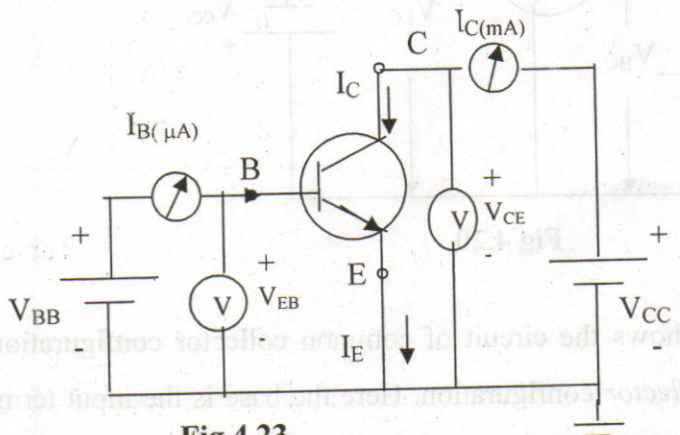

Fig.4.23

The input/output characteristics of a transistor (NPN) connected in CE configuration can be determined with the help of circuit shown in Fig.4.23. In the circuit, V_{BB}, V_{CC} are two power supplies used to bias the transistor. R_B is the base resistor used (of the order of tens or hundreds), to protect the base. In the input, I_B is measured with a micro ammeter and input voltage V_{BE} is measured with a voltmeter. In the output, I_C is measured with a milli ammeter and output voltage V_{CE} is measured with a voltmeter.

The input Characteristics:

To draw the input characteristics the output voltage is fixed at 0V with the help of V_{CC}. Now the input voltage is varied in step of 0.1 V from 0V (using V_{BB}) and the corresponding input currents (I_B) are noted. Same procedure is to be repeated with other fixed values of V_{CE} (say 2V, 4V). Draw a graph as shown below. Tabulate the readings in Table .1.

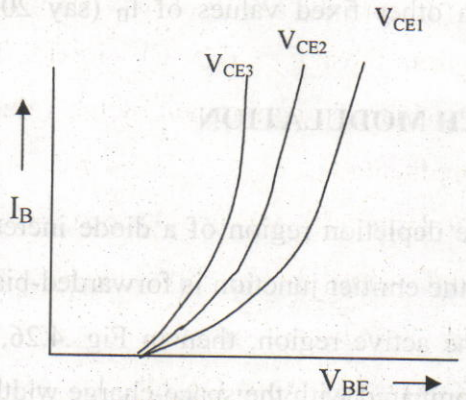

Fig.4.24

Table:1

S.No.	V_{BE}	V_{CE} = 0V	V_{CE} = 2V	V_{CE} = 4V
		I_B	I_B	I_B
1	0V			
2	0.1V			
3	0.2V			
4	0.3V			
5	0.4V			
6	0.5V			
7	0.6V			
8	0.7V			

The Output Characteristics

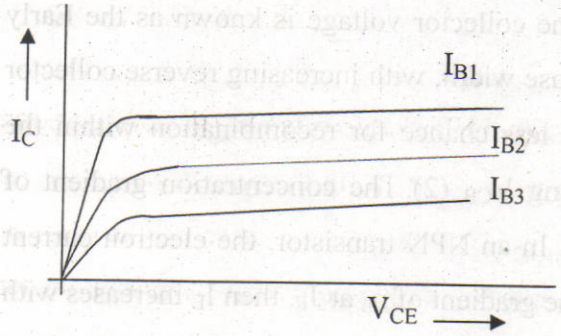

Fig.4.25

Table:2

S.No.	V_{CE}	I_B = 10μA	I_B = 20μA	I_B = 30μA
		I_C	I_C	I_C
1	0V			
2	1V			
3	2V			
4	3V			
5	4V			
6	5V			
7	6V			
8	7V			
9	8V			
10	9V			

To draw the output characteristics, input current I_B is fixed at some value say at 10μA) using V_{BB}. Now vary the output voltage (V_{CE}) with the help of power supply (V_{CC}) from 0V in steps of 1V and note the corresponding output current (I_C). Tabulate the reading in

Table.2. Same procedure is to be repeated with other fixed values of I_B (say 20μA, 30μA).Draw a graph as shown in Fig.4.25.

4.8.1. THE EARLY EFFECT OR BASE-WIDTH MODULATION

We know that the width W of the depletion region of a diode increases with the magnitude of the reverse voltage. Since the emitter junction is forwarded-biased but the collector junction is reverse-biased in the active region, then in Fig .4.26, the barrier width at emitter junction J_E is negligible compared with the space-charge width W at J_C.

The transition region at the junction is the region of uncovered charges on both sides of the junction at the positions occupied by the impurity atoms. As the voltage applied across the junction increases, the transition region penetrates deeper into the collector and base. Since the doping in the base is substantially smaller than that of collector, the per tration of the transition region into the base is much larger than into the collector. Hence the collector depletion region is neglected in Fig.4.26. If the metallurgical base width is W_B, then the effective electrical base width is $W_B' = W_B - W$. This modulation of effective base width by the collector voltage is known as the Early effect. The decrease is W_B' i.e. the effective base width, with increasing reverse collector voltage has three consequences: (1) There is less chance for recombination within the base region. Hence α increases with increasing V_{CB} (2) The concentration gradient of minority carriers is increased within the base. In an NPN transistor, the electron current injected across the emitter is proportional to the gradient of n_p at J_E, then I_E increases with increasing reverse collector voltage. (3). For extremely large voltages , the effective base width W_B' may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is known as ***Punch through***.

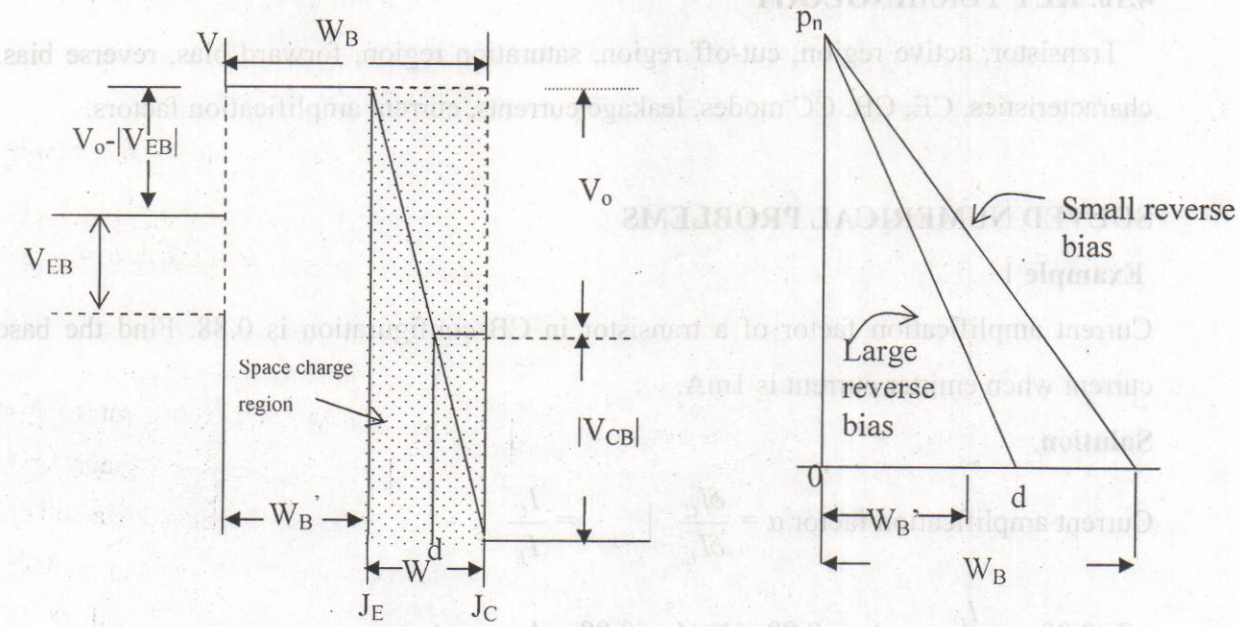

Fig 4.27 Early Effect in a transistor under biased conditions

4.9. SUMMARY

Transistor is a semiconductor device, which has the capacity to amplify electrical signals. It is a bipolar device because both types of charge carriers (electrons and holes) will take part in conduction mechanism. Transistor may be either PNP or NPN type. It has the signal transfer property from forward biased low resistance emitter region to reverse biased high resistance collector region. It can operate in three modes: Common Emitter (CE), Common Base (CB), and Common Collector (CC). CE mode is the most used mode. Transistor is a current amplifying device. Transistor possess current amplification factor, 'α' in CB, 'β' in CE and 'γ' in CC modes. α is less than unity, β and γ values are grater than unity. Transistor input characteristics are similar to forward bias characteristics of a diode. Output characteristics of CE, CB can be divided into three regions, namely active, cut-off and saturation regions. Transistor when biased in the active region, can act as an amplifier. Using the transistor characteristics, one can determine the parameters of the transistor.

4.10. KEY TERMINOLOGY

Transistor, active region, cut-off region, saturation region, forward bias, reverse bias, characteristics, CE, CB, CC modes, leakage currents, current amplification factors.

SOLVED NUMERICAL PROBLEMS

Example 1

Current amplification factor of a transistor in CB configuration is 0.88. Find the base current when emitter current is 1mA.

Solution:

Current amplification factor $\alpha = \frac{\delta I_C}{\delta I_E}\Big|_{V_{CE}} = \frac{I_C}{I_E}$

Or $0.88 = \frac{I_C}{1mA} \rightarrow I_C = 0.88 \times 1mA = 0.88\ mA$

But $I_B = I_E - I_C = 1mA - 0.88\ mA$

$= 0.12\ mA$

Example 2

For a transistor, $\alpha = 0.95$, $I_{CO} = 10\mu A$. If emitter current is 5mA, find collector and base currents.

Solution:

Collector Current $I_C = \alpha I_E + I_{CO}$

$I_C = (0.95 \times 5mA) + 10\ \mu A$

$= 4.76mA$

$I_B = I_C - I_C = 5\ mA - 4.76\ mA = 0.24\ mA = 240\ \mu A$

Example 3

A transistor has $I_{CBO} = 48nA$; $\alpha = 0.992$. Find (1).β, I_{CEO} (2). Collector current when $I_B = 20\mu A$.

Solution:

Given $I_{CBO} = 48nA = 48 \times 10^{-9}A$; $\alpha = 0.992$

1) $\beta = \frac{\alpha}{1-\alpha} = \frac{0.992}{1-0.992} = \frac{0.992}{0.008} = 124$

$I_{CEO} = (\beta = +1)\, I_{CBO} = (1+124) \times 48 \times 10^{-9}$

$= 6000 \times 10^{-9} = 6\ \mu A$

2) Base Current, $I_B = 20\mu A$

$\therefore I_C = \beta I_B + (1+\beta) I_{CBO}$

$= 124 \times 20 \times 10^{-6} + 125 \times 48 \times 10^{-9}$

$= 2480\ \mu A + 6000 \times 10^{-9}\ A$

$= 2480\ \mu A + 6\ \mu A = 2486\ \mu A = 2.486 mA$

Example 4

In a transistor, the base current is 0.08 mA and the emitter current is 9.6mA. Find

(a) Collector current (b) α (c) β

Solution:

Given $I_B = 0.08mA$; $I_E = 9.6mA$

In a transistor $I_E = I_C + I_B$

Collector current $I_C = I_E - I_B$

$= 9.6 - 0.08$

$= 9.52mA$

$\alpha = \frac{I_C}{I_E} = \frac{9.52mA}{9.60mA} = 0.99$

$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-099} = \frac{0.99}{0.01} = 99$

Example *5*

In a transistor circuit, when base current is increased by 50 μA, keeping collector voltage fixed at 2V, the collector current is increased by 1mA. Calculate the current amplification factor of the transistor.

Solution:

This problem is related to CE configuration because collector voltage is fixed. Hence

$\beta = \left(\frac{\delta I_C}{\delta I_B} \right)_{V_{CE}} = \frac{1 \times 10^{-3}}{50 \times 10^{-6}} = \frac{1000}{50} = 20$

$\beta = 20$

4.11 SELF ASSESSMENT QUESTIONS

I. Long Answer Questions

1. Draw the input / output characteristics of a PNP transistor in CB configuration and explain the nature qualitatively.
2. Draw the input/output characteristics of an NPN / PNP transistor in CE configuration and explain their nature qualitatively.
3. Discuss the input and output characteristics of CE transistor and also explain the Cut-off, active and saturation regions.
4. Draw the circuit diagram of CE transistor to draw the input / output characteristics and explain the method . Draw the curves.
5. Explain the working of NPN and PNP transistors.

II. SHORT ANSWER QUESTIONS

1. Give an idea about potential distribution through a transistor.
2. Discuss the current components of a transistor with the help of a diagram.
3. Define α, β and obtain a relationship between them.
4. Draw the input and output characteristics of a CE transistor and mark the cut-off, active and saturation regions.
5. What is an early effect? Explain.
6. What are I_{CBO}, I_{CEO}? How they are related.
7. Draw the circuit diagram of CC transistor amplifier.
8. Explain the working of a PNP transistor.

III. NUMERICAL PROBLEMS:

1. The 'α ' of a transistor is 0.9. What would be the change in collector current corresponding to a change of 0.4 mA in the base current in a Common emitter arrangement. [Ans:3.6mA]
2. The current gain of a transistor in CE circuit is 49. Calculate its common base current gain. Find the base current when emitter current is 3 mA [Ans; $\alpha = 0.98$, $I_B = 0.06A$]
3. In a transistor circuit, $I_E = 3mA$, the leakage current $I_{CBO} = 5\mu A$. If $\alpha = 0.95$, find the collector and base currents. [Ans; $I_C = 2.855mA$, $I_B = 145\mu A$]

4. In a transistor, I_E is 1.01 times as large as the collector current. If the emitter current is 12.12 mA, find the base current. [Ans; I_B =0.12mA]

4.12. REFERENCES

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2. Integrated Electronics - Millman and Halkias, (TMH)
3. Electronic Devices and Circuits- Allen Mottershed, (PHI)
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TRANSISTOR BIASING

OBJECTIVES OF THE LESSON

This lesson explains the concept of bias, necessity of bias, stabilization of operating point, stabilization factor, various methods of biasing, their advantages and disadvantages, thermal runway. This lesson also explains how thermal stability of a transistor is achieved, the concept of load line analysis of an amplifier, types of load lines, operating point.

STRUCTURE OF THE LESSON

5.1 INTRODUCTION

From transistor characteristics, it is clear that the transistor functions most linearly when it is constrained to operate in its active region. To keep the transistor always to operate in active region, it is necessary to provide appropriate D.C potentials and currents, using external sources. Biasing means supplying D.C potentials and currents. The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of signal. This can be achieved with a D.C power supply or voltage cells and / or associating circuit with a transistor. The circuit which provides transistor biasing is known as *Biasing Circuit*. If we intend to amplify the signal with minimum possible distortion, we select Class A operation. If we are interested in power amplification we have to use Class AB or Class B operation. For tuned power amplifiers, Class C operation is preferred. Depending on the type of operation we need, biasing circuit changes. In this lesson, we concentrate on biasing circuits for Class-A operation wherein signal output current flows in the load for 360^0 swing of the AC input signal. Transistor biasing is very essential for the proper operation of transistor in any circuit.

Zero signal Operating Point: The biasing DC current and voltage determine a point on the output characteristic. The output signal swing occurs around this point. A load line whose slope is $1/R_L$ is drawn such that it passes through this operating point. It is also called *Quiescent point* or *Working point*.

Stabilization: The process of making zero signal operating point independent of temperature changes or variation in transistor parameters is known as *Stabilization*.

5.2 NEED FOR STABILIZATION

Fixing of a suitable operating point is not only sufficient but it must also be ensured that it remains where it was fixed. But in transistor circuits, the Q- point shifts with the use of the circuit. Such a shift of operating point may drive the transistor into an undesirable region. The amplifier becomes inefficient and useless. There are two reasons for the Q - point to shift: (i) Transistor parameters are temperature dependent (ii) The parameters change from transistor to transistor.

5.3 THERMAL RUNAWAY

Definition: The self destruction of an unstabilized transistor is known as ***Thermal Runway***.

Explanation:

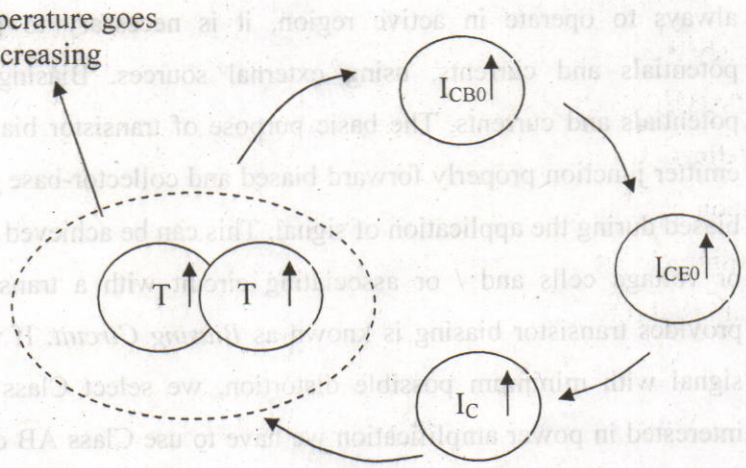

Fig.5.1 Thermal runaway

In a common emitter transistor circuit, the collector current is given by the following expression

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$

where β ------- current amplification factor.

I_{CBO} ---- reverse saturation current or leakage current.

I_B ------- base current.

We know that the reverse saturation current I_{CBO} doubles for every 10^0C rise of temperature. The flow of collector current produces heat which causes the collector junction temperature to rise. This in turn increases I_{CBO}. Hence I_C will increase according to the above equation. This may further increase the junction temperature and consequently I_{CBO}. If these successions of events are allowed to continue, soon I_C will increase beyond the safe operating value. In this situation, the transistor permanently damaged. This phenomenon is known as *Thermal Runaway*.

Condition to avoid thermal Runaway: If thermal runaway is to be avoided, the following condition is to be satisfied while using a transistor.

" The rate at which heat is released at the collector junction must not exceed the rate at which heat can be dissipated".

$$\frac{\partial P_C}{\partial T_J} < \frac{\partial P_D}{\partial T_J}$$

where ,

P_C---- heat released at collector junction

P_D---- power dissipation in Watts

T_J----- junction temperature

To satisfy the condition, the power transistors are fitted with heat sinks.

5.4 STABILITY FACTOR (S)

It is defined as the ratio of change of collector current I_C with respect to the reverse saturation current I_{CBO} with V_{BE} and β held constant. This factor is used to compare the biasing circuits. The larger the value of S, the more likely is the circuit to exhibit thermal instability.

$$S = \left[\frac{\partial I_C}{\partial I_{CBo}} \right]_{V_{BE},\beta}$$

Derivation for 'S'

In the active region of transistor characteristics, the basic relationship between I_C and I_B is given by

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$

Differentiating w.r.t I_C, we get

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (\beta+1) \frac{\partial I_{CBO}}{\partial I_C}$$

$$= \beta \frac{\partial I_B}{\partial I_C} + (\beta+1) \frac{1}{S}$$

Or $$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

..... 5.4.1

In order to calculate the factor S, for any biasing circuit, it is only necessary to find the relationship between I_B and I_C and to use Eq. (5.4.1).

5.5 BIASING CIRCUITS AND ANALYSIS

Providing appropriate DC potentials and currents using external sources is termed as Biasing and the potential applied is known as Bias. The circuits which

provide DC potentials and currents are known as Biasing circuits. Various biasing circuits are:

(i) Fixed bias (ii) Collector-to-base bias (iii) Self bias

5.5.1 Fixed bias [Base Bias]

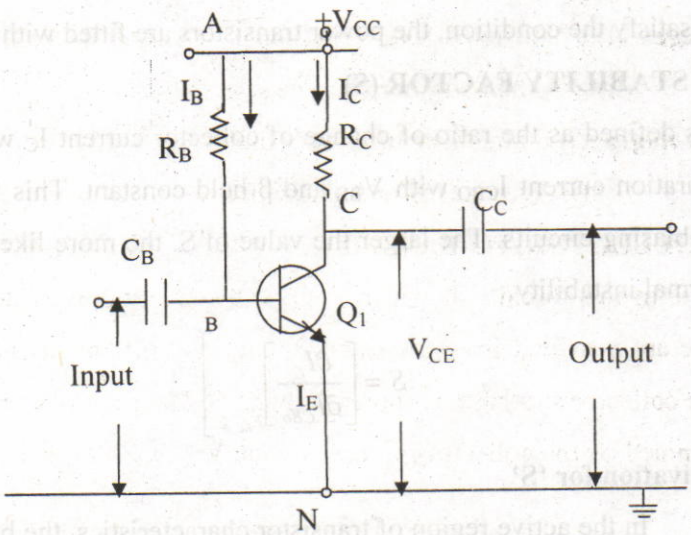

Fig 5.2 Fixed bias circuit

Fig 5.2 shows the circuit of fixed bias. In the circuit, the DC power supply voltages for the collector and base are applied from the same source. A high resistance R_B is connected between the base and supply. Since I_B is constant, when the values of V_{CC} and R_B are constant. Hence the circuit is called a ***Fixed Bias Circuit***.

Analysis

The zero signal collector current = I_C

The required base current under zero signal condition = $I_B = \frac{I_C}{\beta}$

Supply voltage = V_{CC}

Applying KVL to the loop ABENA, we get

$$V_{CC} = I_B R_B + V_{BE}$$

Or $V_{CC} = I_B R_B$ [V_{BE} is negligible]

$$R_B = \frac{V_{CC}}{I_B}$$

Stability Factor (S) $= \dfrac{1+\beta}{1-\beta\left(\dfrac{\partial I_B}{\partial I_C}\right)}$

Since in a fixed bias circuit, I_B is independent of I_C. Hence

$$\frac{\partial I_B}{\partial I_C} = 0 \quad \therefore S = 1+\beta$$

Advantages: (i) This circuit is very simple.

(ii) Biasing conditions can be set easily.

Disadvantages :(i) Stability factor is very high.

(ii) Provides poor stabilization.

5.5.2 COLLECTOR-TO-BASE BIAS

In this circuit, shown in Fig.5.3, the DC supply voltages for the collector and base are provided from the same source V_{CC}; a high resistance R_B is connected between collector and base as shown in Fig 5.3. The required zero signal base current is determined by the collector-to-base voltage V_{CB}.

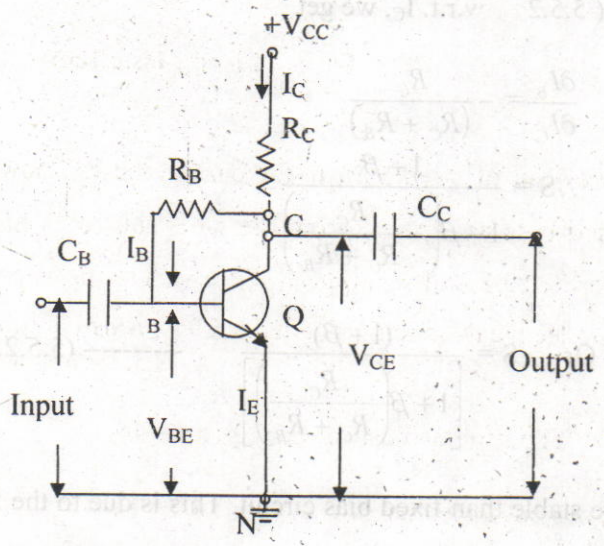

Fig 5.3 Collector to base bias circuit **Analysis**

The zero signal collector current = I_C

The zero signal base current = $I_B = I_C/\beta$

Supply voltage = V_{CC}

Applying KVL to the loop ACBNA, we get

$V_{CC} = I_BR_C + I_CR_C + I_BR_B + V_{BE}$ ---------- (5.5.2:1)

Or $V_{CC} = I_CR_C + I_BR_B + V_{BE}$

(Since I_B is neglected as compared to I_C)

$\therefore I_B R_B = V_{CC} - V_{BE} - I_C R_C$

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B}$$

Or $$R_B \simeq \frac{V_{CC} - I_C R_C}{I_B} \quad (\because V_{BE} << V_{CC}) \qquad \text{---------- (5.5.2.2)}$$

Stability factor: $$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

To evaluate S, first we find an expression for I_B and then we find $\frac{\partial I_B}{\partial I_C}$

From Eq.(5.5.2.1), we can write

$$V_{CC} = I_B[R_C + R_B] + I_C R_C + V_{BE}$$

Or

$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{(R_C + R_B)} \qquad \text{---------- (5.5.2.3)}$$

Differentiating Eq.(5.5.2 w.r.t. I_C, we get

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{(R_C + R_B)}$$

$$\therefore S = \frac{1+\beta}{1-\beta\left(-\frac{R_C}{R_C + R_B}\right)}$$

Or $$S = \frac{(1+\beta)}{\left[1+\beta\left(\frac{R_C}{R_C + R_B}\right)\right]} \qquad \text{---------- (5.5.2.4)}$$

This circuit is more stable than fixed bias circuit. This is due to the feedback from the collector-to-base via R_B.

Achievement of stability

When I_C tends to increase (either because of rise in temperature or because of replacement of transistor by another transistor of large value of β), then the voltage V_{CE} decreases according to $V_{CE} = V_{CC} - I_C R_C$. Hence I_B also decreases because $I_B R_B = V_{CE} - V_{BE}$ which in turn tends to decrease I_C to its original value. Thus the operating point is stabilized.

Advantages

(i) Stability factor is less than (1+β).

(ii) Provides better thermal stability than fixed bias.

Disadvantages

(i) The resistor R_B causes a feed back of AC signal from collector to base and hence reduces the voltage gains.

(ii) Stability factor is fairly high.

5.5.3 SELF BIAS OR VOLTAGE-DIVIDER BIAS

A circuit which is used to establish a stable operating point is known as a *Self biasing circuit.* It is shown in Fig.5.4 The resistors R_1, R_2 provide biasing and R_E provides stabilization. R_C act as a load résistance. Voltage drop across R_2 provide a forward bias to the emitter-base junction and voltage drop across R_1 provides a reverse bias to the collector-base junction. C_B and C_C are the blocking and coupling capacitors.

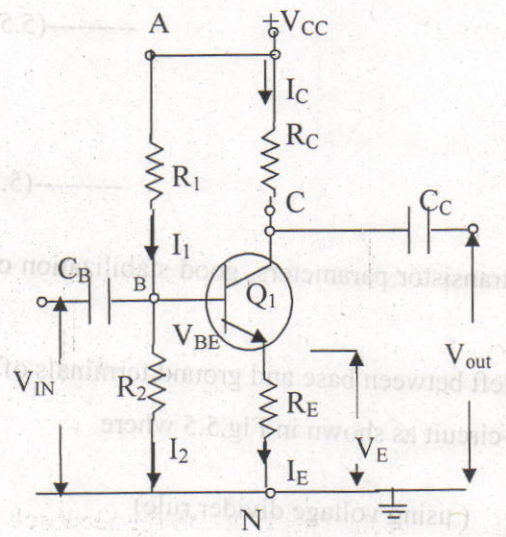

Fig.5.4 Self bias circuit

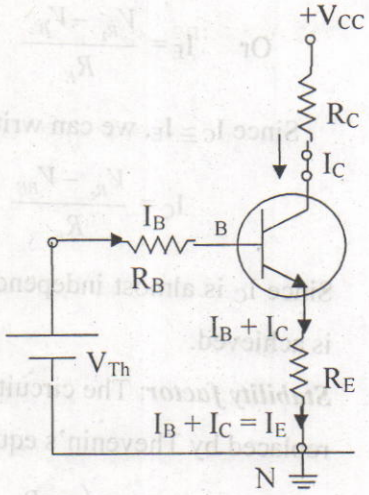

Fig.5.5 Thevenin's Equivalent of Fig 5.4

Fig.5.5 is the Thevenin's equivalent circuit obtained by applying Thevenin's theorem to the input section of circuit shown in Fig.5.4

Analysis

$I_1 \rightarrow$ current flowing through R_1

$I_2 \rightarrow$ current flowing through R_2

From figure, $I_1 = I_B + I_2$

Or $I_1 \cong I_2$ (Since I_B i. . small)

From Fig.5.4, we can write (applying KVL to the input section)

$$V_{CC} = I_1R_1+I_2R_2$$

Or $V_{CC} = I_1(R_1+R_2)$ $(\therefore I_2 \simeq I_1)$

Or $$I_1 = \frac{V_{CC}}{(R_1+R_2)} \qquad \text{----------(5.5.3.1)}$$

From Fig.4.5, $V_{Th} = V_{R2} = I_1R_2$

Or $$V_{Th} = \frac{V_{CC}}{(R_1+R_2)}R_2$$

$$V_{Th} = \left(\frac{R_1}{R_1+R_2}\right)V_{CC} \qquad \text{------ (5.5.3.2)}$$

But $V_{R2} = V_{BE}+V_E$ (Applying KVL to the lower section on input side)

Or $V_{R2} = V_{BE}+I_ER_E$

Or $I_ER_E = V_{R2}-V_{BE}$

Or $$I_E = \frac{V_{R_2}-V_{BE}}{R_E} \qquad \text{--------(5.5.3.3)}$$

Since $I_C \cong I_E$, we can write

$$I_C = \frac{V_{R_2}-V_{BE}}{R_E} \qquad \text{--------(5.5.3 4)}$$

Since I_C is almost independent of transistor parameters, good stabilization of Q point is achieved.

Stability factor: The circuit to the left between base and ground terminals of Fig.5.4 is replaced by Thevenin's equivalent circuit as shown in Fig.5.5 where

$$V_{Th} = \left(\frac{R_2}{R_1+R_2}\right)V_{CC} \qquad \text{(using voltage divider rule)}$$

$$R_B = R_1//R_2 = \frac{R_1R_2}{R_1+R_2}$$

Applying KVL around the base circuit of Fig.5.5, we get

$$V_{Th} = I_BR_B+V_{BE}+I_ER_E$$
$$= I_BR_B+V_{BE}+(I_B+I_C)R_E$$
$$= I_B[R_B+R_E]+I_CR_E+V_{BE}$$

Or $V_{Th} = I_B[R_B+R_E] + I_C R_E$ (Since V_{BE} is small)

Differentiating above equation w.r.t I_C we get

$$0 = \frac{\partial I_B}{\partial I_C}[R_B + R_C] + R_E$$

Or $$\frac{\partial I_B}{\partial I_C}[R_B + R_E] = -R_E$$

Or $$\frac{\partial I_B}{\partial I_C} = -\left(\frac{R_E}{R_B + R_E}\right)$$

But stability factor $$S = \frac{(1+\beta)}{\left[1+\beta\left(\frac{R_C}{R_C + R_B}\right)\right]}$$

Or $$S = \frac{1+\beta}{1+\beta\left[-\frac{R_E}{R_B + R_E}\right]} = \frac{(1+\beta)(R_B + R_E)}{R_B + R_E + \beta R_E}$$

Or $$S = \frac{R_E(1+\beta)\left[1+\frac{R_B}{R_E}\right]}{R_E\left[(1+\beta)+\frac{R_B}{R_E}\right]}$$

Or $$S = \frac{(1+\beta)\left(1+\frac{R_B}{R_E}\right)}{\left(1+\beta+\frac{R_B}{R_E}\right)} \qquad \text{---------- 5.5.3.5}$$

From Eq.(5.5.3.5), it is clear that

(i) $S=1+\beta$ when $R_E \rightarrow 0$

(ii) $S=1$ when $R_B = 0$

Achievement of stability

Let there be rise in temperature. This rises I_{CBO} and hence I_C. The rise in I_C increases I_E. As a result of this, the voltage drop across R_E increases and hence V_{BE} decreases, according to $V_{BE} = V_{Th} - V_E$. This lowers the base current I_B which in turn tends to restore I_C to its original value. Thus the presence of R_E improves the operating point stability.

5.6 LOAD LINE ANALYSIS

Load line is a straight line drawn on the output characteristics of a transistor, joining the cut off and saturation points. There are two types of load lines: (i) DC load line (ii) AC load line.

5.6.1 AC and DC load lines

(i) **DC load line**: This line determines the locus of I_C and V_{CE} in the zero signal conditions.

(ii) **AC load line**: This line determines the locus of I_C and V_{CE} when the signal is applied.

5.6.2 Load line analysis of a transistor:

The output characteristics of a transistor in any configuration are determined experimentally and indicate the relation between output voltage and output current (For ex. V_{CE} and I_C). However, the same information can be obtained in a much simpler way by representing mathematical relation between V_{CE} and I_C graphically. This method is quite easy and is frequently used in the analysis of transistor applications.

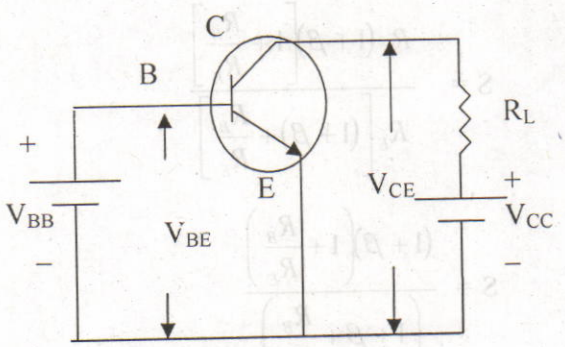

Fig.5.6

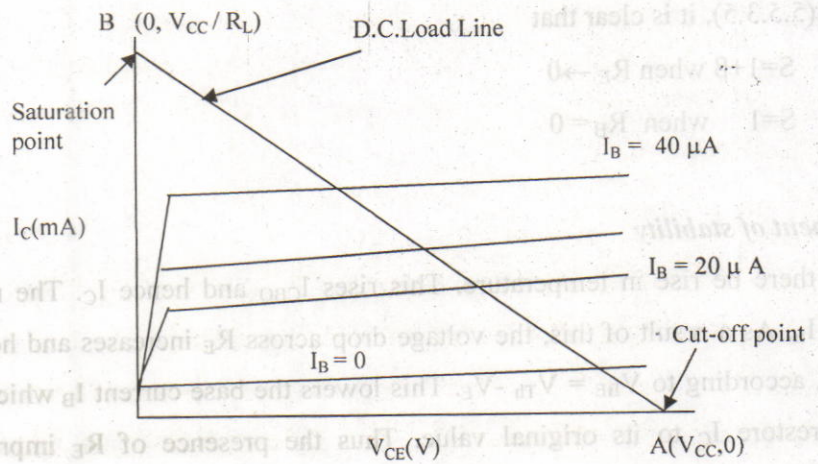

Fig.5.7 Output characteristics

Consider the circuit shown in the Fig.5.6

Applying KVL to the output section, we get

$$V_{CC} = V_{CE} + I_C R_L \qquad \text{--------- 5.6.2.1}$$

This is a first degree equation and can be represented by a straight line on the output characteristics. This is known as DC load line and determines the locus of (V_{CE}, I_C) points, for given values of R_L.

To draw the DC load line

Eq.(1) $\Rightarrow$ $V_{CE} = V_{CC} - I_C R_L$ ---------- 5.6.2.2

Or $I_C = \dfrac{V_{CC} - V_{CE}}{R_L}$

$$I_C = \left(-\frac{1}{R_L}\right) V_{CE} + \left(\frac{1}{R_L}\right) V_{CC} \qquad \text{--------- 5.6.2.3}$$

Eq.(5.6.2.3) is in the form of y = mx + c. Hence this represents the straight line AB with slope $-1/R_L$

Case-1 Consider $I_C = 0$ on X-axis

Eq. (5.6.2.3) $\Rightarrow$ $V_{CE} = V_{CC}$ i.e. A is (V_{CC}, 0) -- ***cutoff point***

Case-2 Let $V_{CE} = 0$ on Y-axis

Eq (5.6.2.3) $\Rightarrow I_C = \dfrac{V_{CC}}{R_L}$

$\therefore$ B is $\left(0, \dfrac{V_{CC}}{R_L}\right)$ -------- ***saturation point***

After marking the points A and B on V_{CE} and I_C- axes, these points are joined to obtain the DC load line.

AC Load line:

It is a line drawn on the output characteristics of a transistor circuit which gives the values of I_C and V_{CE} when signal is applied. This is obtained by joining two points C and D whose coordinates are

C (($V_{CE} + I_C R_{ac}$), 0) and D (0, $I_C + \dfrac{V_{CE}}{R_{ac}}$) where R_{ac} is the AC load of the amplifier circuit. AC load line is shown in Fig.5.8

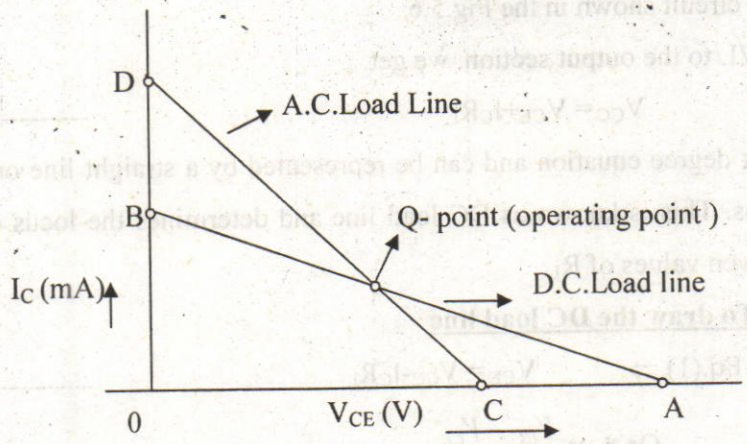

Fig.5.8

5.7 SUMMARY

In order to exhibit the behavior of a transistor, i.e. transferring the signal from low resistance region to high resistance region, emitter and collector junctions are to be biased. This means emitter must be forward biased and collector must be reverse biased. Biasing can be done by using batteries or power supplies or circuits. Each biasing circuit has its own advantages and disadvantages. The merit of biasing circuit in holding the D.C collector current at the operating point is expressed in terms of stability factor S. Load line approach is an easy way of understanding the behavior of a transistor under no signal condition. DC load line can be drawn on the output characteristics. When signal is applied to the transistor, AC load line can be drawn on the output characteristics. A load line can be drawn by marking the cut-off and saturation points on the output characteristics and join them by a straight line.

When transistor's biasing voltages and currents are changed such that maximum power dissipation limit is crossed, the transistor heats up. The increased temperature increases the current which further heats up the transistor, This process known as Thermal runaway permanently damages the transistor.

5.8 KEY TERMINOLOGY

Bias, Biasing, Load line, Stability factor, Biasing circuits, Operating point, Thermal runaway.

SOLVED NUMERICAL PROBLEMS

***Example(1)*:** In a fixed bias circuit, if β=100, R_B=100KΩ, R_C=1KΩ and V_{CC}=10V then find the value of V_{CE}?

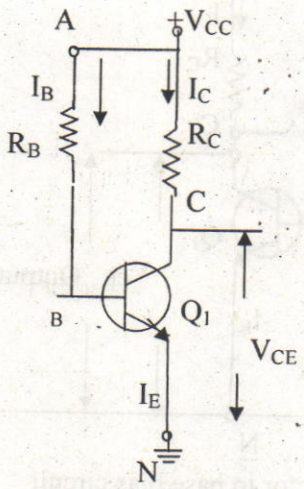

Fig.5.9 Fixed bias circuit

Solution: Given

V_{CC} =10V; RC =1KΩ =1000Ω; β =100; R_B =100 x 10^3 Ω

We know that (by applying KVL to the input section)

$$V_{CC} = I_B R_B + V_{BE}$$

Or $$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{V_{CC}}{R_B} \quad (V_{BE} << V_{CC})$$

$$= \frac{10}{100 \times 10^3} = 0.1\text{mA} = 100\mu\text{A}$$

But collector current $I_C = \beta I_B$

$$\therefore I_C = 100 \times 0.1\text{mA} = 10\text{mA}$$

$\therefore$ Collector to emitter voltage (obtained by applying KVL to the output section)

$$V_C = V_{CC} - I_C R_C$$

$$= 10 - 10 \times 10^{-3} \times 1 \times 10^3 = 0 \text{ V}$$

This shows that the transistor is in saturation region.

Example (2)

For the circuit shown in Fig.5.10, find the operating point if V_{CC} = 15 V, R_B = 200 KΩ, R_C = 2 KΩ, β = 50.

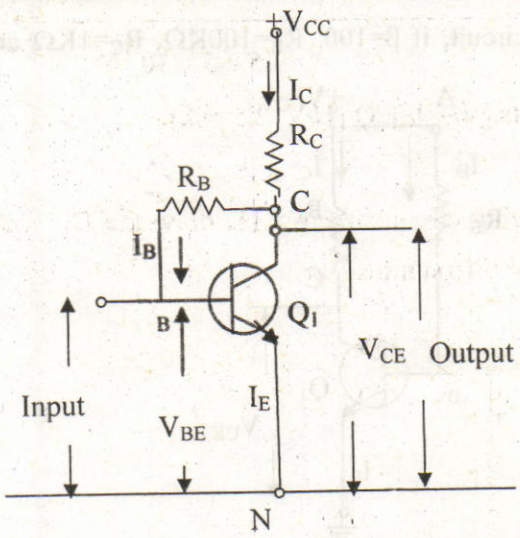

Fig.5.10 Collector to base bias circuit

***Solution*:**

Given $R_B = 200\ K\Omega = 200 \times 10^3\ \Omega$

$R_C = 2\ K\Omega = 2 \times 10^3\ \Omega$

$\beta = 50,$

$V_{CC} = 15\ V$

To find Collector current $I_C = ?$

Collector to emitter voltage $= V_{CE} = ?$

Applying KCL to the input side of Fig.4.10, we get

$$V_{CC} = (I_C + I_B)\, R_C + I_B R_B + V_{BE}$$

Since $I_B << I_C$ and $V_{BB} << V_{CC}$, we can write

$$V_{CC} = I_C R_C + I_B R_B$$

but $I_C = \beta I_B$

$$\therefore V_{CC} = \beta I_B R_C + I_B R_B = I_B [\beta R_C + R_B]$$

$$\therefore I_B = \frac{V_{CC}}{\beta R_C + R_B} = \frac{15}{50 \times 2 \times 10^3 + 200 \times 10^3}$$

$$= \frac{15}{300 \times 10^3} = 5 \times 10^{-5}\ A = 50\ \mu A.$$

$\therefore$ Collector current $I_C = \beta\, I_B = 50 \times 50 \mu A. = 2500\ \mu A. = 2.5\ mA.$

$\therefore$ collector to emitter voltage $V_{CE} = V_{CC} - I_C R_C$

$$= 15 - 2.5 \times 10^{-3} \times 2 \times 10^3$$

$= 15 - 5 = 10$ V.

$\therefore$ Operating points [V_{CE}, I_C], Q [10V, 2.5 mA].

Eample (3)

In the following circuit of Fig.5.11, draw the DC lode line, find the operating point for silicon transistor.

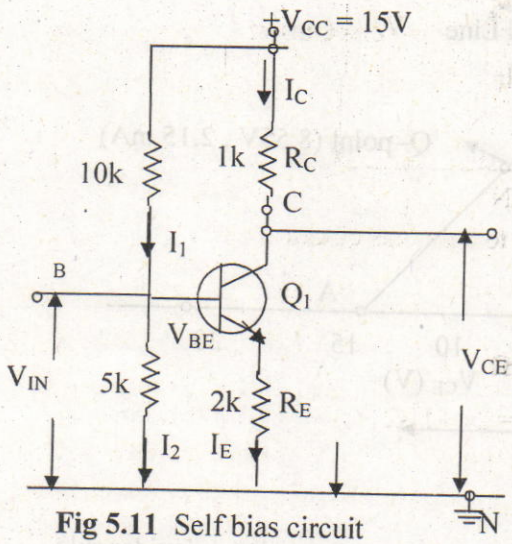

Fig 5.11 Self bias circuit

Solution:

Given $V_{CC} = 15$ V, $V_{BE} = 0.7$ V for Silicon,

$R_1 = 10\ K\Omega = 10 \times 10^3 \Omega$

$R_2 = 5\ K\Omega = 5 \times 10^3 \Omega$

$R_C = 1\ K\Omega = 1 \times 10^3 \Omega$

$R_E = 2\ K\Omega = 2 \times 10^3 \Omega$

To find Q [V_{CC}, I_C]

$V_{CC} = I_C R_C + V_{CE} + I_E R_E$

$V_{CC} = I_C R_C + V_{CC} + I_C R_E \quad (\because I_E \approx I_C)$

$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$ ---------- (1)

Eq. (1) in the form of $y = mx + c$. Hence

Case 1: when $I_C = 0$; $V_{CE} = V_{CC} = 15$ V (cutoff point 'A' on the output characteristics)

Case 2. When $V_{CE} = 0$ V ; $I_C = \dfrac{V_{CC}}{R_C + R_E} = \dfrac{15}{1 \times 10^3 + 2 \times 10^3}$

$= \frac{15}{3000} = 5\times10^{-3} = 5$ mA (saturation point 'B' on the output characteristics)

Graph :

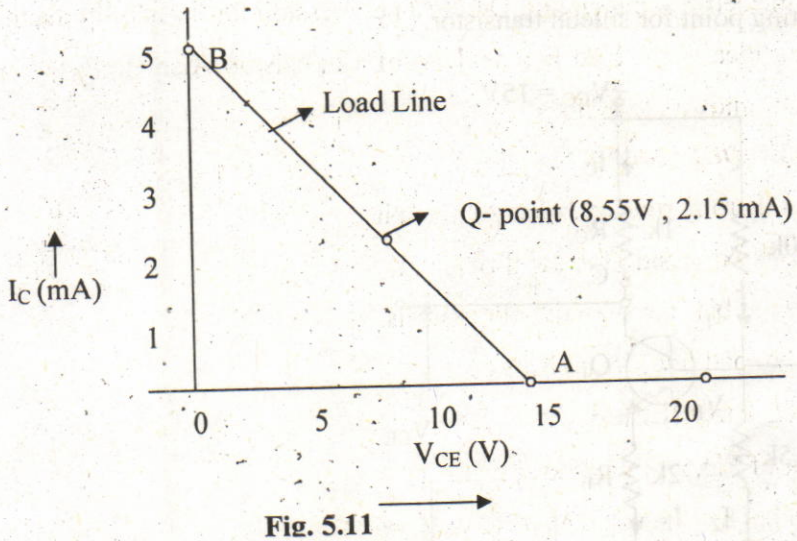

Fig. 5.11

Finding Operating Point:

Potential drop across $R_2 = 5K\Omega$ resistor using voltage devider rule.

$$V_2 = V_{CC}\left[\frac{R_2}{R_1+R_2}\right]$$

$$V_2 = 15\left[\frac{5\times10^3}{10\times10^3+5\times10^3}\right] = 15\left[\frac{5}{15}\right] = 5\text{ V}$$

Emitter current $$I_{CQ} = \frac{V_2 - V_{BE}}{R_E} = \frac{5-0.7}{2\times10^3} = \frac{4.3}{2\times10^3} = 2.15\text{ mA}$$

Hence collector – emitter voltage

$$V_{CEQ} = V_{CC} - I_C(R_C+R_E)$$

$$= 15 - 2.15\times10^{-3}\left(1\times10^3+2\times10^3\right)$$

$$= 15 - 2.15 \text{ x } 3 = 15 - 6.45 = 8.55\text{ V}.$$

'Q' point coordinates are $Q(V_{CEQ}, I_{CQ})$

i.e Q(8.55 V, 2.15mA) .

5.9 SELF ASSESSMENT QUESTIONS

(I) ***LONG ANSWER QUESTIONS***

(i) What is stability factor? Explain how to compare the biasing circuits in terms of this factor. Obtain a relation for stability factor.

(ii) What are the various factors responsible for the shift in Q-point of a transistor? How stability I achieved by self bias arrangement?

(iii) Draw the self biasing circuit. Derive an expression for its stability factor.

(iv) Give an idea about load line analysis of a transistor. Also explain how to draw DC and AC load lines?

(II) ***SHORT ANSWER QUESTIONS***

(i) What is thermal runway? How to avoid it?

(ii) Derive an expression for stability factor.

(iii) Draw fixed bias circuit. Give its analysis.

(iv) What is a load line? What is its use?

(III) NUMERICAL PROBLEMS

(1) In the circuit of Fig.5.13 with no signal,

(i) What will be the Q-point if V_{CC}=12V; R_C=6KΩ

(ii) If zero signal base current is 20μA with β=50,.

draw the load line **Ans**: Q (6V, 1mA)

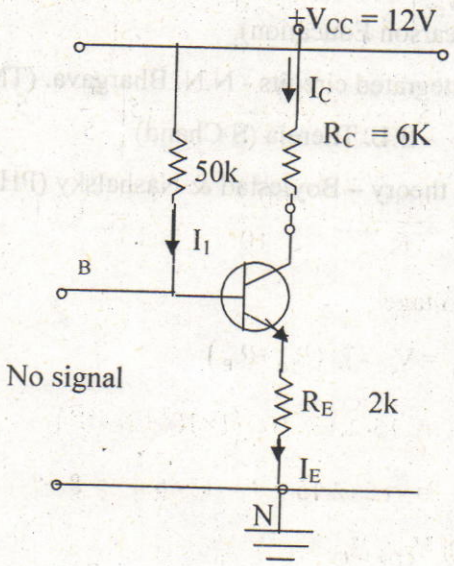

Fig.5.13 Self bias circuit

(2) Draw the DC load line for the following circuit in Fig.5.14

Ans: Cutoff point (10V, 0) ; Saturation point (0, 5 mA)

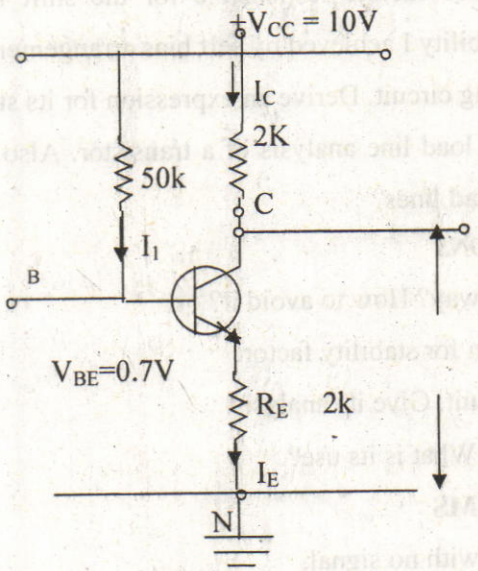

Fig 5.14

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UNIT-II **LESSON-6**

TRASISTOR MODELS

OBJECTIVES OF THE LESSON

This lesson introduces various models used to represent a transistor, explains about the h-parameters, transistor hybrid model, equivalent circuit, analysis of CE transistor amplifier using hybrid parameter model, It also describes the B.J.T high frequency model, and explains about the cut-off frequencies $f\alpha$, f_β and f_T.

STRUCTURE OF THE LESSON

6.1 Introduction

To represent the equivalent circuit for a transistor, various types of models were proposed. Of these, the h-parameters are found to be more suitable for transistors as these can be determined accurately by simple methods. So, the concept of h-parameters, two-port net work, high frequency model of BJT are introduced here. Using the h-parameters, one can understand the behavior of an amplifier. The response of BJT at low and high frequencies can easily be studied the amplifier parameters like, voltage gain, current gain, input impedance, out put impedance can also be calculated. The behavior of transistor at low and high frequencies can be understood with the help of $f\alpha$, f_β and f_T parameters.

6.2 Two-port network representation of a transistor

A transistor is a three terminal device capable of producing amplification. One of the three terminals can be treated as a common terminal for both input and output. We can treat a transistor as a device having one pair of terminals at out put. Hence transistor can be understood as a two-port device, with one input port, where input can be applied for amplification, and with one output port, from which output can be collected. So, a transistor can be represented as a "Black Box" shown in Fig.6.1.

The terminal behavior of a large class of two-port device is specified by two voltages and two currents. We can select two of the four quantities as the impudent variables and express the remaining two in terms of the chosen independent variables

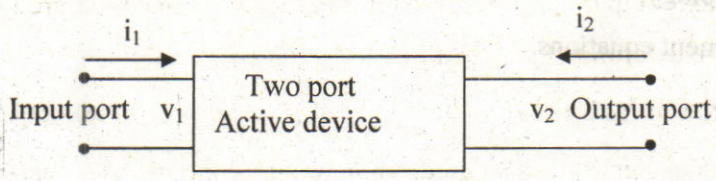

Fig 6.1

6.3 h-parameters or hybrid parameters or mixed parameters:

Consider in Fig 6.1 with input and output voltages and currents. If i_1, i_2 are independent , and if the two-port device is linear , we can write.

$$v_1 = h_{11}i_1 + h_{12}v_2 \qquad \text{(6.3.1)}$$

$$r_2 = h_{21} i_1 + h_{22} v_2 \qquad \text{(6.3.2)}$$

The quantities h_{11}, h_{12}, h_{21} and h_{22} are called the hybrid parameters because they are not all alike dimensionally. From Eq.(6.3.1) and (6.3.2), h-parameters are defined as follows.

$$h_{11} = \left.\frac{v_1}{i_1}\right|_{v_2=0}$$ = Input impedance with output short –circuited (ohms)

$$h_{12} = \left.\frac{v_1}{v_2}\right|_{i_1=0}$$ = Reverse open circuit voltage amplification (dimensionless)

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2=0}$$ = Forward current gain (dimensionless)

$$h_{22} = \left.\frac{i_1}{v_2}\right|_{i_1=0}$$ = Output admittance (mhos)

6.4 Determination of hybrid parameters

The transistor model presented in this lesion is given in terms of the h-parameters, which are real numbers, at audio frequencies. Further they are easy to measure, can also be obtained from the transistor static characteristic curves, and are convenient to use in circuit analysis of transistors by the manufacturers.

If the input and output characteristics of a particular connection are given, the h-parameters can be determined graphically

(i) Determination of h_{fe} and h_{oe}

The output characteristics are used to determine the h_{fe}, h_{oe} parameters. To determine h_{fe}, select an operating point 'Q' on one characteristic curve. Drop a perpendicular (a dotted line) on to X-axis as shown in Fig.6.2.

Also draw a tangent line AB through 'Q'.

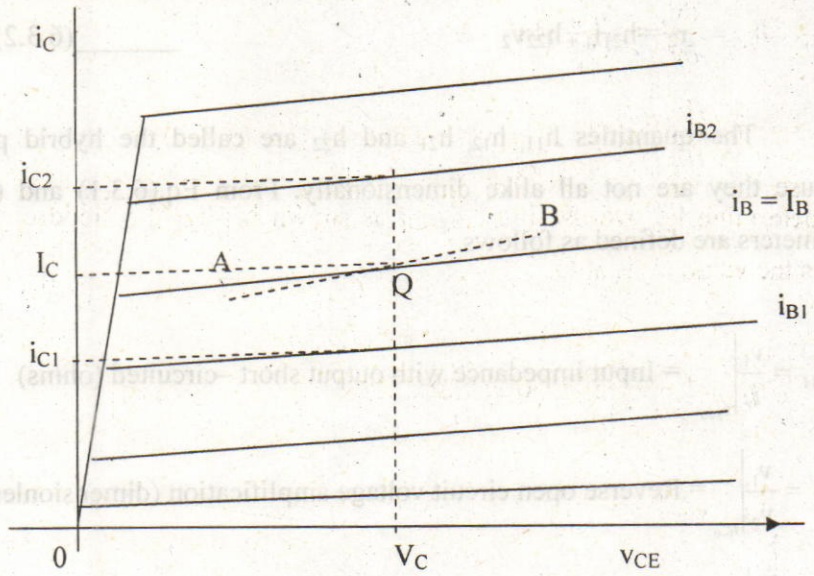

Fig 6.2 Determination of h_{fe} and h_{oe}

From the definition of h_{fe},

$$h_{fe} = \left.\frac{\Delta i_C}{\Delta i_B}\right|_{V_C}$$

$$= \frac{i_{C2} - i_{C1}}{i_{B2} - i_{B1}} \qquad \ldots\ldots(6.4.1)$$

The current increments are taken around the Quiescent point 'Q' which corresponds to the base current $i_b = I_B$ and to the collector voltage $V_{CE} = V_C$.

To determine h_{oe}, we can use the tangent shown in Fig.6.3. The slope of the tangent gives the value of h_{oe}.

$$h_{oe} = \frac{\partial i_c}{\partial v_c} = \frac{i_{c2} - i_{c1}}{v_{c2} - v_{c1}} \,|\, I_B \qquad \ldots\ldots\ldots (6.4.2)$$

ii) Determination of h_{ie} and h_{re}

The input characteristics are used to determine the h_{ie}, h_{re} parameters.

To determine h_{re}, we select an operating point on the middle curve as shown in Fig.6.4. Drop a perpendicular (dotted line) on to X-axis. Also draw a tangent CD through Q. From the definition of h_{re},

$$h_{re} = \frac{\partial v_b}{\partial v_c} \approx \frac{\Delta V_B}{\Delta V_C} \mid I_B$$

$$= \frac{(V_{B2} - V_{B1})}{(V_{C2} - V_{C1})} \qquad \ldots\ldots\ldots (6.4.3)$$

To determine h_{ie}, we use the tangent as shown in Fig; the slope of the tangent gives the value of h_{ie} at Q.

$$\therefore h_{ie} = \frac{\partial v_b}{\partial i_b} = \frac{\Delta V_B}{\Delta i_B} \mid V_C = \frac{V_{B2} - V_{B1}}{i_{B2} - i_{B1}} \qquad \ldots\ldots\ldots (6.4.4)$$

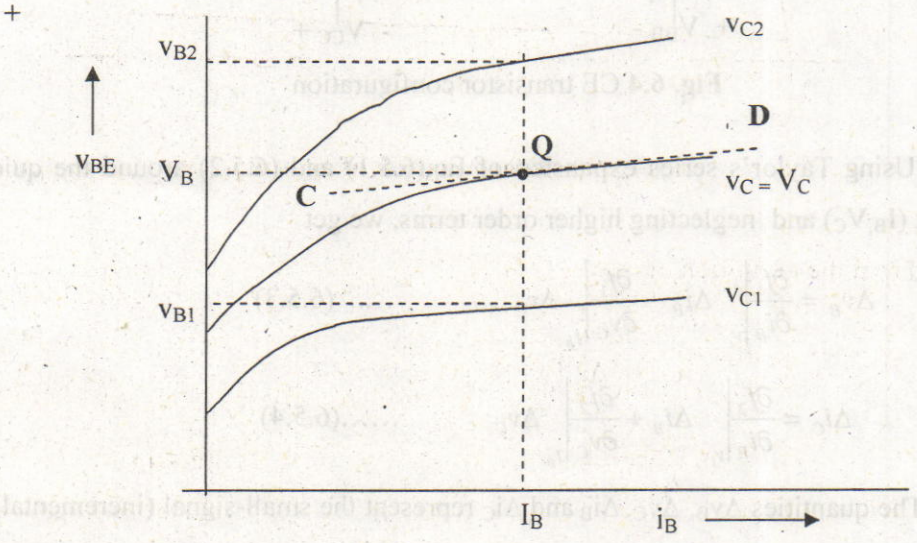

Fig 6.3 Determination of h_{ie} and h_{re}

6.5 Transistor hybrid model

To arrive at a transistor linear model or equivalent circuit, it is assumed that the variations about quiescent point are small. Hence transistor parameters can be considered constant over the signal variation.

To draw the hybrid model, consider the CE connection shown in Fig.6.4. The variables i_B, i_C, $V_{BE} = V_B$, $V_{CE} = V_C$ represent total instantaneous currents and voltages. From the discussion of transistor voltages and currents, we can select the current i_B and voltage v_C as independent variables, and the current i_C and voltage v_B as dependent, variables, we may write

$$v_B = f_1(i_B, v_C) \qquad \ldots\ldots\ldots (6.5.1)$$

$$i_C = f_2(i_B, v_C) \qquad \ldots\ldots (6.5.2)$$

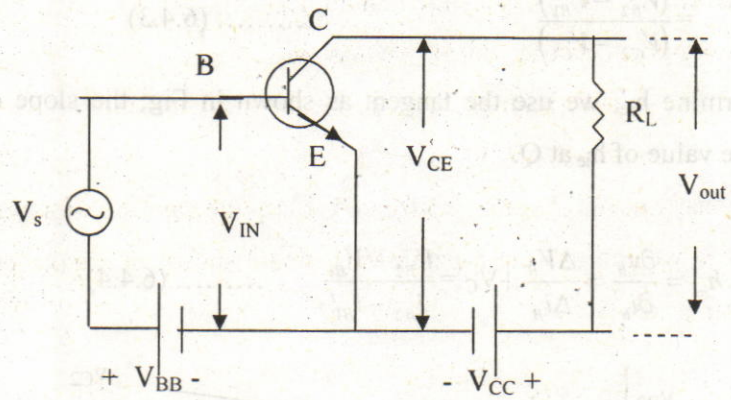

Fig. 6.4 CE transistor configuration

Using Taylor's series expansion of Eq.(6.5.1) and (6.5.2) around the quiescent point (I_B,V_C) and neglecting higher order terms, we get

$$\Delta v_B = \left.\frac{\partial f_1}{\partial i_B}\right|_{V_C} \Delta i_B + \left.\frac{\partial f_1}{\partial v_C}\right|_{I_B} \Delta v_C \qquad \ldots\ldots (6.5.3)$$

$$\Delta i_C = \left.\frac{\partial f_2}{\partial i_B}\right|_{V_C} \Delta i_B + \left.\frac{\partial f_2}{\partial v_C}\right|_{I_B} \Delta v_C \qquad \ldots\ldots (6.5.4)$$

The quantities Δv_B, Δv_C, Δi_B and Δi_C represent the small-signal (incremental) base and collector voltages and currents. We represent the above quantities with symbols v_b, v_c, i_b and i_c. We may write now Eq.(6.5.3) and (6.5.4) in the following form.

$$v_b = h_{ie} i_b + h_{re} v_c \qquad \ldots\ldots (6.5.5)$$

$$i_c = h_{fe} i_b + h_{oe} v_c \qquad \ldots\ldots (6.5.6)$$

Where

$$h_{ie} \equiv \frac{\partial f_1}{\partial i_B} = \left.\frac{\partial v_B}{\partial i_B}\right|_{V_C} \quad ; \quad h_{re} \equiv \frac{\partial f_1}{\partial v_c} = \left.\frac{\partial v_B}{\partial v_C}\right|_{I_B} \qquad \ldots\ldots (6.5.7)$$

and $$h_{fe} \equiv \frac{\partial f_2}{\partial i_B} = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C} \quad ; \quad h_{oe} \equiv \frac{\partial f_2}{\partial v_c} = \left.\frac{\partial i_C}{\partial v_C}\right|_{I_B} \qquad \ldots\ldots (6.5.8)$$

The partial derivatives of Eq. (6.5.7) and (6.5.8) define the h-parameters, for the common-emitter connection. These parameters can be obtained from the transistor characteristics curves and that they are real numbers.

If the two-port device is linear, we may write,

$$v_1 = h_{11}i_1 + h_{12}v_2 \quad \text{..... (6.5.9)}$$

$$i_2 = h_{21}i_1 + h_{22}v_2 \quad \text{.....(6.5.10)}$$

We observe that Eq. (6.5.5) and (6.5.6) are exactly the same form as Eq. (6.5.9) and (6.5.10). Hence we can use the h-parameters model shown in Fig.6.6 can be used to represent a transistor.

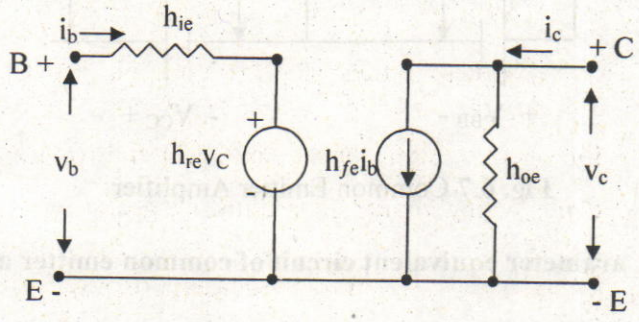

Fig.6.5 Hybrid model for CE configuration

$h_{21} \equiv \left.\frac{i_2}{i1}\right|_{v_{2=0}}$ = short circuit current gain (dimensionless)

$h_{22} \equiv \left.\frac{i_2}{v_2}\right|_{i_{1=0}}$ = output conductance with input open circuit (mhos)

Alternative subscript notation is

i = 11 = input ; o = 22 = output.

f = 21 = forward; r = 12 = reverse transfer.

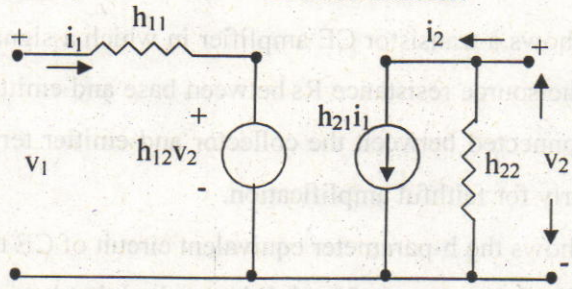

Fig.6.6 Hybrid model for two- port network

In the case of transis he type of configuration.

Ex : $h_{ib} = h_{11b}$ = input resistance in CB configuration

$h_{fe} = h_{21e}$ = short - circuit forward current gain in CE configuration.

The hybrid circuit for any device characterized by Eq.(6.5.9) and (6.5.10) is indicated in Fig.6.6.

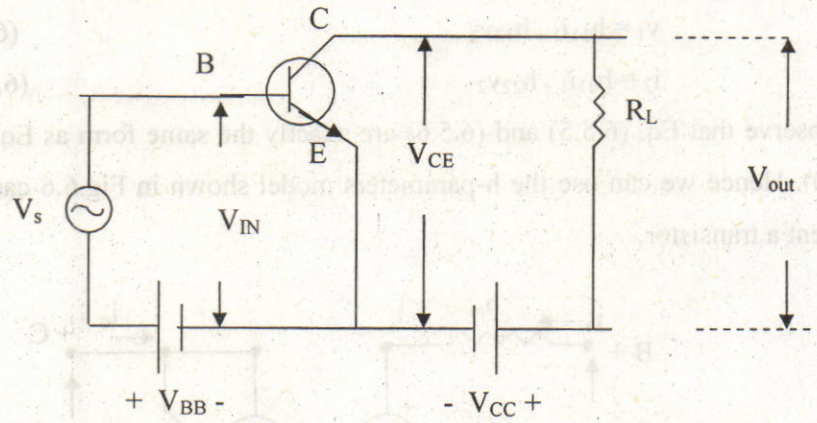

Fig. 6.7 Common Emitter Amplifier

6.6 h arameter equivalent circuit of common emitter amplifier and analysis

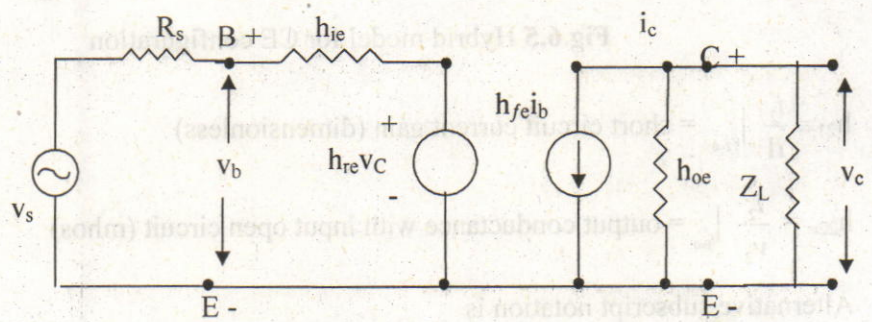

Fig.6.8 Hybrid model for CE amplifier

Fig .6.7 shows a transistor CE amplifier in which a signal source is connected in series with the source resistance Rs between base and emitter terminals. An external load Z_L is connected between the collector and emitter terminals. The transistor is biased properly for faithful amplification.

Fig.6.8 shows the h-parameter equivalent circuit of CE transistor. The circuit of Fig.6.8 is valid for any type of load. It is required that h-parameters remain constant over the operating frequency range. Assume that the varying voltages and currents are sinusoidal in nature.

We analyze the amplifier as shown below:

Analysis

i) Current gain (A_I)

It is defined as the ratio of out put current to the input currents

$$A_I = -\frac{Ic}{I_b} = .+\frac{I_L}{I_b}$$

But $V_C = I_L Z_L = -I_c Z_L$ _____(6.6.1)

Appling KCL to the output, we can write

$$Ic = h_{fe} I_o + h_{oe} V_C \quad \text{_____ 6.6.2)}$$

Or $I_c = h_{fe} I_o + h_{oe}\left[-I_c Z_L\right]$

$= h_{fe} I_o - h_{oe} I_c Z_L$

Or $I_c\left(1 + h_{oe} Z_L\right) = h_{fe} I_b$

Or $\frac{I_c}{I_b} = \frac{h_{fe}}{\left(h_{oe} z_L + 1\right)}$ $\quad \therefore A_I = -\frac{I_c}{I_b} = -h_{fe} \Big/ \left(h_{oe} Z_L + 1\right)$ _____(6.6.3)

(i) Input impedance(Z_i)

It is defined as the ratio of input voltage to the input current.

$$Z_i = \frac{V_o}{I_b}$$

Applying KVL to the input circuit, we get

$h_{ie} I_b + h_{re} V_c = V_b$ _____(6.6.4)

Or $V_b = h_{ie} I_b + h_{re}\left(-I_c Z_L\right)$

But current gain $A_I = -\frac{I_c}{I_b} \Rightarrow -I_c = A_I I_b$

$\therefore V_b = h_{ie} I_b + h_{re} A_I I_b Z_L$

$= I_b\left[h_{ie} + h_{re} A_I Z_L\right]$

$\therefore Z_i = \frac{V_b}{I_b} = h_{ie} + h_{re} A_I Z_L$ _____(6.6.5)

or $Z_i = h_{ie} + h_{re}\left[-\frac{h_{fe}}{h_{oe} Z_L + 1}\right] Z_L$

$$= h_{ie} - \frac{h_{fe}h_{re}}{\frac{1}{Z_L}[h_{oe}Z_L + 1]}$$

$$\text{Or } Z_i = h_{ie} - \frac{h_{fe}h_{re}}{h_{oe} + Y_L} \qquad \text{(6.6.6)}$$

(iii) Voltage Gain (A_v)

It is the ratio of output voltage to the input voltage.

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_c}{V_b}$$

But $V_c = -I_c Z_L = A_I I_b Z_L (\because I_c = -A_I I_b)$

$$\therefore A_V = \frac{A_I I_b Z_L}{V_b} = A_I \left[\frac{I_b}{V_b}\right] Z_L$$

$$\text{Or } A_V = \frac{A_I Z_L}{Z_I} \qquad \text{..... (6.6.7)}$$

(ii)Output Admittance (Y_o)

It is the ratio of out put current to the out put voltage.

$$Y_o = \frac{I_c}{V_c}$$

Output impedance Z_o (=1/Y_o) is obtained by equating V_s to Zero and load impedance to infinity. Also drive the output terminals from a generator V_c.

Let I_c be the current drawn from V_c then we can write.

$$Y_o = \frac{I_c}{V_c} \text{ with } V_S = 0; \quad Z_L = \infty$$

Applying KCL to the junction at the output we can write,

$$I_C = h_{fe} I_b + h_{oe} V_C$$

$$\therefore Y_o = -\frac{I_c}{V_c} = \frac{h_{fe} I_b}{V_c} + h_{oe} \qquad \text{(6.6.8)}$$

From Fig.6.8, with $V_s = 0$, we can write (applying KVL to the input)

$$0 = I_b R_s + I_b h_{ie} + h_{re} V_c$$

$$\text{Or } I_b [R_s + h_{ie}] = -h_{re} V_c$$

$$\text{Or } \frac{I_b}{V_c} = -\frac{h_{re}}{R_s + h_{ie}}$$

Or $$Y_o = -\frac{h_{fe}h_{re}}{R_s + h_{ie}} + h_{oe}$$ _____(6.6.9)

From the above parameters, we can conclude that

(i) Current gain depends inversely on Z_L

(ii) Voltage gain depends directly on Z_L

(iii) Z_i depends on Y_L

(iv) Y_o depends on R_s (source resistance)

6.7 BJT high frequency model

At low frequencies, it is assumed that the transistor responds instantly to changes of input voltages or current. However, at high frequencies, such is not the case because the charge carriers move from emitter to collector essentially through the process of diffusion. This involves time delay, which is insignificant at low frequencies but becomes quite important in case of high frequency signals. The other limitations are (i) presence of junction capacitance at emitter and collector junctions, (ii) transit time of carriers across the base region. Therefore, in high frequency transistors, physical size of device should be kept small; the base width must be narrow to reduce the transit time. The emitter and collector areas must be small to reduce the junction capacitance.

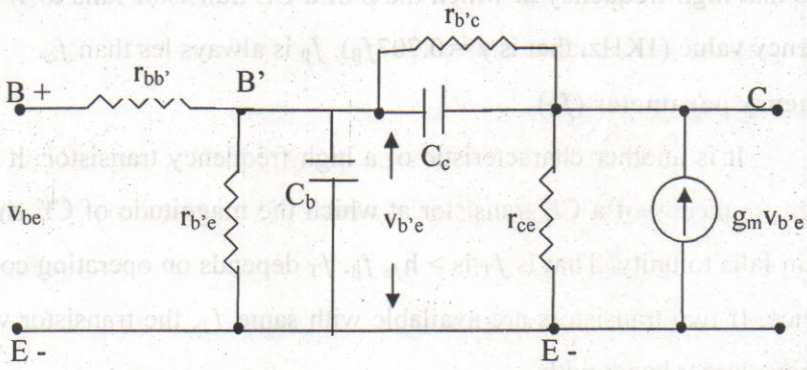

Fig.6.9 hybrid Π model of BJT

Fig.6.9 shows the hybrid Π-model of a transistor in CE configuration at high frequencies. In Fig.6.8 $r_{bb'}$ is the Ohmic base spreading resistance, and is encountered by the base current, due to the thinness of base region. $g_m V_{b'e}$, is the current generator across the emitter junction, the excess minority carrier

concentration injected into the base is proportional to $V_{b'e}$. Hence small signal collector current is proportional to $V_{b'e}$. $r_{b'e}$ is the resistance between internal node B' and E. The increase in minority carriers in the base results in increased recombination base current. C_e is the diffusion capacitance between B' and E. $r_{b'c}$ is the resistance between B' and C accounts for the feedback action.

The varying voltage across the collector base junction, changes the base width (base width modulation). This cause the emitter and collector currents to change. R_{ce} is the resistance between collector and emitter. Capacitance C_c accounts for the collector junction barrier capacitance.

6.8 Transistor cut-off frequencies

In transistors, there is an upper limit for the frequency of operation due to the inherent capacitance between electrodes (inter electrode capacitance), transit time of charge carriers from emitter to collector across the base. The limitation of frequency is expressed in terms of the following terms.

(1) Alpha cutoff frequency ($f\alpha$)

It is that high frequency at which the α of a CB transistor becomes $1/\sqrt{2}$ of its low frequency value ($\equiv$1KHz). It is found that f_α is directly proportional to the minority carrier mobility, inversely proportional to the square of the base width. For ex, if $\alpha = 0.95$ at 1KHz, then $f = 0.707 f_\alpha$

(2) Beta cutoff frequency (f_β)

It is that high frequency at which the β of a CE transistor falls to $1/\sqrt{2}$ of its low frequency value (1KHz. that is $f = 0.707 f_\beta$). f_β is always les than f_α.

(3) Frequency parameter (f_T)

It is another characteristic of a high frequency transistor. It is defined as that high frequency of a CE transistor at which the magnitude of CE short circuit current gain falls to unity. That is f_T is $> h_{fe} f_\beta$. f_T depends on operating conductance of the device. If two transistors are available with same f_T, the transistor with lower gain will have larger bandwidth.

6.9 SUMMARY

Though a bipolar junction transistor is a three terminal device, by taking one of its three terminals as a common terminal, it can be treated as a four-terminal device or a two-port device with two pairs of terminals (two ports). Its functioning can be understood with the help of different models based on h-parameters.

The hybrid Π-model circuit is used to analyze the performance of transistor at high frequencies.

6.10 KEY TERMINOLOGY

Base spreading resistance, h-parameters, f_α , f_β, f_T parameters, two-port network.

SOLVED NUMERICAL PROBLEMS

Example (1)

Find the load resistance to be connected to provide a current gain of 60 by CE transistor amplifier if h_{fe}=100; h_{oe} = 10 μA/V

Solution:

We have current gain $A_I = 60$

$$A_I = - h_{fe} / h_{oe} R_{L+1} \text{ or } 1 + h_{oe} R_L = - h_{fe} / A_I = -100 / -60 = 1.666$$

$$\therefore h_{oer} R_L = 1.666 - 1 = 0.666$$

$$\therefore R_L = 0.666 / 10 \times 10^{-6} = 0.666 \times 10^5$$

$$\therefore R_L = 66.6 \text{ K}\Omega$$

Example (2)

A CE transistor amplifier has a current gain of -60 and an input resistance of 2KΩ. Find the voltage gain if a load of 15KΩ is connected.

Solution:

Given $A_I = -60$, $Z_I = 2\text{k}\Omega$, $Z_L = 15\text{K}\Omega$,

To find : A_V

We know that $A_V = A_I Z_L / Z_I = -60 \times 15 \times 10^3 / (2 \times 10^3)$

$A_V = -450$

6.11 SELF ASSESSMENT QUESTIONS

(I) Long answer questions

(1) Give the high frequency Π-model of CE configuration of a transistor and discuss its parameters.

(2) Define h-parameters for low frequency CE transistor. Give an equivalent h-parameter model for a BJT under CE configuration.

(3) Draw the h-parameter equivalent circuit of CE transistor amplifier and obtain expressions for various parameters.

(II) Short answer questions

(1) Define h-parameters (low frequency) of CE transistor.

(2) Define the parameters f_α, f_β, f_T.

(3) Draw the h-parameter equivalent circuit of CE transistor amplifier.

(4) Draw the high frequency model of CE transistor and explain each element.

(III) Numerical problems

(1) A CE amplifier has a voltage source with an internal resistance $R_S = 1K\Omega$ and a load impedance $Z_L = 100\Omega$. Its h-parameters are $h_{ie} = 1K\Omega$, $h_{re} = 2x10^{-4}$; $h_{fe} = 100$; $h_{oe} = 25\mu A/V$. Find A_I, Z_I, A_v. (**Ans**: $A_I = -100$; $Z_I = 998\Omega$; $A_V = 10$)

(2) A CE transistor amplifier has a voltage gain of -200. Its input resistance is $10K\Omega$. Find its current gain if a load of $3K\Omega$ is connected. (**Ans** : $A_I = -60$)

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UNIT II **LESSON-7**

TRANSISTOR AMPLIFIERS

OBJECTIVIES OF THE LESSON

This lesson explains the concept of an amplifier, their classification, phase angle shift of 180^0 by CE amplifier; discusses about various amplifier parameters like voltage gain, input and output resistances, efficiency, frequency response, RC coupled amplifier and its analysis.

STRUCTURE OF THE LESSON

7.1 INTRODUCTION

Almost no electronic system works without an amplifier. In communication systems (Ex Radio and T.V), the signal received is so weak that it needs amplification in several stages before presented with or without processing as output. We are able to hear the news or cricket commentary on our radio, because of the various amplifiers in the radio receiver which amplify the signal received by its antenna. Amplifier is used not only in communication systems but also in tape recorder, stereo, ECG, EEG, and measuring instruments etc to raise the signal level. Amplifiers are available for amplifying voltage, current and power levels and which operate at various frequencies of radio frequency spectrum.

7.2 Concept of an Amplifier

Amplification: The process of raising the strength of a weak signal is known as Amplification.

Amplifier: It is an electronic device, which accomplishes the task of amplification.

A Bipolar Junction Transistor (BJT) can act as an amplifier, when the following conditions are satisfied:

(1) The transistor is to be operated in the active region (i.e. Emitter junction is forward biased and Collector junction is reverse biased)

(2) A signal source is to be connected in the input circuit.

(3) A load is to be connected in the output circuit.

For the sake of simplicity in the analysis, we assume the signal to be sinusoidal in nature. The load is a simple resistor or impedance. (Impedance is usually a combination of a resistor and capacitor, or a resistor and an inductor or a resistor, inductor and capacitor). Another circuit which utilizes the signal output of the previous stage can also form a load. This circuit is also represented as impedance.

7.3 CB Transistor Amplifier

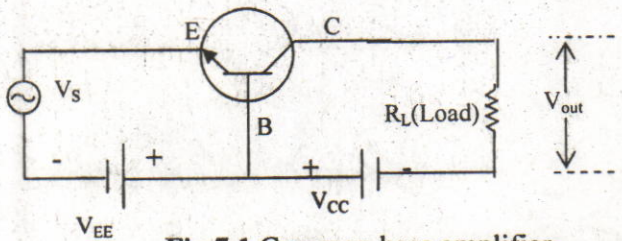

Fig.7.1 Common base amplifier

Fig.7.1 shows the circuit of a CB transistor amplifier. In the circuit, a sinusoidal source is connected in the input and a load R_L is connected in the output. The transistor is biased properly, using V_{EE} and V_{CC} sources, for faithful amplification. The transistor can be either PNP or NPN type.

Working

A sinusoidal voltage generator is used as a voltage source (V_S) to provide input signal to the amplifier. A small change in the input voltage (ΔV_{IN}) between emitter and base causes a relatively large emitter current change (ΔI_E). If α is the fraction of this current change (ΔI_E) that reaches the collector and passes through the load R_L, then we can write

$$\Delta I_C = \alpha\, \Delta I_E \qquad [\because \alpha = \frac{\Delta I_C}{\Delta I_E}]$$

Change in output voltage across load R_L is $V_{OUT} = \Delta I_C \times R_L$

$$\therefore\ V_{OUT} = \alpha\, \Delta I_E \times R_L \qquad \text{---------- (7.3.1)}$$

This is many times larger than the change in the input voltage ΔV_{IN}. Hence the voltage amplification is given by

$A_V \approx \frac{\Delta V_{out}}{\Delta Vin}$ will be grater than unity and the transistor acts as an amplifier.

If "r_e" is the dynamic resistance of the emitter –base junction, then we can write

$$\Delta V_{IN} = \Delta I_E \times r_e$$

$$A_V = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\alpha.\Delta I_E \times R_L}{\Delta I_E \times r_e}$$

$$\therefore A_V = \alpha \frac{R_L}{r_e}$$

7.4 CE Transistor Amplifier

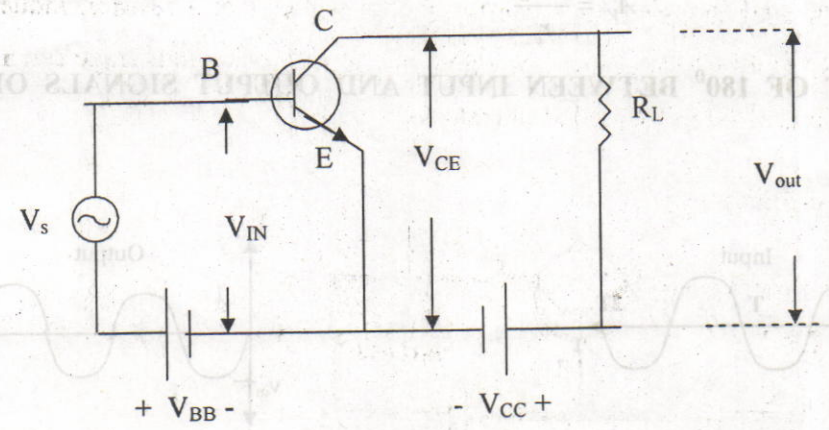

Fig.7.2 Common Emitter Amplifier

Fig.7.2 shows the circuit of a CE transistor amplifier. In the circuit, a sinusoidal source is connected in the input (i.e. between base and emitter) and a load R_L is connected in the output (i.e. between collector and emitter). The transistor is biased properly, using V_{BB} and V_{CC} sources, for faithful amplification. The transistor can be either PNP or NPN.

Working

A small voltage change in the input, ΔV_{IN} (due to signal) between base and emitter causes a relatively large change in base current ΔI_B. If β is the fraction of this current change in ΔI_B that reaches the collector and passes through the load R_L, then we can write

$$\beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{or} \quad \Delta I_C = \beta \Delta I_B$$

Hence change in the output voltage across the load R_L is given by

$$\Delta V_{Out} = \Delta I_C \times R_L$$
$$= \beta \Delta I_B \times R_L$$

This may be many times greater than the change in the input voltage. Hence the voltage amplification $A_V = \frac{\Delta V_{Out}}{\Delta V_{in}}$ will be greater than unity and the transistor acts as an amplifier.

Let r_e be the dynamic resistance of the base-emitter junction, then we can write

$$\Delta V_{in} = r_e \times \Delta I_B$$

$$\therefore A_V = \frac{V_{Out}}{V_{in}} = \frac{\beta . \Delta I_B . R_L}{r_e . \Delta I_B}$$

$$\therefore A_V = \frac{\beta R_L}{r_e}$$

PHASE SHIFT OF 180^0 BETWEEN INPUT AND OUTPUT SIGNALS OF A CE AMPLIFIER

GRAPHS

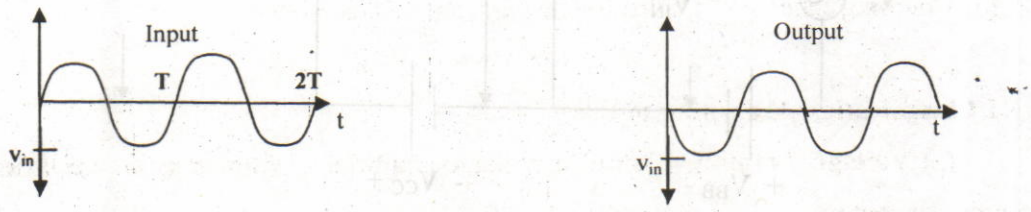

Fig 7.3 180^0 phase shift between input and output waveform

During the positive half cycles of the input signal, the signal amplitude aids the forward bias of the base-emitter junction. This increases the base current and hence the collector current due to the transistor action (since $I_C = \beta I_B$). This increase in collector current produces an increased voltage drop across R_L making the collector voltage V_{EE} less positive. This is in accordance with the equation $V_{CE} = V_{CC} - I_C R_L$.

During the negative half cycle of the input signal, the signal amplitude opposes the forward bias. This reduces the forward current and hence the collector current due to the transistor action (since $I_C = \beta I_B$). This produces a decreased voltage drop across R_L, making collector voltage V_{CE} more positive. Hence we see that the input and output voltages are at a phase of 180^0 to each other (out of phase)

Table 7.5 Differences between CE, CB, CC configurations

QUANTITY	CE	CB	CC
1.Current gain(A_I)	$\rangle 1$	$\langle 1$	$\rangle 1$
2.Voltage gain (A_V)	$\rangle 1$	$\rangle 1$	$\langle 1$
3.Input Resistance (R_I)	Medium	Lowest	Highest
4.Output Resistance (R_O)	Medium	Highest	Least
5.Phase difference between V_{IN} ,V_{OUT}	Out of phase (180^0)	In phase (0^0)	In phase(0^0)
6.Application	For AF applications	For high frequency applications	For impedance matching

7.6 Classification of Amplifiers

Amplifiers can be classified according to

(1) Use : Voltage, current, trans conductance and trans resistance

(2) Method of analysis : Small signal, large signal

(3) Frequency range : Audio frequency (A.F.)
Intermediate frequency (I.F)
Radio frequency (R.F)
Video frequency (V.F)

(4) Conduction angle (or) operating point: Class A, Class B, Class AB, Class C

(5) Coupling scheme : Direct, RC, Inductance, Transformer

7.6.1 Classification According to Use

(a) **Voltage Amplifier:** An ideal voltage amplifier is defined as an amplifier which provides an output voltage proportional to the input voltage. The proportionality factor is

independent of the magnitude of source resistance and load resistance. Also for an ideal voltage amplifier, $R_I = \infty$; $R_O = 0$

(b) Current Amplifier: An ideal current amplifier is defined as an amplifier which provides an output current proportional to the signal (or input) current. The proportionality factor is independent of magnitudes of R_S and R_L. Also $R_I = 0$; $R_O = \infty$, for an ideal current amplifier.

(c) Trance Conductance Amplifier: An ideal trans-conductance amplifier is defined as an amplifier which supplies an output current proportional to the input voltage. The proportionality factor is independent of R_S and R_L. Also $R_I = \infty$ and $R_O = \infty$ for an ideal trans conductance amplifier.

(d) Trans Resistance Amplifier: An ideal trans resistance amplifier is defined as an amplifier which supplies an output voltage proportional to the input current. The proportionality factor is independent of R_I and R_O. Also, $R_I = 0$; $R_O = 0$ for an ideal trans resistance amplifier.

7.6.2 Classification according to method of analysis

(a) Small signal amplifi When the input signal of an amplifier is so weak as to produce small fluctuations in th :tor current compared to its quiescent (working) value, the amplifier is called as *Small signal amplifier*. These amplifiers are used in the first stage of the multistage amplifiers used in Radio, TV receivers and tape recorders.

(b) Large signal amplifier: It is also known as *Power amplifier*. It is a device capable of delivering large amount of power to the load. These power amplifiers feed large power to the antenna in broadcast transmitters.

7.6.3 Classification according to frequency range of operation

(a) A.F. amplifiers: These amplifiers are used to amplify signals of frequency range 20 – 20 KHz.

(b) I.F. amplifiers: These amplifiers are used to amplify signals of frequency range greater than audio frequency but less than radio frequency

(c) R.F. amplifiers: These amplifiers are used to amplify signals of frequency range 20 KHz to 50MHz.

(d) V.H.F. amplifiers: These amplifiers one used to amplify AC signals of frequency from 50MHz to several hundred MHz. They are used in TV.

7.6.4 Classification according to conduction angle (Power Amplifiers)

These amplifiers are designed to raise both voltage and current levels of the signal. As power is nothing but the product of current and voltage, these amplifiers are often termed as

Power amplifiers. If the output signal has to be a true replica of input signal, there should not be any distortion and the signal levels are confined to the linear portion of transistor characteristics.

(a) **Class A amplifier**: A class 'A' amplifier is one in which the collector current flows for 360^0 variation of the input signal as in Fig.7.4. The operating point (Q point) lies at the centre of the load line ($\theta = 360^0$). Signal distortion is minimum in this type of amplifiers. However the power conversion efficiency of these amplifiers never exceeds 50%.

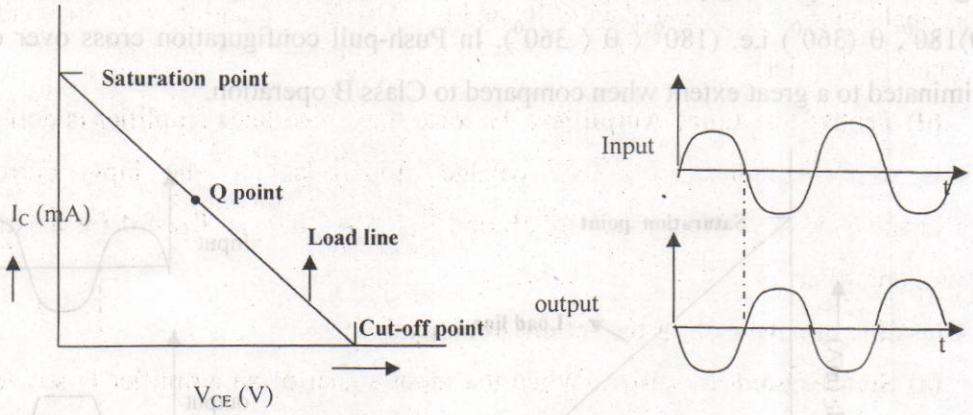

Fig.7.4 Class A operation

(b) Class B amplifier: A class B amplifier is one in which the collector current flows for only 180^0 variation of the input signal as shown in Fig.7.5. The operating point lies at the extreme end of the load line (at cut off point $\theta = 180^0$). .

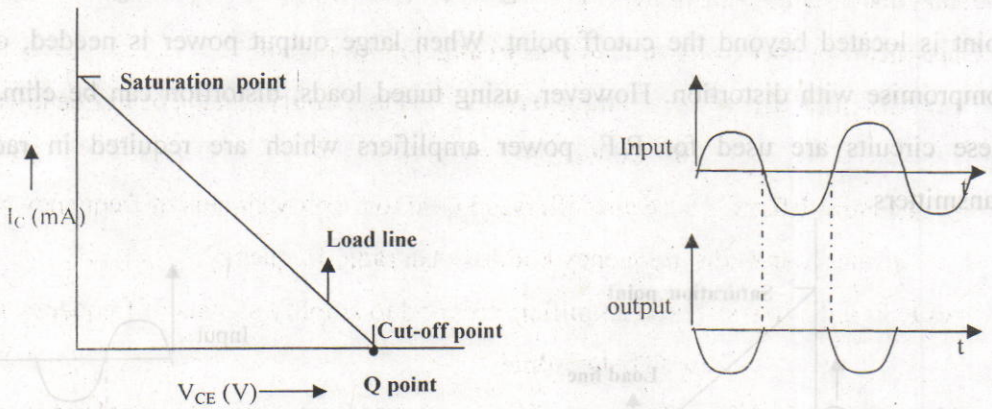

Fig.7.5 Class B operation

Class B operation is more efficient in converting D.C. power to AC power at signal frequency, but gives rise to distortion. As only signal conducts for half of the input cycle to

present the signal at the output in full, either Push-Pull configuration or Complementary symmetry type are used. Because of the fixed cut-in voltage of transistor there will be additional distortion when the signal changes its sign. This is called ***cross over distortion***. This is partially eliminated by biasing the transistor in between Class A and Class B, which is called Class AB operation.

(c) Class AB amplifier: A class AB amplifier is one in which the collector current flows for more than half cycle variation of the input signal and less than the entire cycle as shown in Fig.6.6. The operating point lies between the two extreme defined for class A and class B ($\theta \rangle 180^0$, $\theta \langle 360^0$) i.e. ($180^0 \langle \theta \langle 360^0$). In Push-pull configuration cross over distortion is eliminated to a great extent when compared to Class B operation.

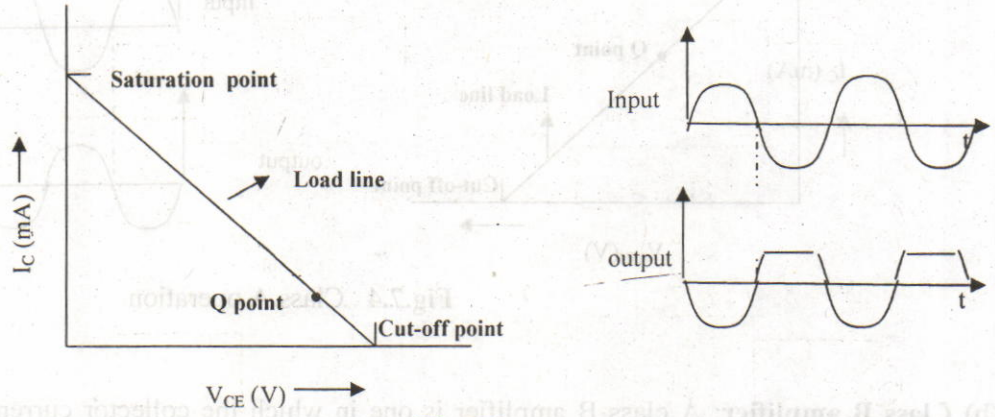

Fig.7.6

(d) Class C amplifier: A class C amplifier is one in which the collector current floes for less than half cycle variation of the input signal ($\theta \langle 180^0$) as shown in Fig.7.7. The operating point is located beyond the cutoff point. When large output power is needed, one has to compromise with distortion. However, using tuned loads, distortion can be eliminated. So these circuits are used for R.F. power amplifiers which are required in radio signal transmitters.

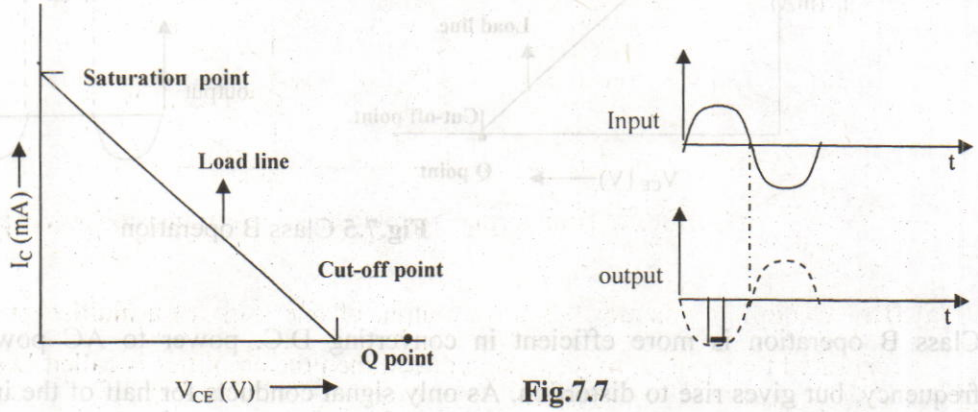

Fig.7.7

7.6.5 Classification according to coupling scheme

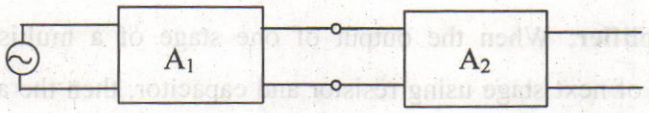

Fig.7.8a Direct Coupling

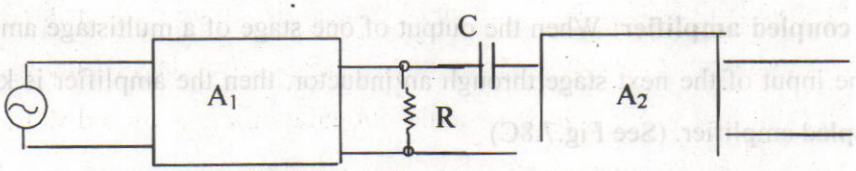

Fig.7.8b R-C Coupling

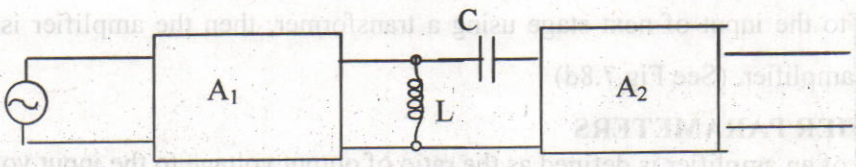

Fig.7.8C Inductance Coupling

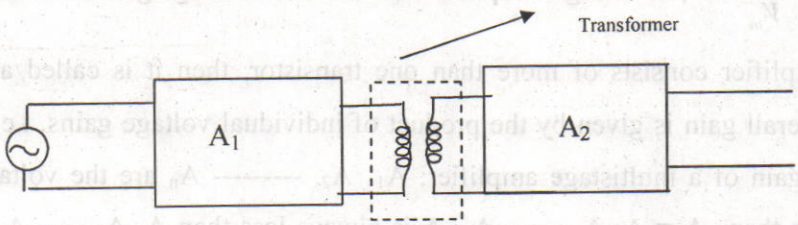

Fig.7.8d Transformer Coupling

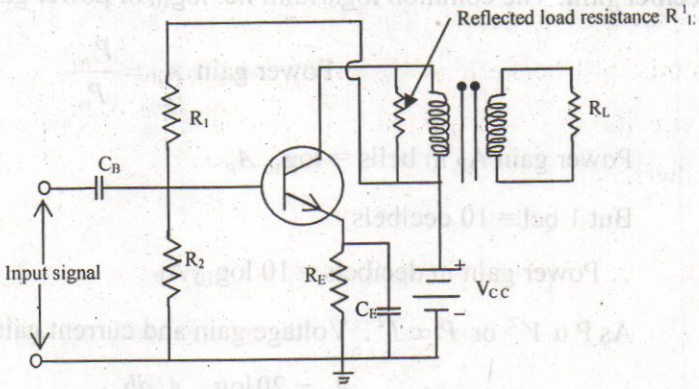

Fig.7.8e. A Transformer coupled class – A transistor power amplifier

(a) **Direct coupled scheme**: When the output of one stage of a multistage amplifier is connected to the input of next stage direct, then the amplifier is called Direct coupled

amplifier. These are used to amplify extremely low frequency signals (⟨10Hz) (See Fig.7.8a)

(b) RC-Coupled amplifier: When the output of one stage of a multistage amplifier is connected to the input of next stage using resistor and capacitor, then the amplifier is called RC-Coupled amplifier. The purpose of RC-coupling is to pass AC signal from one stage to the next stage and to block the passage of DC from one stage to the next stage. (See Fig.7.8b)

c) Inductance coupled amplifier: When the output of one stage of a multistage amplifier is connected to the input of the next stage through an inductor, then the amplifier is known as Inductance coupled amplifier. (See Fig.7.8C)

(d) **Transformer coupled amplifier**: When the output of one stage of a multistage amplifier is connected to the input of next stage using a transformer, then the amplifier is known as Transformer amplifier. (See Fig.7.8d)

7.7 AMPLIFIER PARAMETERS

Gain: The gain of an amplifier is defined as the ratio of output voltage to the input voltage.

I.e. $A_V = \frac{V_{Out}}{V_{in}}$; A_V is voltage Amplification factor or voltage gain of the amplifier.

If an amplifier consists of more than one transistor, then it is called a Multistage amplifier. Its overall gain is given by the product of individual voltage gains. i.e. if A is the overall voltage gain of a multistage amplifier; A_1 , A_2, --------- A_n are the voltage gains of individual stages then $A = A_1.A_2.\text{------}\ A_n$. A is always less than $A_1.A_2.\text{------}A_n$ due to the loading effect of next stage.

Decibel gain: The common logarithm i.e. $\log_{10}$ of power gain is known as bel power gain.

$$\therefore \text{Power gain } A_P = \frac{P_{Out}}{P_{in}}$$

Power gain A_P in bells = $\log_{10} A_P$

But 1 bel = 10 decibels

$\therefore$ Power gain in decibels = $10 \log_{10} A_P$

As $P \alpha V^2$ or $P \propto I^2$. Voltage gain and current gain are expressed as

$$A_V = 20 \log_{10} A_V db$$

Similarly $A_I = 20 \log_{10} A_I db$

Note: If each gain is expressed in db, the overall gain of a multistage amplifier will be given by A = (20 log A_1+ 20 log A_2 + 20 log A_3 +---------- + 20 log A_N) db.

Frequency response: The behavior of an amplifier at various frequencies is known as its ***frequency response***. This behavior is represented in the form of a curve.

Frequency response curve illustrates how the magnitude of voltage gain varies with frequency of the input signal. This curve is drawn by taking voltage gain values along Y- axis and the frequency along X- axis and is shown in Fig.7.9

Bandwidth: It is the range of frequency over which the gain is equal to or greater than 70.7% of the maximum gain. (Or)

The range of frequency at the limits of which its voltage gain falls by 70.7 % or 3 db from the maximum gain. The frequencies f_1 and f_2 are called ***half power frequencies*** or 3 db cut-off or Corner or band or break frequencies.

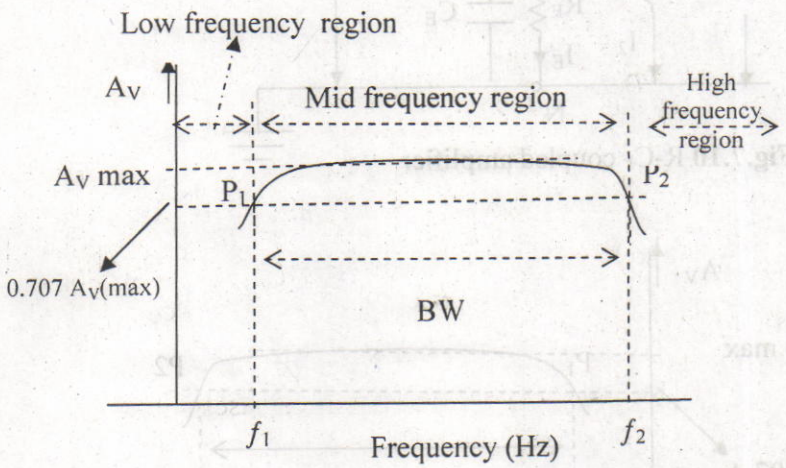

Fig.7.9 Frequency response curve

Efficiency: It is the ratio of output power delivered to the load to the input power applied to the circuit.

$$\eta = \frac{P_{Out}}{P_{in}} \times 100$$

7.8 RC-Coupled Amplifier

Fig.7.10 shows the circuit of an RC coupled CE transistor amplifier. The resistors R_1, R_2, R_E provides biasing and stabilization. The coupling capacitor C_C at the output is used to connect the output of the amplifier with the load or to another amplifier. It transmits amplified signal and blocks DC voltage. The blocking capacitor C_B is used to connect the input signal to the base and is also used to block the DC. The emitter bypass capacitor C_E offers low resistance path to the signal.

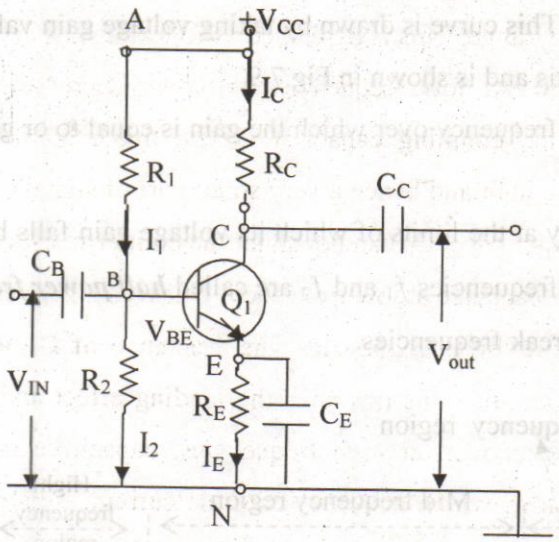

Fig.7.10 R-C- coupled amplifier

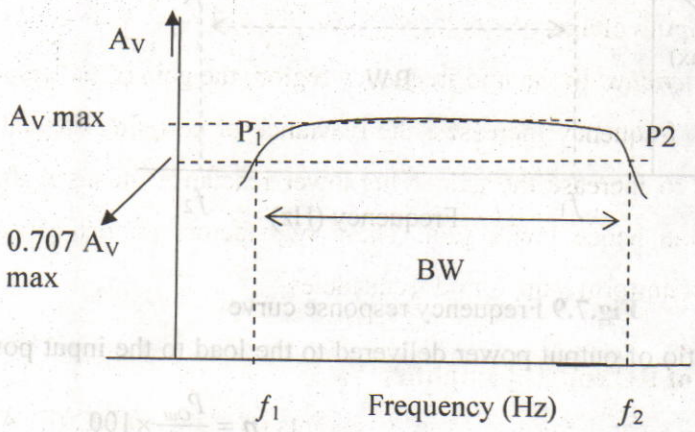

Fig. 7.11 Frequency response curve

Working

When the AC signal is applied to the base of transistor, it provides variations in the bias of emitter- base circuit, correspondingly the base current varies. This varying base current produces large variations, similar to the input signal in the collector circuit. Hence an amplified signal appears across the load. But this is 180^0 out of phase with the input signal.

Frequency Response Curve

Fig.7.11 shows the frequency response curve of an RC-coupled amplifier. It is clear from the curve that the voltage gain drops at low and high frequencies where as it is uniform over the mid frequency range. This is explained as follows.

(1) ***At low frequencies:*** At low frequencies the gain decreases with decreasing frequency due to the coupling capacitor C_C. In this region, the reactance of capacitor C_C is quite high and hence a very small part of signal will pass from one stage to the next stage. Also, C_E can not shunt the emitter resistance R_E effectively because of its large reactance at low frequency. Due to this, the voltage gain falls.

(2) ***High frequencies:*** At high frequencies, the reactance of C_C is very small and behaves as a short circuit. This increases the loading effect and serves to reduce the voltage gain. Moreover, at high frequencies, capacitive reactance of base-emitter junction is low, which increases the base current. This reduces β. Due to these reasons, the voltage gain decreases. The wiring and stray capacitance between various electrodes contributes to shunt capacitance. This also reduces the available output voltage.

(3) ***At mid frequencies:*** In the mid frequency region, the gain of the amplifier remains constant. As frequency increases, the reactance of coupling capacitor decreases, which tends to increase the gain. This lower reactance means higher loading of first stage and hence lower gain. These two factors almost cancel each other resulting in a uniform gain at mid frequencies.

7.9 Equivalent circuit of RC coupled amplifier

Equivalent circuits can be drawn from two points of view. (i) DC (ii) AC. Hence we can draw DC and AC equivalent circuits

i) DC equivalent circuit

a) Ground all AC sources (i.e. short circuit)

b) All capacitors are to be treated as open circuits.

Applying these rules, we can draw DC equivalent circuit of RC- coupled amplifier, as shown in Fig.7.12

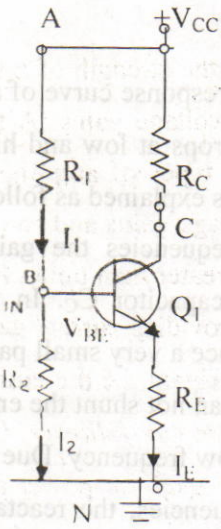

Fig 7.12 D.C. Equivalent circuit

ii) ***AC equivalent circuits***

a) Ground all DC sources (short circuit)

b) All capacitors are to be treated as short circuit.

Applying these rules, we can draw AC equivalent circuit of RC-coupled amplifier as shown in Fig.7.13; which was further simplified as shown in Fig.7.14

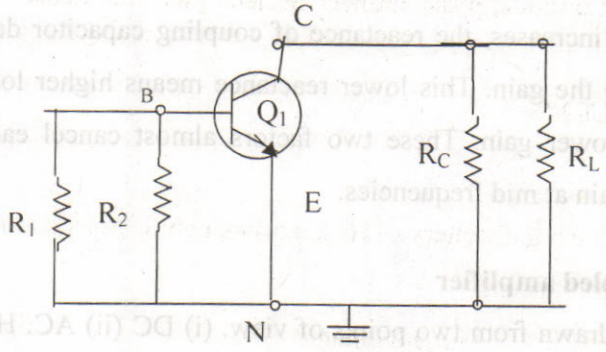

Fig.7.13 A.C Equivalent circuit

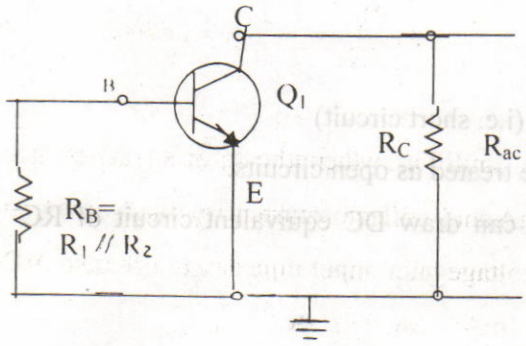

Fig 7.14 A.C Equivalent circuit

7.10 SUMMARY

A transistor can raise the strength of a weak signal and thus it acts as an amplifier. Transistor can provide large voltage gains. A transistor can be connected in three configurations; hence there are three types of amplifiers. CE, CB, CC. CE and CB transistor amplifiers can provide higher voltage gains and can be used as voltage amplifiers. CC amplifier can not provide voltage gain greater than unity. Hence it can only be used as an amplifier for impedance matching and for providing current gain. The output signal will have same magnitude and phase as that of input signal. i.e the emitter follows the changes at the input. So CC amplifier can be called as an *emitter follower*. CE Amplifier can provide both voltage gain and current gain. So it can be used for power amplification. It has input and output impedances suitable for intermediate stages of multi stage amplifiers. Amplifier performance can be understood through its frequency response curve. If voltage gain provided by a single transistor amplifier is insufficient, then more transistor amplifier stages can be used to achieve higher voltage gain. Amplifiers can be of different types depending upon use, conduction angle, coupling, frequency range, method of analysis etc. Amplifiers are mainly used in instruments, public address systems, TV, Radio receiver.

7.11 KEY TERMINOLOGY

Gain, efficiency, equivalent circuits, phase change, decibel gain, multistage amplifier parameters.

SOLVED NUMERICAL PROBLEMS

Example.1

A voltage amplifier operated using a battery of 10 V having a collector load 6kΩ. Calculate the maximum collector current.

Solution: Maximum collector current = $\frac{Supplyvoltage}{collectorload}$

$$= \frac{10}{6K\Omega} = \frac{5}{3\times10^{3}} = 1.66mA$$

Example.2

In a single stage amplifier, when the input signal changes by 0.02V, the base current changes by 10μA and collector current by 1mA of R_C = 2KΩ and R_L= 10KΩ, calculate current gain, voltage gain, input impedance, affective AC load, power gain.

Solution: Given ΔI_C = 1mA; ΔI_B = 10μA

To find: Current gain A_I, Voltage gain A_V, Effective load R_{AC}, Power gain A_P

(i) Current gain $A_I = \frac{\Delta I_C}{\Delta I_B} = \frac{1mA}{10\mu A} = \frac{1\times10^{-3}}{10\times10^{-6}} = 100$

(ii) Input impedance $R_{IN} = \frac{\Delta V_{BE}}{\Delta I_B} = \frac{0.02}{10\mu A} = \frac{0.02}{10\times10^{-6}} = 2000\Omega = 2K\Omega$

(iii) Effective load $R_{ac} = R_C // R_L$

$$= \frac{R_C \times R_L}{R_C + R_L} = \frac{2\times10^3 \times 10\times10^3}{(2+10)10^3} = \frac{20\times1000}{12} = 1.66K\Omega$$

(iv) Voltage gain $A_V = A_I \frac{R_{ac}}{R_{in}} = \frac{100\times1.66\times10^3}{2\times10^3} = 83$

(v) Power gain $A_P = A_I X A_V$

100X83 = 8300

Example.3

In a single stage transistor amplifier used in CE configuration, the collector resistance R_C = 5kΩ; and load resistance R_L = 5kΩ; β= 100 and the input resistance R_I= 2.5 KΩ. Find the output voltage if the input is 1mV.

***Solution*:**

Given $R_C = 5k\Omega$ $R_L = 5k\Omega$

$5X10^3\Omega$; $5X10^3\Omega$;

$\beta = 100$; $V_{IN} = 1mV$; $R_i = 2.5X10^3\Omega$

To find

V_{OUT}?

We know that voltage gain $A_V = \frac{V_{Out}}{V_{in}} \Rightarrow V_{Out} = A_V . V_{in}$

But $A_V = \frac{\beta R_{ac}}{R_{in}}$

$R_{ac} = ACload = R_C // R_L = 5k\Omega // 5K\Omega = 2.5K\Omega$

$\therefore A_V = \frac{100\times2.5\times10^3}{2.5\times10^3} = 100$

$V_{OUT} = A_V X V_{IN}$

$= 100x\ 1x10^{-3}$

$=0.1V$

7.12 SELF ASSESSMENT QUESTIONS

(I) Long answer questions

1. Write about the classification of amplifiers, based on different factors. Define the terms: voltage gain, current gain, input and output resistances.
2. Draw the circuit if RC coupled CE amplifier and explain its frequency response at various frequencies.
3. Discuss the working of CE transistor amplifier and also explain how it produces a phase shift of 180^0 .
4. Explain how one can draw AC and DC equivalent circuits of a RC coupled CE amplifier.

(II) Short answer questions

1. Compare the characteristics of three amplifier configurations
2. How a CE amplifier produces a phase shift of 180^0 between input and output signals? Explain.
3. Draw the frequency response curve of RC coupled amplifier and mark the low, mid, and high frequency regions.
4. Differentiate between voltage gain and decibel voltage gain
5. Explain how a transistor raises the strength of a weak signal
6. Give the classification of amplifiers based on conducting angle
7. What are the conditions under which a transistor can act as an amplifier?

(III) Numerical problems

1. What is the voltage gain of a CE amplifier if its $R_{IN} = 2.5\ k\Omega$, ac load $R_{AC} = 5k\Omega$; $\beta =$ 50 [Ans: 100]
2. In the CE transistor CE amplifier, if $R_C = 10k\Omega$, $R_L = 10K\Omega$; $\beta = 100$, $R_{IN} = 2.5k\Omega$, find the output voltage for an input voltage of 1mV [Ans: 200mV]
3. In a single stage CE amplifier, $R_C = 10K\Omega$, $R_{IN} = 2k\Omega$, $\beta = 50$, $R_L = 20\ k\Omega$. find voltage gain [Ans: 166.7]

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UNIT -III

LESSON 8

FEEDBACK AMPLIFIERS

OBJECTIVES OF THE LESSON

This lesson explains you the basic idea of feedback, various types of feedback: (positive and negative feedback), their advantages and disadvantages, gain of an amplifier with the inclusion of feedback. Effect of feedback on various parameters of an amplifier like gain, noise, bandwidth, input and out put impedances. It also describes the working of emitter follower, derivation of its parameters; concept of Darlington pair.

STRUCTURE OF THE LESSON

8.1 INTRODUCTION

The process of returning a part of output voltage or current of an amplifier to its input terminals is known as *Feedback*. There are two types of feedback. These are known as positive feedback and negative feedback. Positive feedback increases the gain whereas negative feedback reduces the gain. But negative feedback has so many advantages as compared to positive feedback. They are (1) Any of the four basic amplifier types (voltage, current, transconductance and trans resistance) may be improved by the proper use of negative feedback (2) Any of the four basic amplifier configurations may be made to exhibit the properties of the other, by the proper application of negative feedback. (3) The transfer gain of the amplifier with feedback can be stabilized against variations of the parameters of the transistor or parameters of other active devices. (4) Significant improvement in the frequency response of the feedback amplifier by proper use of negative feedback (5) Reduction of distortion and noise. Positive feedback is used to produce oscillations, whereas negative feedback is used mostly in amplifiers for stable operation.

FEEDBACK AMPLIFIER

8.2 CONCEPT OF FEEDBACK: H.S Black first proposed the principle of feedback in electronic circuits (amplifiers) in 1934.

The process of returning a part of output signal and feeding it back to the input terminals again is called *Feedback*. The use of feedback can make the characteristics of a practical amplifier to approach those of ideal amplifiers.

Fig.8.1 shows the block diagram of a basic amplifier. Here v_i is the input signal and v_o is the output signal. The voltage gain of the amplifier A is given by

$$A = \frac{v_0}{v_i}$$

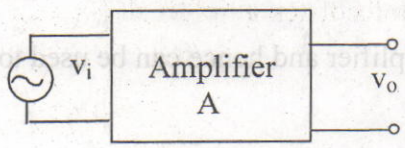

Fig.8.1

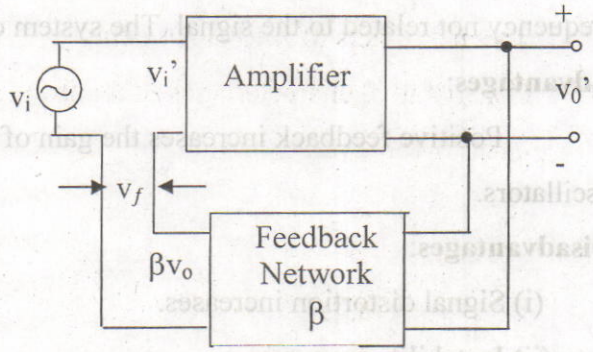

Fig.8.2

In this amplifier, the input does not know what is happening at the output. If, due to some reason, the output changes, net input remains unaffected, such a system is called O*pen loop* or *Non feedback* system.

In Fig 8.2, the output of the amplifier is fedback to the input through a feedback network or a β-network. A fraction βv_o of the output voltage is fedback to the input. This changes the net input voltage to the amplifier. Thus the input is modified by the output. The input knows at every instant what the output is. Such a system is called a *Closed loop* or *Feedback* system.

The gain with feedback is called *Closed loop gain* A_{fb} while the gain without feedback is called *open loop gain* A.

8.3 TYPES OF FEEDBACK

Depending upon whether the feedback signal aids or opposes the input signal, there are two basic types of feedback in amplifiers: Positive and Negative.

8.3.1 POSITIVE FEEDBACK or REGENERATIVE FEEDBACK

When the feedback signal (voltage or current) is in phase with the input signal and thus aids it, it is called *Positive Feedback.*

Let v_f be the feedback voltage which is in phase with the input voltage vi; then the net input voltage to the amplifier is $vi = vi^1 + v_f$. Since the net input to the amplifier is increased, the output of the amplifier also increases from v_o to vo^1. In other words, the gain of the amplifier increases because of the positive feedback. Due to this regenerative process the signal amplitude increases and enters into non linear part of transistor characteristics thereby a severe distortion occurs in signal shape. The original input becomes negligible when compared to the feedback signal, thereby make the system to work as an oscillator at a frequency not related to the signal. The system ceases to work as an amplifier.

Advantages:

Positive feedback increases the gain of the amplifier and hence can be used to design oscillators.

Disadvantages:

(i) Signal distortion increases.

(ii) Instability increases.

8.3.2 NEGATIVE FEEDBACK or DEGENERATIVE FEEDBACK

When the feedback signal is out of phase with the input signal and thus opposes it, the effective input signal decreases.. So, it is called Negative feedback or inverse feedback or degenerative feedback.

Let v_f be the feedback voltage, which is in phase opposition to the input voltage v_i, then the net input voltage to the amplifier is $v_i' = v_i - v_f$. Since the net input to the amplifier is reduced, the output of the amplifier also decreases from v_o to v_o'.

In other words, the gain of the amplifier reduces because of the negative feedback.

ADVANTAGES

(i) Stability in gain

(ii) Improves the overall characteristics of an amplifier

(iii) Reduction in distortion and noise

(iv) Improves frequency response

(v) Increased bandwidth.

(vi) Modifies input and out put impedances.

DISADVANTAGE: It reduces the gain of the amplifier.

8.4 OTHER CLASSIFICATION OF FEEDBACK

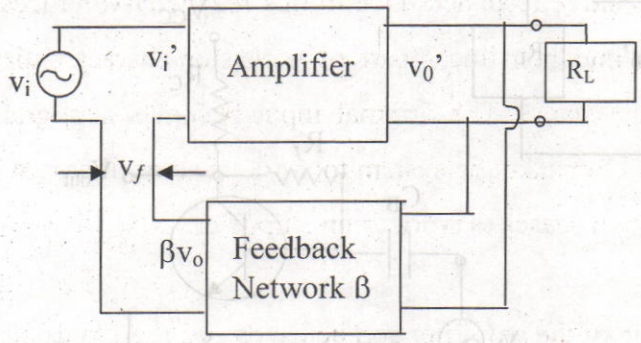

Fig.8.3 Series voltage feed back

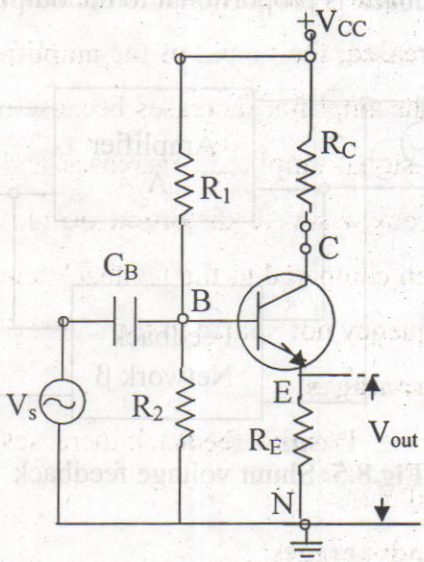

Fig.8.3a Voltage series feedback amplifier

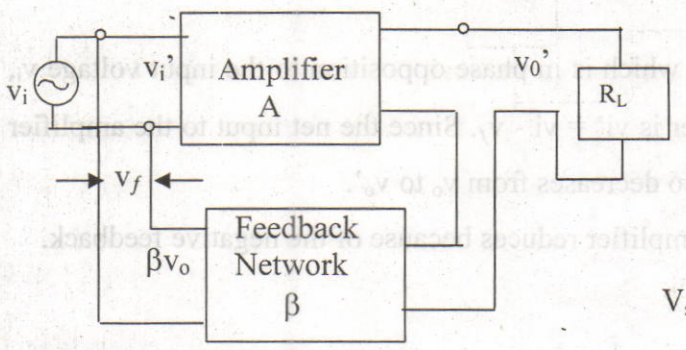

Fig 8.4 Series current feedback

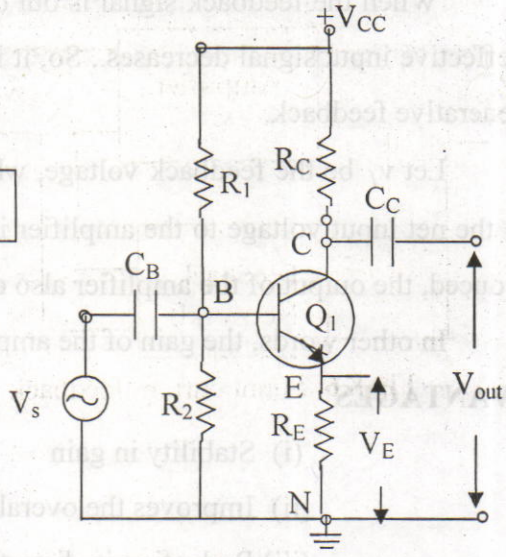

Fig.8.4a Current series feedback amplifier

The feedback can also be classified as voltage feedback or current feedback. In case of voltage feedback, the signal fe : is proportional to the output voltage, whatever may be the load impedance. In case of current feedback, the signal fedback is proportional to the output current, whatever may be the load impedance. In case of current feedback, the signal feedback is proportional to the output current, whatever may be the load impedance.

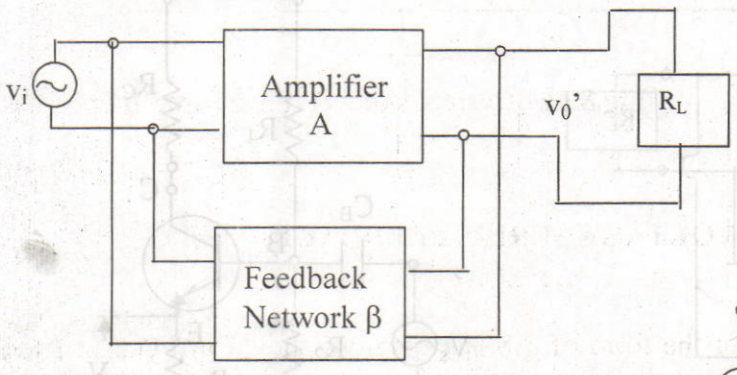

Fig.8.5 Shunt voltage feedback

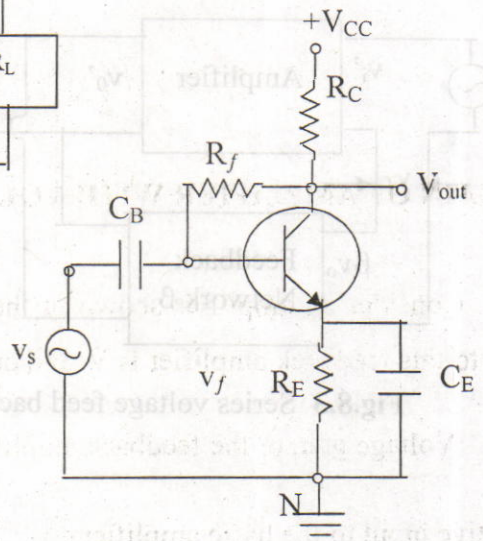

Fig.8.5a Voltage shunt feedback amplifier

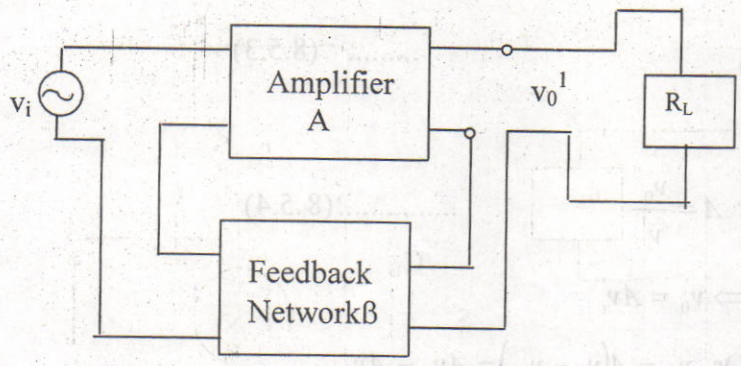

Fig 8.6 Shunt current feedback

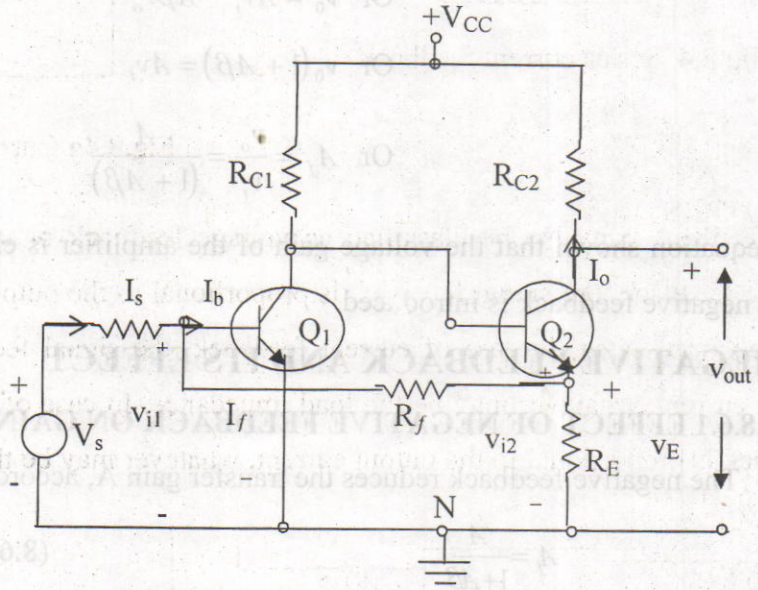

Fig.8.6a Current shunt feedback amplifier

8.5 GAIN OF AMPLIFIER WITH VOLTAGE SERIES FEEDBACK

Consider an amplifier shown in the form of a block diagram shown in Fig.8.5. The input to this feedback amplifier is V_i and output is Vo^1.

Voltage gain of the feedback amplifier $A_f = \frac{v_0}{v_i}$ -----(8.5.1)

Effective input to the basic amplifier $= v_i$

But $v_i = v_i - v_f$ ..... (8.5.2)

Feedback voltage $v_f = \beta v_0'$ ..... (8.5.3)

β is feedback factor

Internal gain of the basic amplifier $A = \frac{v_0'}{v'}$ .....(8.5.4)

$$\Rightarrow v_0' = Av_i'$$

$$\text{Or } v_0' = A(v_i - v_f) = Av_i - Av_f$$

$$\text{Or } v_0' = Av_i - A\beta v_o'$$

$$\text{Or } v_0'(1 + A\beta) = Av_i$$

$$\text{Or } A_f = \frac{v_o'}{v_i} = \frac{A}{(1 + A\beta)}$$

This equation shown that the voltage gain of the amplifier is changed by the factor (1+Aβ) when negative feedback is introduced.

8.6 NEGATIVE FEEDBACK AND ITS EFFECT

8.6.1 EFFECT OF NEGATIVE FEEDBACK ON GAIN

The negative feedback reduces the transfer gain A, according to the relation

$$A_f = \frac{A}{1+A\beta} \qquad (8.6.1.1)$$

i.e, $A_f < A$

Suppose the gain A is very large, so that Aβ>>1, then

$$A_f = \frac{A}{A\beta} = \frac{1}{\beta}$$

Thus the gain of the feedback amplifier is made independent of the transfer gain A. The gain with feedback A_f only depends on β i.e. on the properties of the feedback network and is independent of transistor parameters. This network consists of stable elements like resistors and capacitors and hence the gain is stabilized. The condition for this stabilization is that Aβ>>1.

8.6.2 EFFECT OF NEGATIVE FEEDBACK ON DISTORTION AND NOISE

Distortion:

Negative feedback reduces the amplifier distortion in the same magnitude as gain. Suppose that a large amplitude signal is applied to a stage of an amplifier. Due to this, the operation of the device extends slightly beyond its range of linear operation and hence the output signal is slightly distorted. If now negative feedback is introduced, the input signal will be increased by the same amount by which the gain is reduced. Hence the output signal amplitude remains the same.

$$D_f = \frac{D}{1+D\beta};\ D_f < D$$

where $D_f \rightarrow$ Distortion with feedback

$D \rightarrow$ Distortion without feedback

The feedback can also be classified as voltage feedback or current feedback. In case of voltage feedback, the signal feedback is proportional to the output voltage, whatever may be the load impedance. In case of current feedback, the signal fedback is proportional to the output current, whatever may be the load impedance. In case of current feedback, the signal feedback is proportional to the output current, whatever may be the load impedance.

Noise:

Negative feedback reduces the noise in the same magnitude as the gain according to

$$N_f = \frac{N}{1+A\beta} \Rightarrow \quad N_f < N$$

Where $N_f \rightarrow$ Noise with feedback

$N \rightarrow$ Noise without feedback

8.6.3 EFFECT OF NEGATIVE FEEDBACK ON BANDWIDTH

The negative feedback affects the cut off frequencies just like gain. The lower cutoff frequency f_1 is lowered by a factor of (1+Aβ) and upper cut off frequency f_2 is raised by the same factor (1+Aβ). Since $f_1 << f_2$, the bandwidth can be taken as f_2-$f_1 \cong f_2$. Thus if negative feedback is employed in an amplifier, its bandwidth increases by the same factor (1+Aβ) by which its gain reduces as shown in Fig.8.7.

Hence

$$f_{1f} = \frac{f_1}{1 + A\beta}$$

$$f_{2f} = f_2 (1 + A\beta)$$

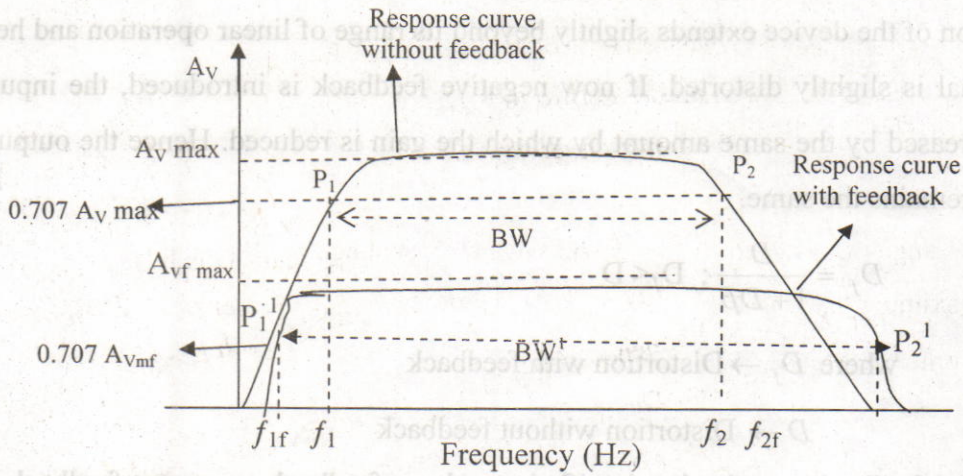

Fig. 8.7 Frequency response curve

8.6.4 EFFECT OF NEGATIVE FEEDBACK ON INPUT RESESTANCE

The effect of negative feedback on input resistance depends upon the way in which the output is fedback to the input.

If the output signal (voltage or current) is fedback in series with the input, then the input current decreases. The effective input resistance decreases according to

$$R_{if} = R_i(1 + A\beta)$$

If the output signal (current or voltage) is fed back to the input in parallel, then the effective input resistance decreases according to, $R_{if} = \dfrac{R_i}{(1 + A\beta)}$

8.6.5 EFFECT OF NEGATIVE FEEDBACK ON OUTPUT RESISTANCE

The effect of negative feedback on output resistance depends upon the quantity that is fedback to the input from the output.

If the output voltage is returned to the input (either in series or in parallel), the output resistance decreases according to

$$R_{of} = \frac{R_o}{1 + A\beta}$$

If the output current is returned to input (either in series or in parallel), the output resistance increases according to

$R_{of} = R_o(1+A\beta)$

8.7 THE NET EFFECTS OF FEEDBACK CIRCUITS

The net effects of feedback circuits are consolidated in Table 8.1

Table 8.1

Parameter	Voltage series feedback	Voltage shunt feedback	Current Series feedback	Current Shunt feedback
Feedback voltage/ Current	$V_f = \beta V_o$	$I_f = \beta V_o$	$V_f = \beta V_o$	$I_f = \beta V_o$
Gain	$A_{vf} = \frac{A_V}{1+A_V\beta}$	$R_{mf} = \frac{R_m}{1+R_m\beta}$	$g_{mf} = \frac{g_m}{1+g_m\beta}$	$A_{if} = \frac{A_i}{1+A_i\beta}$
R_{if}	$R_i[1+A_V\beta]$	$\frac{R_i}{1+\beta R_m}$	$R_i[1+g_m\beta]$	$\frac{R_i}{1+A_i\beta}$
R_{of}	$\frac{R_o}{1+A_V\beta}$	$\frac{R_o}{1+\beta R_m}$	$R_o[1+g_m\beta]$	$R_o[1+A_i\beta]$

Characteristics of negative feedback amplifier

i) The feedback signal is in phase opposition to the input signal

ii) The effective input signal is the difference of source and feedback signals i.e $V_i = V_s - V_f$.

iii) The gain with feedback is always less than the open loop gain.

iv) Bandwidth increases. The gain bandwidth remains the same.

v) Stability increases

vi) Noise and distortion decreases.

vii) Input impedance and output impedances are modified.

8.8. COMPARITIVE CHARACTERISTICS OF FEEDBACK AND NON FEEDBACK AMPLIFIERS

Parameter	Amplifier without feedback	Amplifier with feedback
Gain	A	$A_f = \frac{A}{1+A\beta}$
Input resistance	R_i	$R_{if} = R_i (1+A\beta)$
Output resistance	R_o	$R_{of} = \frac{Ro}{1+A\beta}$
Band width	B.W	$(B.W_f) = B.W [1+A\beta]$
Noise	N	$N_f = \frac{N}{1+A\beta}$
Non linear distortion	D	$D_f = \frac{D}{1+A\beta}$

8.9 EMITTER FOLLOWER

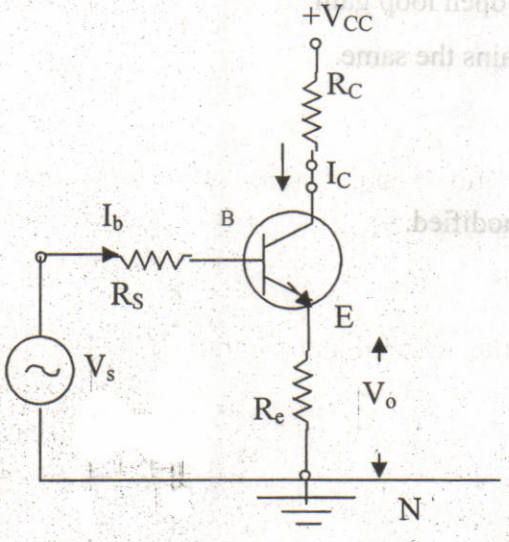

Fig.8.8 Emitter follower

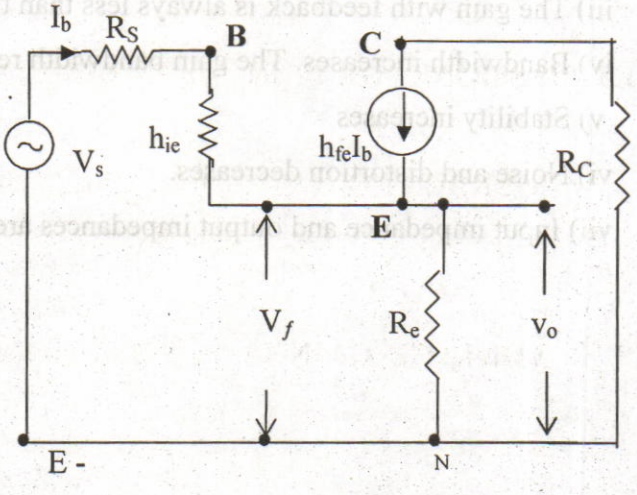

Fig.8.9 Hybrid model for Emitter follower

A special case of the CE amplifier with the emitter unbypassed is the common collector amplifier or Emitter follower. This is shown in Fig.8.8. The output voltage is taken across the emitter resistor R_e and the feedback factor is unity. Thus the emitter follower exhibits 100% negative feedback. This is a case of voltage series feedback, since the voltage developed in the output is in series with the input voltage as far as the base emitter junction is concerned.

Working

The operation of emitter follower is the same as that of common emitter configuration. When the base current is Ico, the emitter current will be zero and no current will flow in the load. As the transistor is brought out of this back biased condition by increasing the magnitude of the base current, the transistor will pass through the active region and eventually reach saturation. In this condition, all the supply voltage, except for a very small drop across the transistor, will appear across the load.

Analysis

Fig.8.8 is the emitter follower circuit. It is so called because its voltage gain is close to unity and hence a change in base voltage appears as an equal change in the output voltage developed across Re. In other words, the emitter follows the input signal. Fig.8.9 shows the small signal equivalent circuit.

EXPRESSIONS FOR VARIOUS PARAMETERS

1. **CURRENT GAIN** (Ai): It is defined as the ratio of output current to input current.

$$A_f = \frac{I_0}{I_i} = \frac{I_i + h_{fe} I_i}{I_i} = 1 + h_{fe} \qquad \text{..... 8.9.1}$$

2. **VOLTAGE GAIN** (Av): It is defined as the ratio of output voltage to the input voltage.

$$A_{vs} = \frac{V_0}{V_s}$$

To find the voltage gain A_{vs} without feedback, we connect the front side of Vs to emitter E. Then

$$V_S = (R_S + h_{fe})I_i \quad \text{..... 8.9.2}$$

$$V_o = h_{fe} R_e I_i \quad \text{..... 8.9.3}$$

and

$$A_{VS} = \frac{V_0}{V_S} = \frac{h_{fe} R_e I_i}{(R_s + h_{ie}) I_i}$$

or

$$A_{VS} = \frac{h_{fe} R_s}{R_S + h_{ie}} \quad \text{..... 8.9.4}$$

$$\therefore A_{VSf} = \frac{A_{VS}}{1 + \beta A_{VS}} = \frac{\dfrac{h_{fe} R_e}{R_S + h_{ie}}}{1 + \dfrac{h_{fe} R_e}{R_S + h_{ie}}}$$

$$A_{VF} = \frac{h_{fe} R_e}{R_S + h_{ie} + h_{fe} R_e} \quad \text{.....8.9.5}$$

3. INPUT RESISTANCE (R_i)

It is defined as the ratio of input voltage to the input current.

$$R_S = \frac{V_S}{I_i} = h_{ie} + R_S \quad \text{..... 8.9.6}$$

Now with R_S=0, Eq. (8.9.3) becomes

$$A_{VS} = \frac{h_{fe} R_e}{h_{ie}}$$ and Eq.(8.9.5) becomes $R_i = h_{ie}$

Input resistances, $R_{if} = R_i (1 + A_{VS}\beta)$

Or

$$R_{if} = h_{ie}\left(1 + \frac{h_{fe} R_e}{h_{ie}}\right) \quad \text{(since } \beta = 1\text{)}$$

$$R_{if} = h_{ie} + h_{fe} R_e \quad \text{..... 8.9.7}$$

4. OUTPUT RESISTANCE (R_o)

It is defined as the ratio of output voltage to the output current.

$$R_0 = \frac{V}{I}$$

Where V → Open circuit output voltage

I → Short-circuit output current.

Hence output resistance without feedback is infinite.

$$\therefore R_{of} = \frac{R_0}{1 + A_{vs}\beta} = \frac{\lim_{Re\to\infty} R_e}{1 + \beta \lim_{Re\to\infty} A_{vs}}$$

$$= \lim_{Re\to\infty} \left[\frac{R_e}{1 + h_{fe} \dfrac{R_e}{R_s + h_{ie}}} \right]$$

$$= \lim_{Re\to\infty} \frac{R_e (R_s + h_{ie})}{R_s + h_{ie} + h_{fe} R_e}$$

$$= \frac{R_s + h_{ie}}{h_{fe} + \lim_{Re\to\infty} \left[\dfrac{R_s + h_{ie}}{R_e} \right]}$$

. Hence $R_{of} = \dfrac{R_s + h_{ie}}{h_{fe}}$

APPLICATIONS

1. This circuit can be used for impendence matching in CROs video stage of a T.V receiver etc.
2. This circuit can be used as a buffer stage and can also be used to increase the power level of the signal.
3. Its very high input resistance and very low output resistance can be used to match high impedance signal source to low impedance load without loading signal source.

8.10 DARLINGTON PAIR

For very weak signal sources for which even emitter follower input impedance >500KΩ is a burden, we have to provide an amplifier with much higher input impedance larger than 500KΩ. Darlington pair amplifiers are used in such cases.

Darlington pair is the name given to a pair of similar transistors in which the collectors of two transistors are tied together and the emitter of one is directly connected to the base of the other. It is commercially mounted in a single package that has only three leads base, collector and emitter as shown in Fig.8.10. In other words, this circuit consists of two cascaded emitter followers with infinite emitter resistance in the first stage as shown in Fig.8.11. The voltage gain of this circuit is close to unity and current gain is very high.

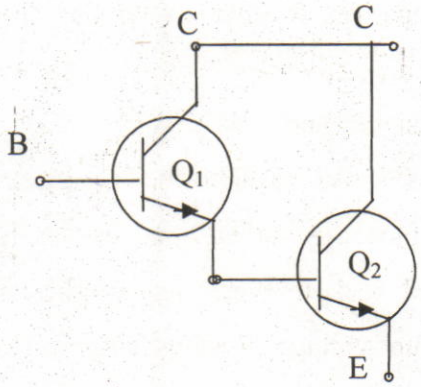

Fig 8.10 Darlington pair

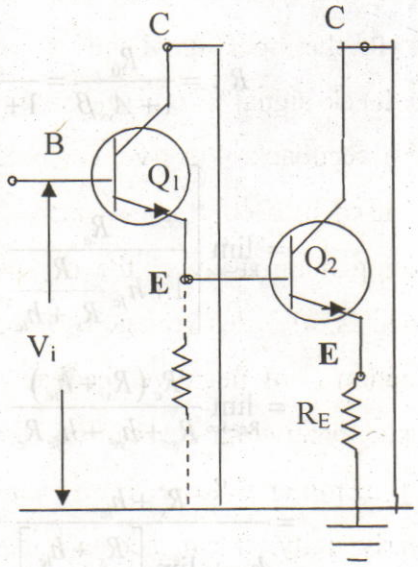

Fig 8.11 Darlington pair Amplifier

MERITS

1. Darlington emitter follower has high input impedance than that of a single stage emitter follower.
2. It has voltage gain less close to unity compared to a single stage emitter follower.
3. Darlington pair can be readily formed from two adjacent transistors in an integrated circuit.
4. It has a high impedance transformation capability.

DISADVANTAGE

The overall leakage current of Darlington pair is high because the leakage current of the first transistor is amplified by the second.

8.11 SUMMARY

When a part of the output voltage (or current) of an amplifier is given back to the input circuit, feedback is said to exist. Feedback is a concept or method to obtain the desired characteristics; generally feedback is included in the system. The advantages of feedback system are: high accuracy, fast response, independence of operating conditions, flexibility, improved stability. Depending upon the feedback signal aids or opposes the input signal, there are two types of feedback: (i) Positive (2) negative. When the feedback signal is in phase with the input signal and thus aids it, it is called positive feedback. In the other case, if the feedback signal is out of phase with the input signal and thus opposes it, it I s called negative feedback. Positive feedback is sometimes called regenerative feedback; and is mostly used in oscillators. Negative feedback is some times called degenerative feedback. Depending upon the way the output energy is feed back to the input, amplifiers can be classified as, a) series voltage b) series current c) shunt voltage, d) shunt current. Due to the introduction of negative feedback, amplifier parameters like in put resistance, out put resistance, bandwidth etc. can be controlled as we desire . Noise and distortion can also be reduced . Emitter follower is an example of feedback amplifier. Its voltage gain is less than but nearly unity. It can act as buffer amplifier with high input impedance . Still higher impedance can be obtained by connecting two such emitter followers in cascade. This arrangement is known as darling ton pair .

8.12 KEY TERMINOLOGY

Feedback, positive and negative feedback, voltage gain; emitter follower, bandwidth, distortion, noise, Darlington pair.

SOLVED NUMERICAL PROBLEMS:

Example1

Calculate the gain of a negative feedback amplifier with an internal gain A=100 and Feedback factor β=1/10

Solution:

Given $A = 100\ \beta = 1/10 = 0.1$

To find $A_f = ?$

We know that $A_f = \frac{A}{1+A\beta} = \frac{100}{1+100x\frac{1}{10}} = \frac{100}{11} = 9.09$

Example.2

An amplifier with Z_i = 1KΩ has a voltage gain A = 100. If a negative feed back of β = 0.01 is applied to it , what shall be the input impedance of the feedback amplifier?

Solution:

Given $Z_i = 1K\Omega$; β = 0.01 ; A = 100

To find $Z_{if} = ?$

$$Z_{if} = Z_i(1+\beta A) = 1(1+0.01\times 100) = 2k\Omega$$

Example 4

We have an amplifier of 60dB gain. It has an output impedance Z_0 = 12kΩ. It is required to modify its output impedance to 600 Ω. by applying negative feedback. Calculate the values of feedback factor, percentage change in the overall gain for 10% change in the gain of the internal amplifier?

Solution :

Given A=60dB =

Z_o = 12k Ω

Z_{of} = 600

To calculate Feedback factor βA =?

$$Z_{of} = \frac{Z_o}{1+A\beta}$$

$$A\beta = \frac{Z_o}{Z_{of}} - 1$$

$$= \frac{12000}{600} - 1 = 20 - 1 = 19$$

Example 5

The gain of the amplifier is 100 and its bandwidth is 400 KHz. If the 5% feedback is introduced, find the gain and bandwidth?

Solution:

Given A= 100

B.W. = 400 KHz

Feedback ratio = 0.05

To find gain A_{fb} with feedback and B.W.' bandwidth with feedback

$\beta A = 0.05 \times 100 = 5$

$$A_{fb} = \frac{A}{1+A\beta} = \frac{100}{1+5} \approx 17$$

$$B.W.' = B.W.(!+A\beta) = 400 \times (1+5) = 24000kHz$$

Example.6

In a negative feedback amplifier, the gain without feedback is 100, feedback ratio is 1/25 and input voltage is 50mV. Calculate 1). Gain with feedback 2) Feedback factor 3) Output voltage 4) Feedback voltage 5) New input voltage.

1) Gain with feedback

$$A_f = \frac{A}{1+\beta A} = \frac{100}{1+\frac{1}{25}\times 100} = 20$$

2) Feedback factor $\beta A = \frac{1}{25} \times 100 = 4$

3) Output voltage $V_o' = A_f V_i = 20 \times 50mV = 1V$

4) Feedback voltage $\beta V_o' = \frac{1}{25} \times 1 = 0.4V$

5) New increased input voltage

$$V_i' = V_i(1+\beta A)$$

$$= 50(1+\frac{1}{25}\times 100) = 250mV$$

Example 7

The basic amplifier has a voltage gain of 40dB with the application of negative feedback, the gain is reduced to 20dB. Find the gain with and without, feedback. Also find the feedback ratio?

Solution

$A_v = 40dB$ i.e. $20 \log A_v = 40$;

Therefore $\log A_v = 40/20 = 2$;

Or $A_v = 10^2 = 100$

Given $A_{vf} = 20$ dB i.e, $20 \log A_{vf} = 20$;

Or $A_{vf} = 10$,

We have $A_{vf} = \dfrac{A_v}{1 + A_v\beta}$

$$10 = \frac{100}{1 + 100 \times \beta}$$

Solving for β, we get $\beta = 0.09$

Example 8

An amplifier has a gain of 120dB and it has bandwidth of 140 KHz with lower 3dB frequency of 20 kHz and upper 3dB frequency 160 KHz. Find the gain, lower and upper 3dB frequencies if 5% negative feedback is introduced?

Solution:

Given $20\log A_v = 120$ or $A_v = 10^6$

BW= 149kHz; $f_L = 20kHz$; $f_H = 160kHz$; $\beta = 0.05$

We have $A_{vf} = \dfrac{A_v}{1 + A_v\beta}$

$$A_{vf} = \frac{10^6}{1 + \beta \times 10^6} = \frac{10^6}{1 + 0.05 \times 10^6} = \frac{10^6}{5 \times 10^4} = 20$$

$$f_{lf} = \frac{f_l}{1 + \beta \times A_v} = \frac{20 \times 10^3}{1 + 0.05 \times 10^6} = \frac{20 \times 10^3}{5 \times 10^4} = 0.4Hz$$

$$f_{Hf} = f_H(1 + \beta A) = 160kHz \times 0.05 \times 10^6 = 8MHz$$

SELF ASSESSMENT QUESTIONS

(1)Long answer questions

1. What is feedback? Discuss about the positive and negative feedback. Obtain an expression for the voltage gain of an amplifier with negative feedback?
2. Discuss the effect of negative feedback on gain, input resistance, bandwidth distortion and

noise?

3. What is an emitter follower? Explain its working , give its analysis?
4. Draw the circuit of emitter follower? Derive an expression for 1. Current gain 2.Voltage Gain 3. input resistance 4.Output resistance.
5. Explain the action of emitter follower and Darlington pair?

(2) Short answer questions

1. Obtain an expression for voltage gain of negative feedback amplifier?
2. Mention the advantages and disadvantages of negative feedback?
3. Draw the circuit of darling-ton pair and describe its action?
4. Discuss the effect of negative feedback on bandwidth of an amplifier?
5. Discuss how voltage gain is stabilized by the use of negative feedback?

NUMERICAL PROBLEMS

1.Calculate the average gain of negative feedback amplifier circuit having internal gain A=100 and feedback factor β = 0.1. [Ans; 9.09]

2.An amplifier has internal gain A of 200. Its output impedance is 1k Negative feedback is introduced in the circuit (β =0.02) . Calculate the output impedance of the feedback amplifier? [Ans; 200]

3. What should be the feedback factor of the negative feedback circuit applied to an amplifier of an internal gain A = 180 and Zi = 250 Ω in order to increase the input impedance to 2kΩ ? . [Ans: 0.0389]

4.A feedback amplifier has an internal gain A = 40dB and feedback factor 0.05 of the input impedance of this circuit is 12KΩ , what would have been the input impedance of the amplifier if feedback was not present. [Ans; 0.0389]

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UNIT - III **LESSION-9**

OSCILLATORS-I

OBJECTIVES OF THE LESSION

This lesion explains you the concept and importance of oscillators; Various conditions to be satisfied to produce oscillations; Sinusoidal oscillators either by using RC- networks, Ex Wein bridge, phase shift oscillators; or by using LC-networks, Ex: Hartley and Colpitts oscillators; This lesion also discuses about the Crystal oscillator, and its advantages; frequency stability.

STRUCTURE THE LESSION

9.1 INTRODUCTION

Oscillator may be defined as an electronic circuit that converts energy from a DC source into a periodically varying electrical output. Amplifiers with excessive regenerative feedback produce oscillations at a frequency that satisfies Bhakhausen criterion. The operating frequency is decided by the frequency for which the feedback signal is in phase with input signal. Oscillators do not need external input signal. The oscillating frequency is selected by the frequency selective network from the noise present in the circuit. For amplifiers (that result when feedback path is removed) whose output is 180^0 out of phase with input, the frequency selective network is designed to produce an additional phase shift of 180^0. For amplifiers that produce in phase output, the frequency selective network produces zero or 360^0 phase shift. For low frequencies, R-C phase shift oscillator, Wien's bridge oscillators are used. For radio frequency oscillations, tuned circuits are used. Nowadays, piezoelectric crystal oscillators are being used as these can produce frequencies from few KHz to MHz. The output of crystal oscillator is not sinusoidal and is rich in harmonics. These are used in conjunction with tuned circuits which are tuned to multiples of fundamental frequency of piezo electric crystal; Giga Hertz frequency signals can be very easily generated by this method. For microwave frequencies, Klystrons, traveling wave oscillators, Magnetrons and Tunnel diodes are being used. In this lesson, we confine to R-C oscillators and L-C oscillators.

Oscillators can produce either sinusoidal or non-sinusoidal waveforms. Oscillators which produce sine waves are called *Sinusoidal Oscillators* Ex: Wien bridge, Phase shift, Colpitt's and Hartley oscillators. On the other hand, oscillators which produce non-sinusoidal waveforms are called *Relaxation* or *Non-sinusoidal Oscillators*. Ex: Astable, Monostable, Bistable multivibrators.

9.2 BARKHAUSEN CRITERION FOR OSCILLATIONS

Barkhausen proposed a criterion for an electronic circuit to produce sustained (constant amplitude) oscillations. This criterion is known as Barkhausen criterion. It is stated as "*Oscillations will be sustained if the magnitude of the product of the transfer*

gain of the amplifier A and the feedback factor β of the feedback network is greater than or equal to unity."

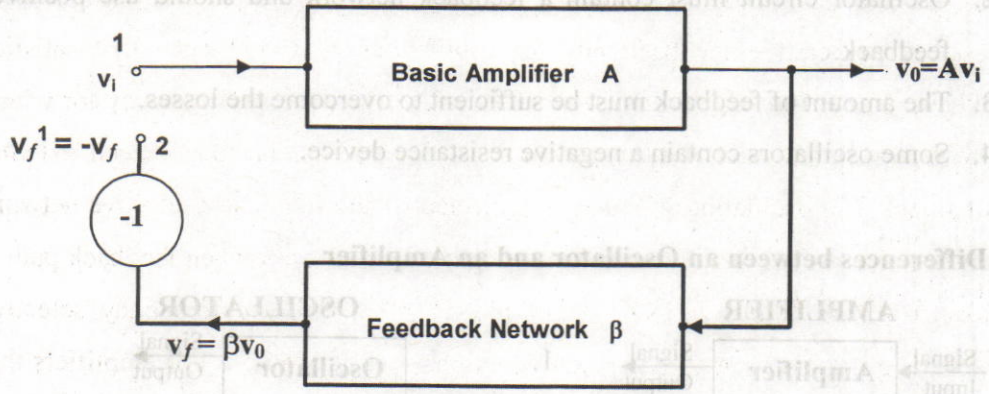


Fig.9.1

EXPLANATION

Fig.9.1 shows an amplifier, a feedback network and an input mixing circuit not yet connected to form a closed loop. The amplifier provides an output signal v_0 as a consequence of input signal v_i , directly applied to the input.

From the figure,

Output of the feedback circuit, $v_f = \beta v_0 = A\beta v_i$

Output of the mixing circuit,

$$v_f' = - v_f = -A\beta v_i$$

$$\text{Loop gain} = \text{Loop output} / \text{Loop input}$$

$$= v_f' / v_i = -A\beta v_i / v_i$$

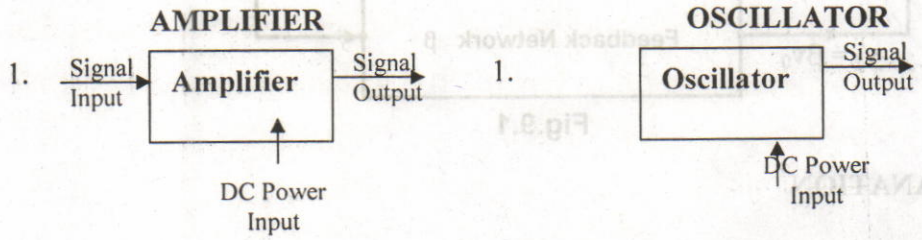
$$= - A\beta$$

The amplifier would continue to provide the same output v_0 as before, provided $v_f' = v_i$. In other words, if the external source were removed and if terminal '2' were connected to terminal '1'. The condition $v_f' = v_i$ is equivalent to $- A\beta = 1$ or loop gain must equal unity. This condition is called the Bharkausen criterion. This implies that $|A\beta| = 1$ and the phase of $-A\beta$ is zero.

Features of an Oscillator

1. Oscillator circuit must contain an active device (BJT or FET or an Op.Amp.) that works as an amplifier.
2. Oscillator circuit must contain a feedback network and should use positive feedback.
3. The amount of feedback must be sufficient to overcome the losses.
4. Some oscillators contain a negative resistance device.

9.3. Differences between an Oscillator and an Amplifier



AMPLIFIER	OSCILLATOR
2. Amplifier is an electronic circuit which can raise the strength of a weak signal applied at its input.	2. Oscillator is also an electronic circuit which itself can generate alternating signal over a wide frequency range.
3. In an amplifier, the frequency, waveform and magnitude of AC power generated is controlled by an AC input signal.	3. In an oscillator, the frequency, waveform and magnitude of AC power generated is controlled by the circuit itself.
4. Amplifier produces an output signal only when there is a signal at its input.	4. Oscillator does not require any input to start energy conversion process.
5. Amplifier utilizes D.C and Enhances power of AC wave-form applied at its output	5. Oscillator utilizes DC and converts it into AC power. So we can call it as an *Inverter.*
6. Amplifier utilizes mostly negative feedback mechanism.	6. Oscillator always utilizes positive feedback mechanism.
7. Amplifiers are used in all most All electronic devices in various Forms	7. Oscillators are mostly used in laboratory test equipment, harmonic generators carrier generators in Transmitters and Beat frequency oscillators in receivers.

9.4. RC-OSCILLATORS (SINUSOIDAL OSCILLATORS)

Oscillators which utilize an RC network (feedback network) as the frequency determining network is called as an RC Oscillator. Ex: Phase shift, Wien bridge. RC oscillators are used to generate audio frequency (AF) signals.

9.4.1 PHASE SHIIFT OSCILLATOR

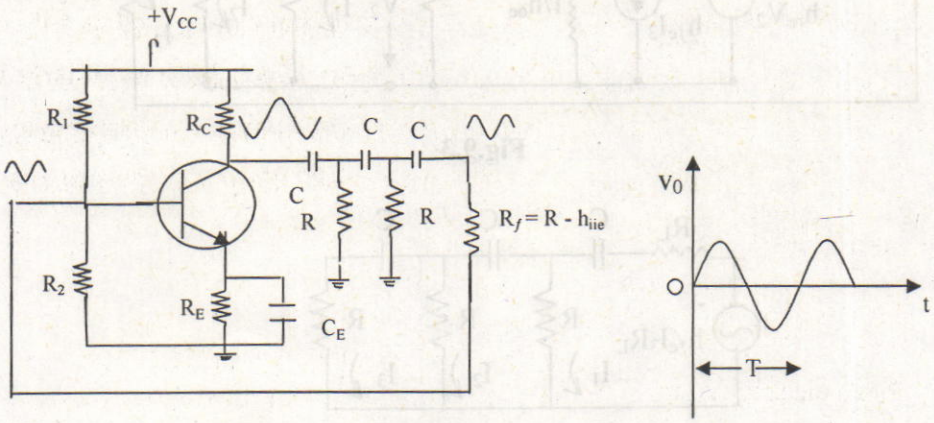


Fig.9.2 Phase shift oscillator and its output waveform

Working

The circuit of a Phase shift oscillator using an NPN transistor in *CE* configuration is shown in Fig.8.2. The resistor R_1, R_2 and R_E provide the necessary bias conditions for the circuit. C_E is the emitter bypass capacitor. The output developed at the collector is fed back to the input (to the base) via a cascaded RC-network. This cascaded network consists of three identical RC-networks. In the last section, $R_f + h_{ie} = R$, where h_{ie} is the input resistance of the transistor. We assume that resistors R_1, R_2 and R_3 do not effect the signal operation and hence we ignore them in the analysis.

The circuit is set into oscillations by any random variation caused in the base current. Due to transistor action, this variable base current is amplified and appears in collector circuit and fed back through the RC-cascaded network. This network produces a phase shift of 180^0 between its input and output voltages. An additional phase shift of 180^0 is produced by the CE transistor (transistor connected in common emitter configuration). Thus the total phase shift around the loop is 360^0 or 0^0 and the circuit acts as an oscillator.

Analysis

By using the h-parameter equivalent circuit of a transistor, we can draw the following circuit shown in Fig.9.3 for analysis.

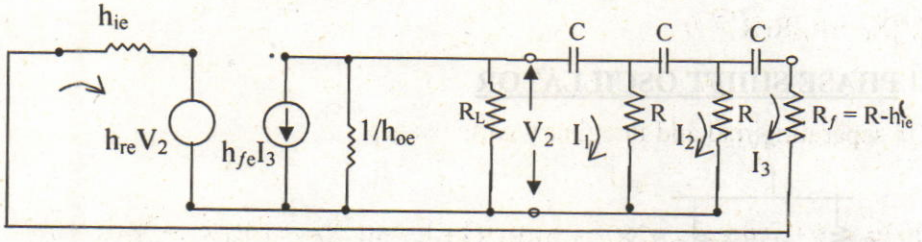


Fig.9.3

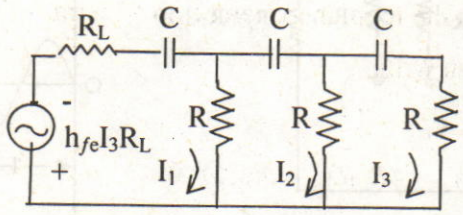


Fig.9.4

($\frac{1}{h_{oe}} >> R_L$, hence $\frac{1}{h_{oe}}$ can be neglected; h_{re} is very small, hence $h_{re}V_2$ can be neglected $h_{fe}I_3$ in parallel with R_L can be replaced by Thevenin's theorem). Hence the Phase shift oscillator equivalent circuit is drawn as shown in Fig.9.4.

Applying KVL to the three mashes, we get { here $X_C = \frac{1}{2\pi fC}$ }

$$(R_L - jX_C + R)I_1 - RI_2 + h_{fe}I_3R_L = 0 \quad \text{..... 9.4.1.1}$$

$$-RI_1 + (2R - jX_C)I_2 - RI_3 = 0 \quad \text{.....9.4.1.2}$$

$$0\,I_1 - RI_2 + (2R - jX_C)\,I_3 = 0 \quad \text{.....9.4.1.3}$$

$$\begin{vmatrix} (R_L + R - jX_C) & -R & h_{fe}R_L \\ -R & (2R-jX_C) & -R \\ 0 & -R & (2R-jX_C) \end{vmatrix} = 0$$

or $(R_L + R - jX_C)\left[(2R - jX_C)^2 - R^2\right] + R\left[-R(2R - jX_C)\right] + h_{fe}R_L\left[R^2\right] = 0$

or $(R_L + R - jX_C)(3R^2 - 4RjX_C - X_C^2) - 2R^3 + R^2 j X_C + h_{fe}R_L R^2 = 0$

$3R^2R_L + 3R^3 - 3jR^2X_C - 4RR_L jX_C - 4R^2jX_C - 4RX_C^2 - R_LX_C^2 - RX_C^2 + jX_C^3 - 2R^3 + R^2jX_C + h_{fe}R_LR^2 = 0$

On separating real and imaginary parts we get

$3R^2R_L + R^3 - 5RX_C^2 - R_LX_C^2 + h_{fe}R_LR^2 + j(-6R^2X_C - 4RR_LX_C + X_C^3) = 0$ 9.4.1.4

For '0' phase shift around the loop, there can be no 'j' term

Hence from Eq.(4), we can write

$$j.(-6R^2X_C - 4R_LRX_C + X_C^3) = 0$$

or $$X_C\left[X_C^2 - 4RR_L - 6R^2\right] = 0$$

$$X_C^2 = 4RR_L - 6R^2 \qquad \text{..... 9,4,1,5}$$

or $$\frac{1}{4\pi^2 f^2 C^2} = 4RR_L + 6R^2 \quad (\text{since } X_C = \frac{1}{2\pi fC})$$

or $$f^2 = \frac{1}{4\Pi^2 C^2\left(4RR_L + 6R^2\right)}$$

or $$f = \frac{1}{\sqrt{4\Pi^2 C^2\left(4RR_L + 6R^2\right)}}$$

$$= \frac{1}{2\Pi RC}\frac{1}{\sqrt{6 + 4K}}$$

where $K \equiv \frac{R_L}{R}$

If $R_L = R$ then the frequency of oscillations is given by

$$f = \frac{1}{2\Pi RC\sqrt{10}} \qquad \text{---------- 9.4.1.6}$$

Hence Eq. (4) becomes,

$$3R^2R_L + R^3 - X_C^2(5R + R_L) + h_{fe}R_LR^2 = 0$$

Using $X_C^2 = 4RR_L + 6R^2$, the above equation becomes

$$3R^2R_L + R^3 - (4RR_L + 6R)^2 [5R + R_L] + h_{fE}R_LR^2 = 0$$

Or $3R^2R_L + R^3 - 20R^2R_L - 4RR_L^2 + 30R^3 - 6R^2R_L + h_{fE}R_LR^2 = 0$

$$h_{fe}R_LR^2 = 23\,R^2\,R_L + 29\,R^3 + 4\,R\,R_L^2$$

$$h_{fe} = 23 + 29\frac{R}{R_L} + 4\frac{R_L}{R} \qquad \text{.....9.4.1.7}$$

If $R = R_L$, the condition for sustained oscillations is $h_{fe} = 23 + 29 + 4 = 56$

$$h_{fe} = 56 \qquad \text{..... 9.4.1.8}$$

i.e. the forward current transfer ratio of the transistor in a Phase shift oscillator must be at least equal or greater than 56, for sustained oscillations.

Features of R-C phase shift oscillator

1. This oscillator can be designed to work with either BJT or FET or OpAmp.. With BJT, circuit is designed using voltage shunt feedback to avoid the loading of feedback network by the low input impedance of transistor.. If FET is used, voltage series feedback is used

Its input impedance is quite high..

2. The active device produces 180 phase shift

3, It consists of positive feedback and negative feedback signal coupled through the feedback resistor R_f in series with R_i of the amplifier.

4. It is suitable to produce oscillations in the audio frequency range.

5. A transistor of large h_{fe} is needed to overcome the losses in the RC network.

9.4.2 WIEN BRIDGE OSCILLATOR

It is a low frequency, low distortion, tunable sine wave RC Oscillator. This utilized a two stage RC–coupled CE amplifier as an amplifying stage and one RC-bridge network as a feedback network. The circuit of Wien Bridge Oscillator is shown in Fig.9.5

When the power is first applied, a small base current develops at the base of Q_1. Due to transistor action, this appears in amplified form, but with a phase difference of 180^0 , at its collector. This amplified signal is fed back to the base of Q_1 through a

Wien bridge circuit (frequency determining and feedback circuit). The feedback signal and the actual signal at the base of Q_1 are at a phase of 360^0 or 0^0 . Thus the total phase shift around the loop is 360^0 which means a positive feedback. The frequency selective circuit permits only a signal with a frequency equal to f_r to appear in phase at the base of Q_1. This is amplified and continually reinforced, resulting in a build-up of the sine wave output.

Analysis

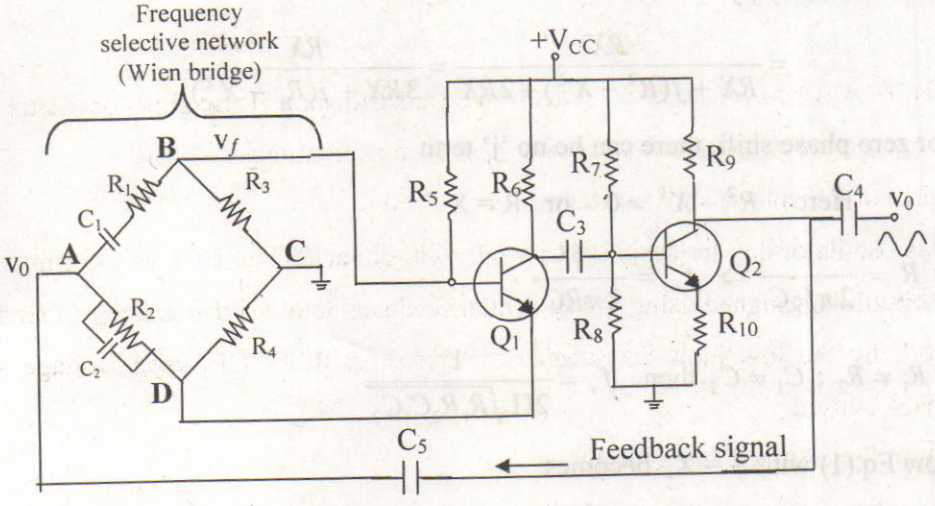


Fig.9.5 Wien bridge oscillator

Fig.9.6 is the part of the circuit (feedback part) and is shown in simplified form in Fig.9.7. Here V_o is the actual signal developed at output of Q_2, V_f is the signal fed back to Q_1.

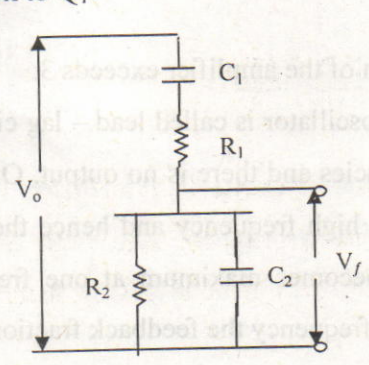


Fig 9.6

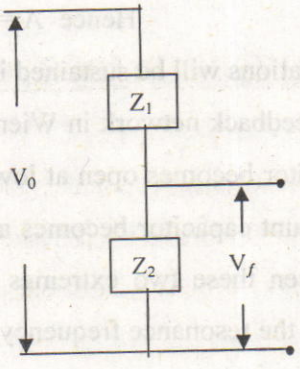


Fig 9.7

et $R_1 = R_2 = R$; $C_1 = C_2 = C$

$$Vf = \frac{Z_p}{Z_s + Z_p} V_o$$

$$\therefore \frac{V_f}{V_o} = \frac{Z_p}{Z_p + Z_s} = \frac{\frac{R(-jX)}{R+(-jX)}}{\frac{R(-jX)}{R+(-jX)} + R + (-jX)}$$

or $\beta = \frac{-jRX}{-jRX + (R - jX)^2} = \frac{RX}{RX + j(R^2 - j2RX - X^2)}$ (multiply numerator and denominator by j)

$$= \frac{RX}{RX + j(R^2 - X^2) + 2RX} = \frac{RX}{3RX + j(R^2 - X^2)}$$

For zero phase shift, there can be no 'j' term

Here $R^2 - X^2 = 0$ or R = X

or $R = \frac{1}{2\pi f_r C} \Rightarrow f_r = \frac{1}{2\pi RC}$

If $R_1 \neq R_2$; $C_1 \neq C_2$ then $f_r = \frac{1}{2\Pi\sqrt{R_1 R_2 C_1 C_2}}$

Now Eq.(1) with R = X, becomes

Feedback factor $\beta = \frac{V_f}{V_o} = \frac{RX}{3RX} = \frac{1}{3} \Rightarrow \beta = \frac{1}{3}$

To satisfy Barkhausen criterion; Aβ must be made equal to 1.

i.e. $A = \frac{1}{\beta}$ or $A = \frac{1}{1/3} = 3$.

Hence A = 3

Oscillations will be sustained if the gain of the amplifier exceeds 3.

The feedback network in Wien bridge oscillator is called lead – lag circuit. The series capacitor becomes open at low frequencies and there is no output. On the other hand the shunt capacitor becomes a short at high frequency and hence there is no output. Between these two extremes output becomes maximum at one frequency, This is called the resonance frequency. At this frequency the feedback fraction becomes 1/3..

Advantages

1. The overall gain is high because of two transistors.
2. The frequency of oscillations can be easily changed.

3. It gives constant output.

Disadvantage

1. It cannot generate very high frequencies.

Salient feature

1. It consists of two transistors to produce a phase shift of 360.
2. It can be used to produce oscillations over the frequency range 5Hz to 1MHz.
3. The frequency of oscillations can be varied conveniently by varying simultaneously the two capacitors .
4. It provides stable output.

9.5 LC OSCILLATORS

The two types of LC oscillators are Colpitt's and Hartley oscillators. These belong to LC oscillators family because their frequency determining circuit consists of inductor and capacitor as the elements.

9.5.1 COLPITT'S OSCILLATOR

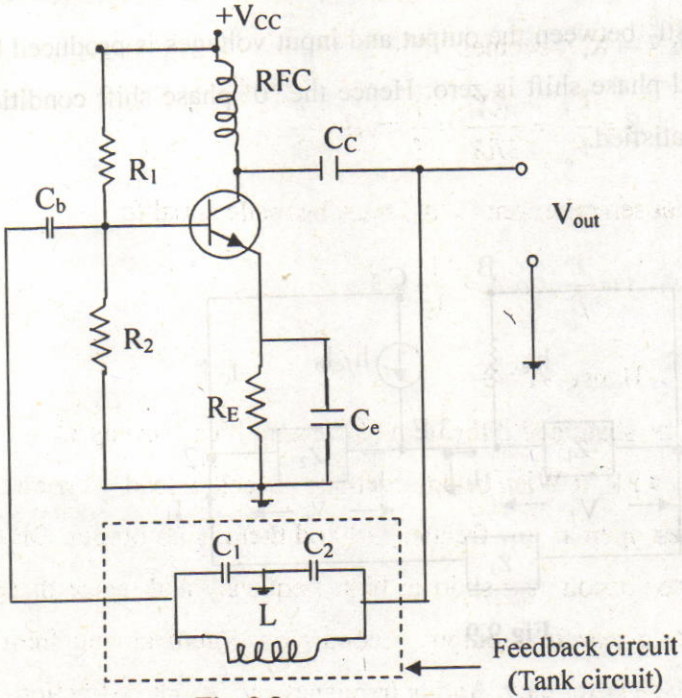


Fig. 9.8

Description

The circuit of Colpitt's oscillator is shown in Fig.9.8. It can be viewed as a single stage CE amplifier followed by a feedback circuit (Tank circuit). The resistors

R_1, R_2 and R_e provide the necessary bias conditions for the circuit. The capacitors C_1 and C_2 and the inductor L form the frequency determining network. The function of C_C and C_B is to block DC and to provide an AC path. RFC is a Radio Frequency Choke offers very high impedance to high frequency currents. It prevents Radio Frequency currents from reaching the source of collector supply voltage and prevents the source from short circuiting the alternating output voltage.

Working

When the collector supply voltage is switched on, the capacitors C_1 and C_2 are charged. These capacitors discharge through coil L setting up damped harmonic oscillations is the tank circuit. This oscillatory current in tank circuit produces an AC voltage across C_1 (i.e. between the terminals 1 and 3) and an AC voltage across C_2 (i.e. between the terminals 2 and 3). If the terminal 1 is at positive potential with respect to 3 at any instant, terminal 2 will be at negative potential with respect to 3 at the same instant. Thus the phase difference between the voltages is always 180^0. A further phase shift of 180^0 between the output and input voltages is produced by CE transistor. Thus the total phase shift is zero. Hence the '0' phase shift condition for sustained oscillation is satisfied.

ANALYSIS

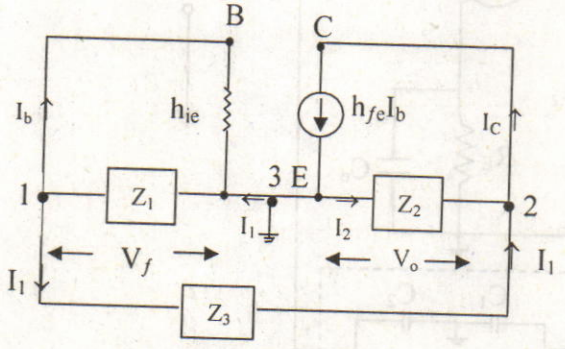


Fig.9.9

The above figure shows the equivalent circuit of Colpitt's oscillator. Here $h_{re}V_C$ is neglected $\frac{1}{h_{oe}}$ is omitted (because h_{re} is negligible; h_{oe} is very small.)

(i)Load Impedance (Z_L)

It is the impedance between the terminals 2 and 3; and is given by

$$Z_L = Z_2 II\left(Z^1 + Z_3\right)$$

where $Z^1 = Z_1 II h_{ie} = \dfrac{h_{ie} Z_1}{Z_1 + h_{ie}}$ 9.5.1.1

$$\therefore Z_L = \frac{Z_2\left(Z^1 + Z_3\right)}{Z_2 + Z^1 + Z_3} = \frac{Z_2\left[\dfrac{h_{ie} Z_1}{Z_1 + h_{ie}} + Z_3\right]}{Z_2 + Z_3 + \dfrac{h_{ie} Z_1}{Z_1 + h_{ie}}}$$

$$= \frac{\left[h_{ie} Z_1 + h_{ie} Z_3 + Z_1 Z_3\right] Z_2}{h_{ie}\left(Z_1 + Z_2 + Z_3\right) + Z_1 Z_2 + Z_1 Z_3} \quad \text{.....9.5.1.2}$$

(ii) Voltage gain of the basic amplifier is

$$A_V = -\frac{h_{fe} Z_L}{h_{ie}} \quad \text{.....9.5.1.3}$$

(iii) Feed back factor $\beta = \dfrac{V_f}{V_o}$

From the equivalent circuit, $V_f = \dfrac{Z^1}{Z^1 + Z_3} V_o$

Or $\beta = \dfrac{V_f}{V_o} = \dfrac{Z^1}{Z^1 + Z_3}$

or $\beta = \dfrac{\dfrac{h_{ie} Z_1}{h_{ie} + Z_1}}{\dfrac{h_{ie} Z_1}{h_{ie} + Z_1} + Z_3} = \dfrac{h_{ie} Z_1}{Z_1 Z_3 + h_{ie}\left[Z_1 + Z_3\right]}$ ------9.5.1.4

(iv) Barkhausen criterion is $A_V.\beta = 1$

i.e. $\dfrac{-h_{fe} Z_L}{h_{ie}} . \dfrac{h_{ie} Z_1}{Z_1 Z_3 + h_{ie}\left(Z_1 + Z_3\right)} = 1$

or $\dfrac{-h_{fe} Z_1}{Z_1 Z_3 + h_{ie}\left(Z_1 + Z_3\right)} \left(\dfrac{\left(h_{ie} Z_1 + h_{ie} Z_3 + Z_1 Z_3\right) Z_2}{h_{ie}\left(Z_1 + Z_2 + Z_3\right) + Z_1 Z_2 + Z_1 Z_3} \right) = 1$

or $\dfrac{h_{fe} . Z_1 . Z_2}{h_{ie}\left(Z_1 + Z_2 + Z_3\right) + Z_1 Z_2 + Z_1 Z_3} = -1$

or $h_{ie}\left(Z_1 + Z_2 + Z_3\right) + Z_1 Z_2 + Z_1 Z_3 = -h_{fe} . Z_1 . Z_2$

or $h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 (1+h_{fe}) + Z_1 Z_3 = 0$ - -------9.5.1.5

In case of Colpitt's oscillator, Z_1 is a capacitor, Z_2 is a capacitor and Z_3 is an inductor.

$$\therefore \quad Z_1 = \frac{-j}{\varpi C_1}; \qquad Z_2 = \frac{-j}{\varpi C_2}; \qquad Z_3 = j\omega L.$$

Hence Eq. (5) becomes

$$h_{ie}\left(-\frac{j}{\varpi C_1} - \frac{j}{\varpi C_2} + j\varpi L\right) + \left(-\frac{j}{\varpi C_1}\right)\left(-\frac{j}{\varpi C_2}\right)(1 + h_{fe}) + \left(-\frac{j}{\varpi C_1}\right)(j\varpi L) = 0$$

or

$$-jh_{ie}\left(\frac{1}{\varpi C_1} + \frac{1}{\varpi C_2} - \varpi L\right) - \left[\left(\frac{1+h_{fe}}{\varpi^2 C_1 C_2}\right) - \frac{L}{C_1}\right] = 0. \qquad \text{.....9.5.1.6}$$

For '0' phase shift, there can be no 'j' term.

$$\left(\frac{1}{\varpi C_1} + \frac{1}{\varpi C_2} - \varpi L\right) = 0 \qquad \text{.....9.5.1.7}$$

or $$\varpi L = \frac{1}{\varpi}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)$$

or $$\varpi^2 = \frac{1}{L}\left(\frac{C_1 + C_2}{C_1 C_2}\right) \qquad \text{.....9.5.1.8}$$

$$\varpi = \frac{1}{\sqrt{LC_{eq}}} \quad \text{where } C_{eq} = \left(\frac{C_1 C_2}{C_1 + C_2}\right).$$

Frequency of oscillation $f = \dfrac{1}{2\Pi\sqrt{LC_{eqv}}}$ 9.5.1.9

Condition for sustained oscillations

Substituting Eq.(7) into Eq.(6), we get,

$$-\frac{L}{C_1} + \frac{1+h_{fe}}{\varpi^2 C_1 C_2} = 0$$

or $$-\frac{L}{C_1} + \frac{1+h_{fe}}{\left(\dfrac{C_1 + C_2}{L}\right)} = 0$$

$$[\text{since } \varpi^2 C_1 C_2 = \left(\frac{C_1 + C_2}{L}\right) \text{ from Eq.(8)}]$$

$$\text{or} \qquad \frac{1}{C_1} = \left(\frac{1 + h_{fe}}{C_1 + C_2}\right)$$

$$\text{or} \qquad 1 + h_{fe} = \frac{C_1 + C_2}{C_1}$$

$$h_{fe} = \frac{C_2}{C_1} \qquad \text{.....9.5.1.10}$$

Colpitts oscillator is used in commercial signal generators to produce frequencies up to 100MHz

9.5.2 HARTELY OSCILLATOR

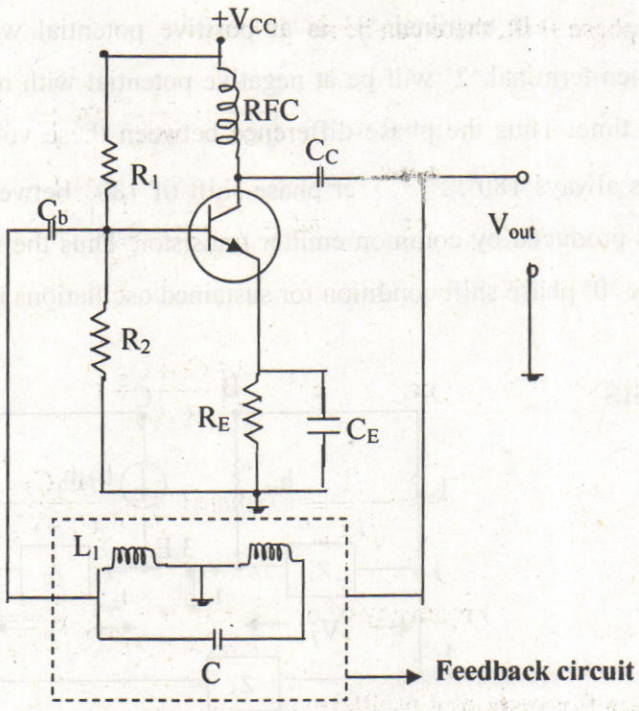


Fig 9.10

Description

The circuit of Hartley's oscillator is shown in Fig 9.10. It can be viewed as a single stage amplifier followed by a feedback circuit (tank circuit). The resistors R_1, R_2 and R_e provide the necessary bias conditions for the circuit .The capacitor C and the inductors L and L_2 form the frequency determining network. The function of C_C and C_B is to block DC and to provide an AC path. RFC is a Radio

Frequency Choke offers very high impedance to high frequency currents from reaching the source of collector supply voltage and prevents the source from short circuiting the alternating output voltage.

Working

When the collector supply voltage is switched on, the collector current starts rising and charges the capacitor 'C'. When this capacitor is fully charged it discharges through the coil L_1 and L_2 setting up damped harmonic oscillations in the tank circuit. This oscillatory current in tank circuit provides an AC voltage across L_1 which is applied to the base-emitter junction of the transistor and appears in the amplified form in the collector circuit. Feedback of energy from output to input is accomplished through auto transformer action. This energy supplied to the tank circuit overcomes the losses occurring in it. Hence oscillations are sustained.

If terminal '1' is at positive potential w.r.t terminal '3' at any instant, then terminal '2' will be at negative potential with respect to terminal '3' at the same time. Thus the phase difference between these voltages (voltage acrossL_1 and L_2) is always 180^0. An er phase shift of 180^0 between the output and input voltage is produced by common emitter transistor. Thus the total phase shift is zero. Hence, the '0' phase shift condition for sustained oscillations is satisfied.

ANALYSIS

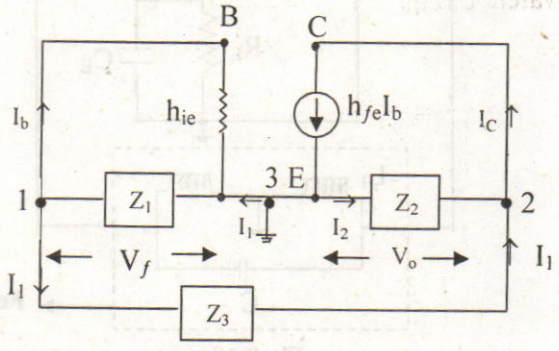


Fig 9.11 Equivalent circuit

Fig.9.11 sows the equivalent circuit of Hartley's oscillator. Here $h_{re}V_c$ is neglected and $\frac{1}{h_{oe}}$ is omitted.

(i)**Load Impedance:** Z_L. It is the impedance between the terminals 2 and 3 (output terminals) and is given by,

$$Z_L = Z_2 II \left(Z^1 + Z_3\right)$$

where $Z^1 = Z_1 II h_{ie}$

$$= \frac{h_{ie} Z_1}{Z_1 + h_{ie}} \qquad \text{.....9.5.2.1}$$

$$\therefore Z_L = Z_2 II \left(Z^1 + Z_3\right)$$

$$= \frac{Z_2 . \left(Z^1 + Z_3\right)}{Z_2 + Z^1 + Z_3}$$

$$= \frac{Z_2 . \left(\frac{h_{ie} Z_1}{h_{ie} + Z_1} + Z_3\right)}{Z_2 + Z_3 + \left(\frac{h_{ie} Z_1}{h_{ie} + Z_1}\right)}$$

$$Z_1 = \frac{\left[h_{ie} Z_1 + h_{ie} Z_3 + Z_1 Z_3\right] Z_2}{h_{ie}\left(Z_1 + Z_2 + Z_3\right) + Z_1 Z_2 + Z_1 Z_3} \qquad \text{.....9.5.2.2}$$

(ii) Voltage gain of the basic amplifier is

$$A_V = -\frac{h_{fe} Z_L}{h_{ie}} \qquad \text{..... .....9.5.2.3}$$

(iii) Feedback factor $\beta = \frac{V_f}{V_o}$

From the equivalent circuit, $V_f = \frac{Z^1}{Z^1 + Z_3} V_o$

or $$\beta = \frac{V_f}{V_o} = \frac{Z^1}{Z^1 + Z_3}$$

$$= \frac{\frac{h_{ie} Z_1}{h_{ie} + Z_1}}{\left[\frac{h_{ie} Z_1}{h_{ie} + Z_1} + Z_3\right]}$$

$$= \frac{h_{ie} Z_1}{Z_1 Z_3 + h_{ie}\left[Z_1 + Z_3\right]} \qquad \text{.....9.5.2.4}$$

(iv) **Barkhausen criterion** is $A_V \beta = 1$

i.e $$\frac{-h_{fe} Z_L}{h_{ie}} \cdot \frac{h_{ie} Z_1}{Z_1 Z_3 + h_{ie}\left(Z_1 + Z_3\right)} = 1$$

On putting the value of Z_L, we get

$$\frac{-h_{fe}Z_1}{h_{ie}(Z_1+Z_3)+Z_1Z_3}\cdot\frac{\left[h_{ie}(Z_1+Z_3)+Z_1Z_3\right]Z_2}{h_{ie}(Z_1+Z_2+Z_3)+Z_1Z_2+Z_1Z_3}=1$$

or $$\frac{h_{fe}.Z_1.Z_2}{h_{ie}(Z_1+Z_2+Z_3)+Z_1Z_2+Z_1Z_3}=-1$$

or $$h_{ie}(Z_1+Z_2+Z_3)+Z_1Z_2+Z_1Z_3=-h_{fe}.Z_1.Z_2$$

or $$h_{ie}(Z_1+Z_2+Z_3)+(1+h_{fe})Z_1Z_2+Z_1Z_3=0 \quad \text{.....9.5.2.5}$$

In case of Hartley's oscillator

$$Z_1=j\omega L_1;\quad Z_2=j\omega L_2;\quad Z_3=\frac{-j}{\omega C}$$

Hence Eq.(5) becomes,

$$h_{ie}\left[j\omega L_1+j\omega L_2-\frac{j}{\omega C}\right]+(1+h_{fe})\left[j\omega L_1.j\omega L_2\right]+\left[j\omega L_1.\left(\frac{-j}{\omega C}\right)\right]=0$$

or $$jh_{ie}\left[\omega(L_1+L_2)-\frac{1}{\omega C}\right]+(1+h_{ie})\omega^2L_1L_2+\frac{L_1}{C}=0 \quad \text{.....9.5.2.6}$$

(v) ***For 'zero' phase shift, there can be no 'j' term***

Hence, $$\omega(L_1+L_2)-\frac{1}{\omega C}=0 \quad \text{.....9.5.2.7}$$

or $$\omega(L_1+L_2)=\frac{1}{\omega C}$$

$$\omega^2=\frac{1}{(L_1+L_2)C}=\frac{1}{CL_{eq}} \quad \text{.....9.5.2.8}$$

Where $$L_{eq}=(L_1+L_2) \quad \text{..... 9.5.2.8a}$$

Frequency of oscillations $\therefore$ $$\boxed{f=\frac{1}{2\Pi\sqrt{CL_{eq}}}}$$

(vi) Condition for sustained oscillations

On substitution of Eq.(7) in to Eq.(6), we get .

$$-(1+h_{fe})\omega^2L_1L_2+\frac{L_1}{C}=0$$

or $$L_1 = (1 + h_{fe})\omega^2 L_1 L_2$$

But from Eq.(8) $$\omega^2 = \frac{1}{C(L_1 + L_2)}$$

$$\therefore \frac{L_1}{C} = \frac{(1 + h_{fe}) L_1 L_2}{C(L_1 + L_2)}$$

or $$(1 + h_{fe}) = \frac{L_1 + L_2}{L_2}$$

$$= 1 + \frac{L_1}{L_2}$$

$$h_{fe} = \frac{L_1}{L_2} \qquad \text{.....9.5.2.9}$$

NOTE: It mutual inductance is also taken into consideration, then Eq.(8) (a) and Eq.(9) becomes: $L_{eq} = (L_1 + M) + (L_2 + M) + L_1 + L_2 + 2M$

$$h_{fe} = \frac{(L_1 + M)}{(L_2 + M)}$$

9.6 Frequency stability of oscillators

Definition : It is a measure of oscillators ability to maintain as nearly a fixed frequency as possible over as a long time interval as possible.

For most purposes, the operating frequency of an oscillator must remain constant but the frequency of an oscillator changes due to the following factors:

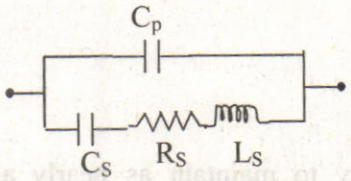
1. Variation of supply voltage: This can be overcome by using an electronically Regulated power supply.
2. Variation in reactive components of the tuned circuit due to change in temperature. This effect can be minimized by the use of a coil having larger number of turns and a low DC input voltage.
3. Variation in load.
4. Variation in transistor parameters due to thermal changes.
5. Mechanical variations.

Piezo Electric Crystal

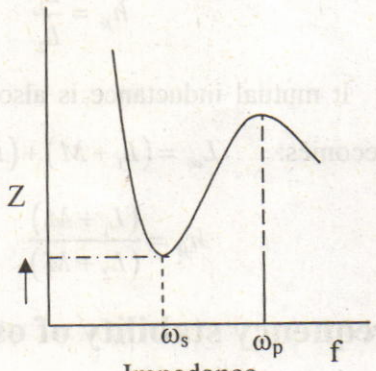
When the frequency of the oscillator is to be kept at fixed frequency, a quartz crystal which has piezoelectric property is generally used instead of the tuned circuit. Quartz crystals are piezoelectric . A quartz crystal has

two sets of axes. These are electrical and mechanical axes. When electrical stress is applied along electrical axes. The crystal sets into mechanical vibrations along mechanical axes. Likewise mechanical stress along mechanical axes voltage change along electrical axes. Thus the crystal will be set into vibration. A piezoelectric crystal's electrical equivalent circuit is shown in Fig . It has one series resonant frequency and one parallel resonance frequency.. Series resonance frequency is lower than parallel resonant frequency. Thus a piezo electric crystal can be used as either a series LCR or parallel LCR circuit with very high Quality factor. Because of large q-factor, the crystal posses great frequency stability and frequency discriminating capacity.. When kept in temperature controlled ovens, piezo electric crystals can have a frequency stability of 1 ppm.

Piezo electric crystal



Equivalent circuit



Impedance characteristic of crystal

Fig 9.12

Advantages of Quartz crystal

1. Greater mechanical strength.
2. Simplicity of manufacturing.
3. Quantity factor is very high (Q =10,000).
4. Higher order of frequency stability.
5. Frequency of oscillation of crystal is independent of supply voltage, transistor parameters.

9.7 CRYSTAL OSCILLATOR

When a high degree of frequency stability particularly over long periods of time is required, a crystal oscillator is generally used. Crystal oscillator consists of a quartz crystal as its tuned circuit.

The principle of operation of a crystal oscillator depends upon the Piezo electric effect. When mechanical stress is applied across the opposite faces of a quartz crystal, a potential difference is developed across them. It is called Piezo electric effect. Conversely, when a p.d is applied across its opposite faces, it causes the crystal to either expand or contract . If an alternating voltage is applied, the crystals set into vibration. The frequency of vibration is equal to the resonant frequency of the crystal.

PIERCE CRYSTAL OSCILLATOR

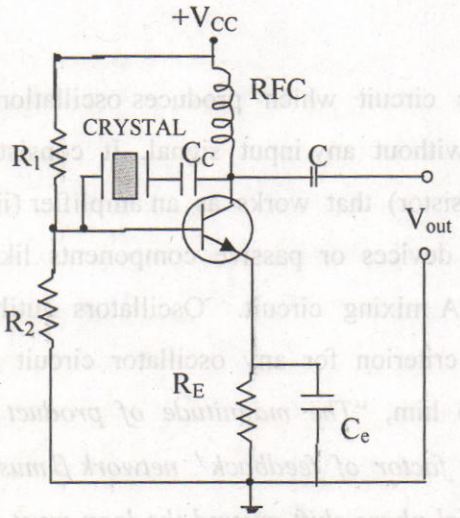


Fig.9.13

Fig.9.13 shows the circuit diagram of Pierce crystal oscillator. The resistors R_1, R_2 and R_3 provide bias and stabilization. C_E is an emitter bypass capacitor; C_C is a coupling capacitor. RFC is a Radio Frequency Coil provides DC collector load and prevents any AC signal from reaching the DC supply.

The crystal is connected as a series element in the feedback path from collector to base. Since in series resonance, crystal impedance is the smallest, the amount of positive feedback is the largest. The crystal normally provides feedback but also the necessary phase shift.

When the collector supply voltage is switched on, a transient current develops at the base. This appears in an amplified form at the collector but with a phase of 180^0 (due to CE configuration). This amplified signal is fed back to the base through the feedback path. The crystal provides an additional phase of 180^0,

so that the total phase around the positive feedback loop is 360^0. Hence sustained oscillations are produced, the frequency of which is decided by the crystal.

Oscillation frequency

$$f_o = \frac{1}{2\Pi\sqrt{LC_C}}$$

where 'L' is the equivalent inductance of crystal.

Advantages

(1) It has no tuned circuit.

(2) Frequency of oscillation can be changed easily.

9.8 SUMMARY

Oscillator is an electronic circuit which produces oscillations or non-sinusoidal waveforms on its own without any input signal. It consists basically three parts: (i) Active device (Transistor) that works as an amplifier (ii) Feedback circuit, consisting of either active devices or passive components like resistors, capacitors and inductors and (iii) A mixing circuit. Oscillators utilize ***positive feedback***. Barkhausen proposed a criterion for any oscillator circuit to produce sustained oscillations. According to him, "*The magnitude of product of gain of basic amplifier A and the feedback factor of feedback network β must be grater than or equal to unity*". *Also the total phase shift around the loop must be equal to zero or* 360^0. The product $\mathbf{A\beta}$ is called the ***loop gain***. Oscillator can produces either sinusoidal waveforms like sine or cosine waveforms or non-sinusoidal waveforms like square, rectangular waveforms etc. In any oscillator, the active device, i.e. transistor when used in CE configuration provides a phase shift of 180^0. An additional phase shift of 180^0 is provided by either an RC-network or an LC-network or another amplifier circuit or a quartz crystal. RC-oscillators can provide a sine wave output of AF range, whereas LC -oscillators can provide a sine wave output of RF (radio frequency) or high frequency range. Non-sinusoidal oscillators are also known as ***Relaxation oscillators***. Due to fluctuation in supply voltages, or change of active or passive components or temperature variation, the frequency of output signal produced by oscillators may change. To achieve frequency stability, quartz crystal oscillators were developed. The quartz crystal has advantages like excellent frequency stability, high Quality factor of 10000, simplicity of manufacturing, greater mechanical strength.

9.9. Key Terminology

Loop gain, oscillator, frequency stability, sinusoidal oscillator, LC-oscillator, RC-oscillator, Barkhausen criterion.

SOLVED NUMERICAL PROBLEMS

Example.1

Calculate the capacitance C_2 of a Colpitt's oscillator if L =100μH, C_1=0.1μF and resonant frequency $f = 100KHz$.

Solution: Given

$$C_1 = 0.1\mu F = 0.1 \times 10^{-6}\ F$$

$$L = 100\mu H, = 100\times10^{-6} H = 10^{-4} H$$

$$f = 100KHz = 100 \times 10^3 = 10^5\ Hz$$

To find C_2=?

We know that $f = \dfrac{1}{2\Pi\sqrt{LC_{eq}}}$ or $C_{eq} = \dfrac{1}{4\Pi^2 Lf^2}$ ---(1)

where $C_{eq} = \dfrac{C_1C_2}{C_1 + C_2}$ ------(2)

From Eq.(1) $C_{eq} = \dfrac{7\times7}{4\times22\times22\times10^{-4}\times10^{10}} = 0.0253\times10^{-6}F$

From Eq.(2), $$0.0253\times10^{-6} = \frac{10^{-7}\times C_2}{10^{-7} + C_2}$$

$$\left(C_2 + 10^{-7}\right)\times 0.0253\times10^{-6} = 10^{-7}C_2$$

$$= 0.1\times10^{-6}C_2$$

$$0.0253C_2 + 0.00253\times10^{-6} = 0.1C_2$$

$$0.0747C_2 = 0.00253\times10^{-6}$$

$$C_2 = \frac{0.00253}{0.0747}\times10^{-6} = 0.0338\times10^{-6}\text{F} = 0.0338\mu$$

Example.2

A phase shift oscillator uses three identical RC-sections in the feedback network. The values of components are $R = 100K\Omega$, $C = 0.01\mu F$. Calculate the frequency of the oscillation.

Solution: **Given** $R = 100K\Omega = 100\times10^{3} = 10^{5}\Omega$

$$C = 0.01\mu F = 0.01\times10^{-6}F = 10^{-8}F$$

To find $f = ?$

Frequency of the oscillation $f = \dfrac{1}{2\Pi RC\sqrt{10}}$

$$= \frac{7}{44\times10^{5}\times10^{-8}\times\sqrt{10}} = \frac{7000}{44\times\sqrt{10}}Hz$$

$$f = 50.3Hz$$

Example.3

A Wien bridge oscillator is to cover a frequency range from 20Hz to 20 KHz. The capacity of variable capacitor varies from 30pF to 300pF. Calculate the values of resistances required to cover the frequency range.

Solution: **Given** Frequency range = 20 Hz to 20 KHz

Capacity range = 30pF to 300pF

To find Resistance range = ?

Frequency of oscillation $f = 1/ (2\Pi RC)$

If f is minimum, C is maximum,

Hence, if $C = 300PF$, $f = 20Hz$

$\therefore R_{max} = 1/(2\Pi fC) = 7/(44 \times 20 \times 300 \times 10^{-12}) = (7000/264) \times 10^{6}\Omega = 26.5M\Omega$

Similarly, if $C = 30PF$, $f = 20Hz$

$$R_{min} = \frac{1}{2\Pi fc} = \frac{7}{44\times20\times10^{3}\times30\times10^{-12}}$$

$$= (70000 / 264) \times 10^{3} = 265\ K\Omega.$$

Example 4

In a Hartley oscillator $L_1 = 100\mu H$, $L_2 = 1mH$ and mutual inductance between coils $M = 20\mu H$. If $C = 20PF$, calculate the frequency of oscillations.

Solution: **Given** $L_1 = 100\mu H = 100\times10^{-6}H$

$$L_2 = 1mH = 1000\times10^{-6}H$$

$$M = 20\times10^{-6}H; C = 20 \times 10^{-12}$$

To find Frequency of oscillations $= f = ?$

We know that $f = \dfrac{1}{2\Pi\sqrt{CL_{eq}}}$;

$$L_{eq} = L_1 + L_2 + 2m = 100\times10^{-6}H + 1000\times10^{-6}H + 2\times20\times10^{-6}H$$

$$= 1102\times10^{-6}H$$

$$f = \frac{1}{2\Pi\sqrt{CL_{eq}}}$$

$$f = \frac{7}{44\times\sqrt{20\times10^{-12}\times1102\times10^{-6}}}H$$

$$= \frac{7000000}{44\times\sqrt{22040}}$$

$$= 1052KHz$$

9.10 Self assessment questions

(I) Long answer questions

1. What is Barkhausen criterion? Explain the working of Wien bridge oscillator with a circuit diagram. Derive an expression for its frequency of oscillations.
2. Draw the circuit diagram of Phase shift oscillator, explain its working. Obtain an expression for its frequency of oscillations.
3. Draw the circuits of Colpitt's and Hartley oscillator and explain their working.
4. What is frequency stability? Draw the circuit of crystal oscillator and explain how it produces oscillations?

(II) Short answer questions

1. What is frequency stability? How is it achieved?
2. Differentiate between oscillator and amplifier.
3. Draw the circuit of Wien bridge oscillator and explain how it produces oscillations?
4. State and explain the Barkhausen criterion for oscillations.
5. What is frequency stability? Why the frequency of oscillator changes?

(III) Numerical Problems

1. A Phase shift oscillator uses three identical RC sections with R=1MΩ and C = 68pF. Calculate the frequency of oscillations. Ans: 954 Hz.

2. The RC network of a Wien bridge oscillator consists of resistor of values $R_1=R_2=220M\Omega$ and capacitors of $C_1 = C_2 = 250pF$. Calculate the frequency of oscillations. Ans: 2.9 KHz.
3. A quartz crystal has the following parameters; L=0.5H; C=0.05 pF; R=1 KΩ. Find the frequency of oscillations. Ans: f=1.00065 MHz.

9.11 REFERENCES

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UNIT –III

LESSON-10

OSCILLATORS -II

OBJECTIVES OF THE LESSION

This lesson explains you the concepts of non sinusoidal oscillators like Astable multivibrator, Monostable multivibrator, Bistable multivibrator, Schmitt trigger circuits. It also explains you the way of producing non-sinusoidal waveforms like square waveform, estimation of frequency of generated output. It also provides the list of various applications of multivibrators.

STRUCTURE OF THE LESSION

10.1 INTRODUCTION

The oscillator which generate waveforms, other than sine wave forms are called Non-sinusoidal or Relaxation oscillators. Non-sinusoidal waveforms may be square wave, rectangular wave, sawtooth wave, pulse etc.

RELAXATION OSCILLATORS

It is defined as a circuit in which voltage or current change abruptly from one value to another and which continues to oscillate between these two values as long as dc power is supplied to it. These can be classified as Astable, Monostable, and Bistable Multivibrators.

MULTIVIBRATORS

An electronic circuit that generates non–sinusoidal waveforms is known as a Multivibrator. It is basically a two-stage amplifier with positive feedback from the output of one amplifier to the input of the other. The feedback is supplied in such a manner that one transistor is driven to saturation and the other to cut-off. Thus multivibrators are based on the switching characteristics of the transistor and on the time required to switch from one state to another.

TYPES OF MULTIVIBRATORS

(1) Astable Multivibrator (Non–driven type)

(2) Monostable Multivibrator (Triggered type)

(3) Bistable Multivibrator (Triggered type)

USES OF MULTIVIBRATORS

1. As frequency divider.
2. As saw tooth generator
3. As square wave and pulse generators
4. As memory elements in computers
5. As standard frequency sources
6. For use in TV and RADAR circuits.

10.2 ASTABLE MULTIVIBRATOR

Def: *A multivibrator which generates square waves on its own is known as an Astable or Free Running Multivibrator.*

An astable multivibrator has no stable state. It switches automatically between the two states (ON and OFF) and remains in each for a time

dependent upon the circuit constants. It is an oscillator since it requires no external pulse for its operation.

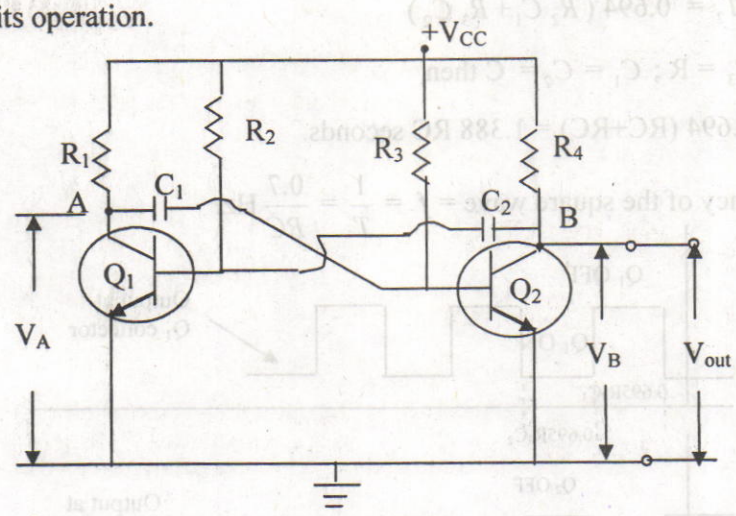

Fig.10.1

Fig.10.1 shows the circuit of a collector–coupled AMV using two similar transistors. Here the feedback ratio is unity and positive, because of 180^0 phase shift in each stage. Hence the circuit oscillates.

When the power is switched on, suppose that Q_1 starts conducting before Q_2 conducts. Due to feedback, Q_1 will be driven to saturation and Q_2 to cut - off. Since Q_1 is in saturation, whole of V_{cc} drops across R_1. Hence V_A = 0V. Since Q_2 is cut-off i.e., it conducts no current and hence $V_B = V_{CC}$. Since V_A = 0V, C_1 starts to charge through R_2 towards V_{CC}. The voltage across C_1 drives Q_2 into saturation. The potential at B decreases from V_{CC} to almost 0V .This potential decrease (negative swing) is applied to the base of Q_1 through C_2 .Consequently Q_1 is driven to cutoff and $V_A = V_{CC}$. Since V_B = 0V, C_2 starts charging through R_3 towards V_{CC}. This voltage of C_1 drives Q_1 to saturation and V_A = 0V. In this way, whole cycle is repeated. Since each transistor is driven alternately into saturation and cut-off, the voltage waveform at A or B is essentially a square waveform with a peak amplitude equal to V_{CC}, as shown in Fig 10.2

SWITCHING TIMES

ON time for Q_1 (or OFF time for Q_2) = 0.694 $R_2 C_1 = T_1$

OFF time for Q_1 (or ON time for Q_2) = 0.694 $R_3 C_2 = T_2$

Total time period of the square wave is

$T = T_1 + T_2 = 0.694 (R_2 C_1 + R_3 C_2)$

If $R_2 = R_3 = R$; $C_1 = C_2 = C$ then

$T = 0.694 (RC+RC) = 1.388\ RC$ seconds.

Frequency of the square wave = $f = \frac{1}{T} = \frac{0.7}{RC}$ Hz.

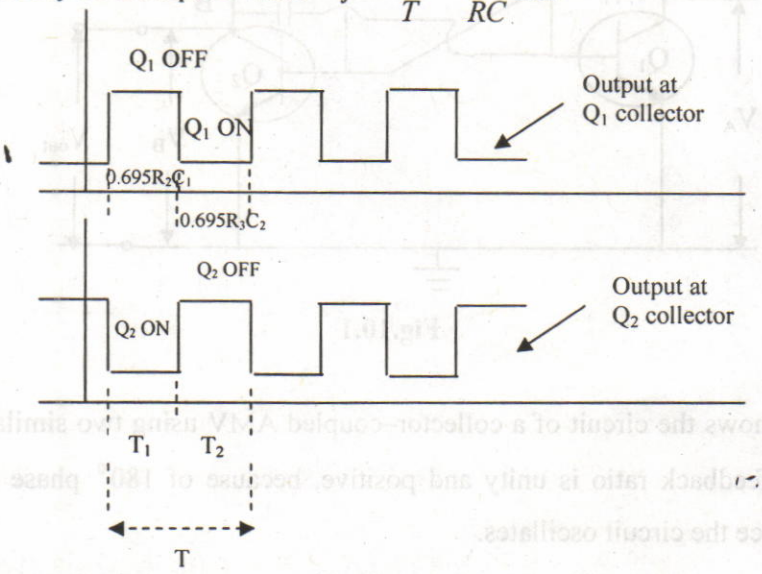

Fig.10.2

10.3 MONOSTABLE MULTIVIBRATOR

A multivibrator in which one transistor is always conducting (i.e. is in ON state) and the other is non-conducting (i.e. in the OFF state) is called Monostable multivibrator. A mono stable multivibrator has only one state stable. This means that if one transistor is conducting and the other is non conducting, the circuit will remain in this position. With the application of external pulse, the circuit will interchange the states.

However, after a certain time, the circuit will automatically switch back to the original state and remains there until another pulse is applied. Thus a mono stable multivibrator can not generate square waves on its own.

Working

The circuit shown in Fig.10.4 consists of two similar transistors Q_1 and Q_2. V_{BB} and R_5 keeps Q_1 at cut-off (reverse biases Q_1). The V_{CC} and R_2 keeps Q_2 in saturation (Q_2 forward biased). The input pulse is given through C_2 to obtain the square wave.

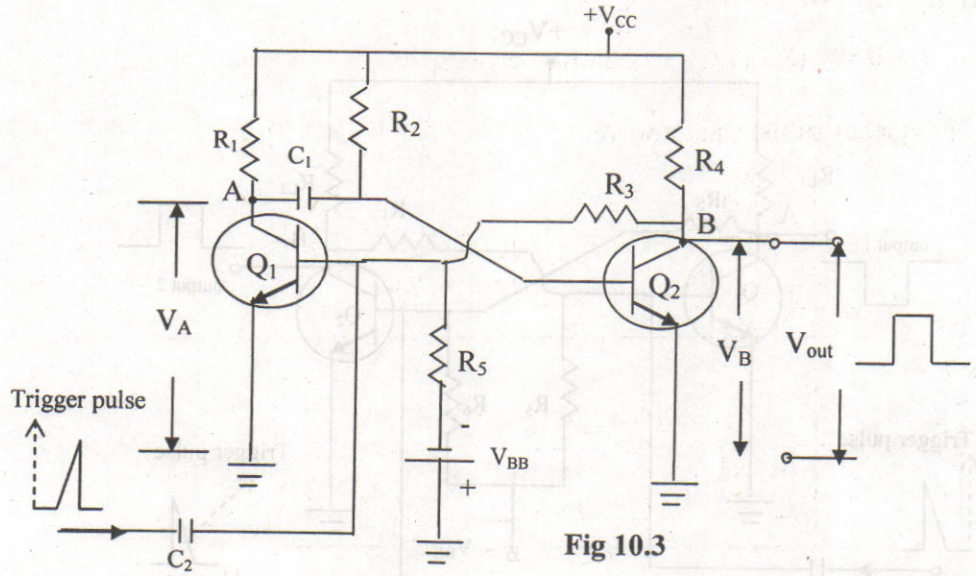

Fig 10.3

With the circuit shown, Q_1 is at cut [illegible]nd Q_2 is at saturation .When a positive pulse of short duration is applied to the base of Q_1 through C_2, then Q_1 starts conducting and its collector voltage falls.(i.e.V_A approaches 0V). This decreasing voltage is fed to Q_2 via C_1 where it decreases its forword bias .This makes Q_2 to cutoff i.e. $V_B = V_{CC}$ .This increases the forword bias of Q_1 further i.e. $V_A = 0V$. This action is cumulative and ends with Q_1 conducting (saturation) and Q_2 cutoff.

As V_A = 0V, C_1 starts to discharge through saturated Q_1 to ground. As C_1 discharges, Q_2 is pulled out of cutoff .As Q_2 conducts further, the negative going signal from B via R_3, drives Q_1 to cutoff. Hence, the circuit returns to its original state with Q_2 in saturation and Q_1 at cutoff. The output is taken at A or B. The width of the pulse is determined by the time constant C_1R_2. Since this multivibrator produces one output pulse for every input trigger pulse, it is called *Monostable or One-shot Multivibrator.*

Duration of the pulse $T = 0.69\ R_2C_1$

The monostable multivibrator cannot generate square waves on its own like astable multivibrator. It supplies a single output pulse of fixed duration for every input trigger pulse.

10.4 BISTABLE MULTIVIBRATOR (BMV)

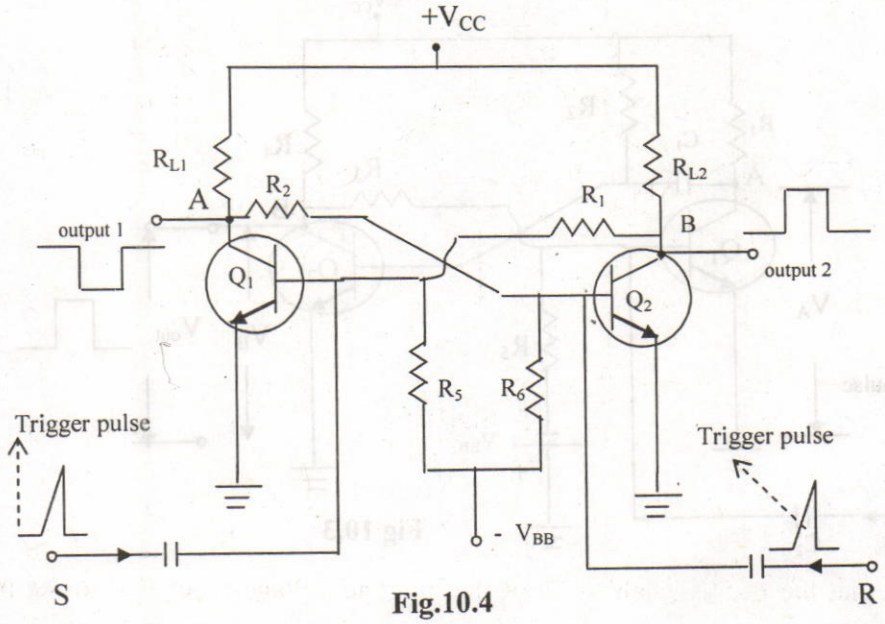

Fig.10.4

A multivibrator which has both states stable is called a Bistable Multivibrator. It can stay in one of its two states indefinitely; (as long as power is supplied) changing to other state only when it receives a trigger pulse from outside. When it receives another triggering pulse, then it goes back to its original state. The Bistable Multivibrator is also known as *Flip-Flop* circuit and is shown in Fig.10.4

Working

If Q_1 is conducting, then V_A = 0V. This makes Q_2 cutoff. Similarly with Q_2 OFF (non conducting), the potential divider from V_{CC} to V_{BB} (R_{L2}, R_1, R_2) keeps Q_1 to conduct. Thus Q_1 holds Q_2 OFF and Q_2 hold Q_1 ON.

Suppose a positive pulse is applied to R. It will cause Q_2 to conduct. This makes Q_1 to cutoff. Consequently, the BMV switches over to its other state. Similarly a positive trigger pulse at S will switch the BMV to its original state.

10.5 SCHMITT TRIGGER

This is also a Bistable Multivibrator circuit. It has two stable states and the magnitude of the input voltage determines which of the two is positive. It is also called emitter coupled binary because positive feedback occurs by coupling through R_E.

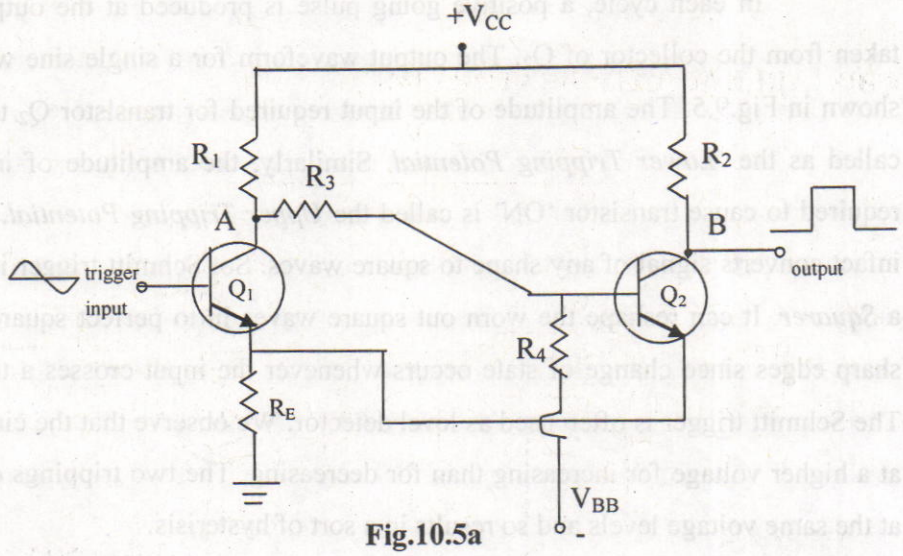

Fig.10.5a

Working

Suppose that the positive half cycle of the input ac voltage is applied to the trigger input. This is sufficient to put Q_1 into conduction and ultimately reaches saturation .This makes $V_A = 0V$. As base of Q_2 is coupled to collector of Q_1 via R_3, Q_2 is driven to cut-off. This process is cumulative and ends up with Q_1 in ON state and Q_2 in OFF state.

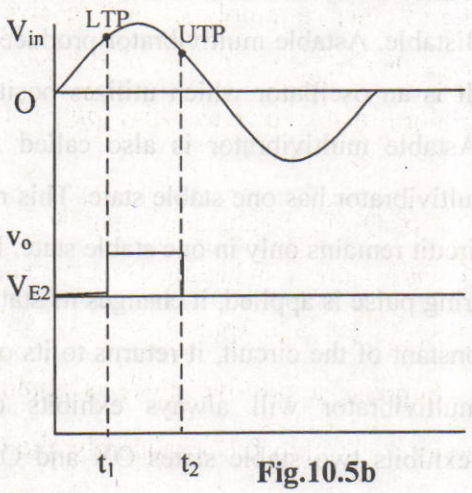

Fig.10.5b

During the negative half cycle of the input signal, the reverse operation will takes place .i.e. Q_1 is driven to cut-off (OFF state) and Q_2 to saturation (ON state).This completes one cycle. This cycle is repeated as input voltage rises and falls again.

In each cycle, a positive going pulse is produced at the output which is taken from the collector of Q_2. The output waveform for a single sine wave input is shown in Fig.9.5. The amplitude of the input required for transistor Q_2 to conduct is called as the '*Lower Tripping Potential*. Similarly, the amplitude of input voltage required to cause transistor 'ON' is called the *Upper Tripping Potential*. The circuit, infact converts signal of any shape to square waves. So, Schmitt trigger is also called a *Squarer*. It can reshape the worn out square waves in to perfect square wave with sharp edges since change of state occurs whenever the input crosses a trigger point. The Schmitt trigger is often used as level detector. We observe that the circuit triggers at a higher voltage for increasing than for decreasing. The two trippings do not occur at the same voltage levels and so results in a sort of hysterisis.

USE: For wave shaping purposes.

10.6 SUMMARY

Multivibrator is a relaxation oscillator. This means that the voltage or current at the output changes abruptly from one value to another. This process will be continued cyclically as long as dc power is supplied to the circuit. The term multivibrator is divided from the fact that a square wave actually consists of large number of sinusoidals of different frequencies. This fact can be understood by analyzing square wave using Fourier analysis. Multivibrators can be of different types like Astable, Monostable; Bistable. Astable multivibrator produces a square wave output. It has no stable states. It is an oscillator which utilizes positive feedback. Astable means no stable state. Astable multivibrator is also called *Free running multivibrator*. A monostable multivibrator has one stable state. This requires a triggering pulse to give output. This circuit remains only in one stable state. It may be either ON or OFF state. When a triggering pulse is applied, it changes its state and after some time determined by the time constant of the circuit, it returns to its original state. This means that the monostable multivibrator will always exhibits one stable state. The Bistable multivibrator exhibits two stable states ON and OFF. To produce one rectangular output pulse, the circuit needs two triggering pulses. It is also called as binary or FLIP-FLOP; it can store a binary digit of either 1 or 0. Hence it can be used as the basic memory element. If such circuits are connected in the form of matrix, it can store more and more binary information. A Schmitt trigger is also one type of multivibrator. It can only be used as a wave shaping circuit. It reshapes the digital

pulses that suffered distortion in shape while traveling through the transmission networks into their standard format and power levels.

10.7 KEY TERMINOLOGY

ON state, OFF state, Astable, Monostable, Bistable, Trigger input, Positive feedback.

SOLVED NUMERICAL PROBLEMS

Example.1

In an Astable multivibrator the values of two resistors are $R_1 = R_2 = 15\ K\Omega$, and capacitor values are $C_1 = C_2 = 0.005\ \mu F$. Calculate the frequency of oscillation.

Solution:

Given $R_1 = R_2 = 15\ K\ \Omega = 15000\Omega$; **To find** $f = ?$

$$C_1 = C_2 = 0.005\ \mu F = 0.005 \times 10^{-6} F = 5 \times 10^{-9} F$$

Time period $T = 0.69(R_1C_1 + R_2C_2) = 1.38RC$

(Since $R_1 = R_2 = R$, $C_1 = C_2 = C$)

$$= 1.38 \times 15000 \times 5 \times 10^{-9} \text{ sec}$$

$$T = 20.7 \times 10^{-6} \text{ sec.}$$

$$\text{Frequency } (f) = \frac{1}{T} = \frac{10^6}{20.7} = 9.66 \text{ KHz}$$

10.8 SELF ASSESSMENT QUESTIONS

I) Long Answer Questions

1. What are multivibrators? Explain the working of monostable multivibrator.
2. What is a multivibrator? What are different types of multivibrators? Explain the action of free running multivibrator with a neat circuit diagram. Draw its output wave form.

II) Short Answer Questions

1. Draw the circuit diagram of Schmitt trigger circuit and draw its input and output waveforms.
2. Explain the action of Monostable multivibrator.
3. Explain the action of Bistable multivibrator.
4. What is a multivibrator? Why it is called so? Give the classification of multivibrators.

III) Numerical Problems

1. In a free running multivibrator, $R_1 = R_2 = 10K\Omega$, $C_1 = C_2 = 0.01\mu F$. Find the frequency of oscillators. Ans:
2. An astable multivibrator has $R_1 = R_2 = R = 10K\ \Omega$, $C_1 = C_2 = C = 120pF$. Calculate the frequency of oscillations. Ans:

10.9 REFERENCES

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2. Principle of Electronics –V.K.Mehta, (S.Chand.)
3. Basic Electronics-B.L .Theraja (S.Chand.)
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UNIT-IV **LESSON-11**

FIELD EFFECT TRANSISTOR

OBJECTIVES OF THE LESSON

This lesson explains the concepts of Field Effect Transistor, biasing methods, characteristics (Drain, Transfer), construction, advantages, parameters of FET, models, application of FET, MOSFET and its types (Enhancement and Depletion), characteristics, applications.

STRUCTURE OF THE LESSON

11.1 INTRODUCTION

The Field Effect Transistor (FET) is a semiconductor device which depends for its operation on the control of the current by an electric field. The two types of FETs are Junction Field effect Transistor (JFET) and the Insulated Gate field Effect Transistor (IGFET) or Metal-Oxide Semiconductor Field Effect Transistor [MOSFET]. JEFET is also called a *unipolar transistor* because in it the current is carried by only one type of charge carries (either electrons or holes). It is a transistor because its characteristics are similar to that of the transistor. It can also act as an amplifier. It exhibits only output and transfer characteristics. Another version of JFET or an ordinary BJT is MOSFET, but it has much more input impendence than JFET or BJT. It can work in two modes Enhancement and Depletion.

11.2 BASIC STRUCTURE OF N-CHANNEL FET

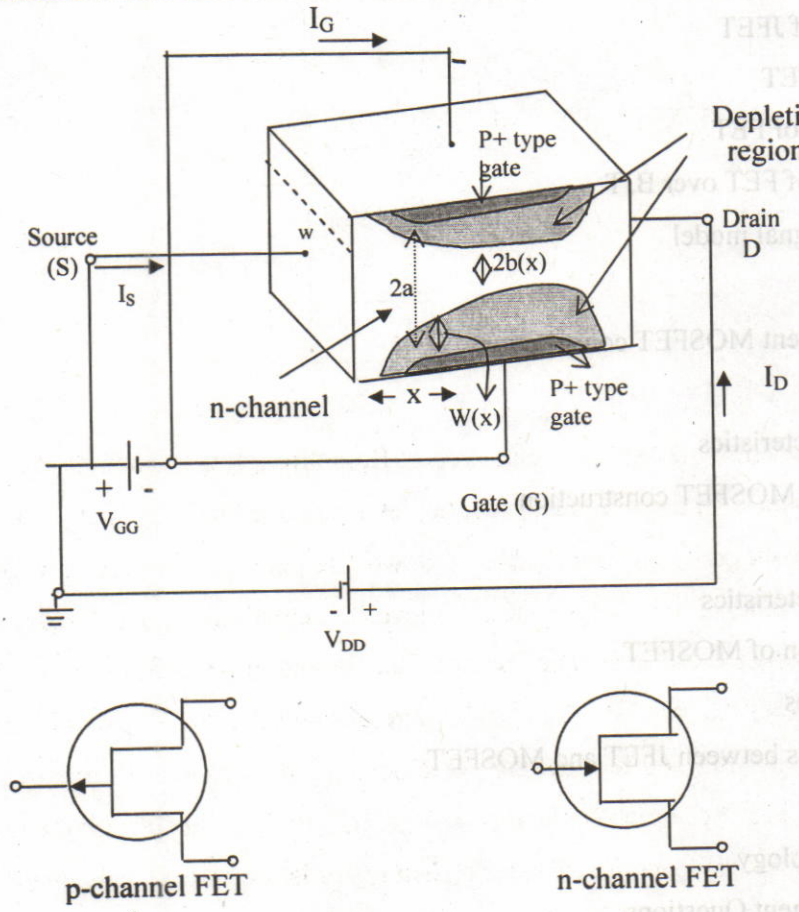


Fig.11.1

The basic structure of an n-channel J-FET is shown in Fig.11.1. Ohmic contacts are made to the two ends of an n-type semiconductor bar, and current flows along the length of the bar when a voltage is applied between the two ends. The left hand end of the bar is called the *Source(s)*, through which the majority carries (electrons) enter the channel. The right hand end of the bar is called the *Drain (D)* through which the majority carries leave the bar. On the other two sides of the n-type bar; heavily doped (p+) regions are formed by alloying or diffusion. These impurity regions are called the *Gates* G, which control the carries flow. The two gates are electrically connected internally. The region of the n-type material between the two gate regions is the ***channel*** through which the majority carries more from source to drain.

11.3 FET OPERATION

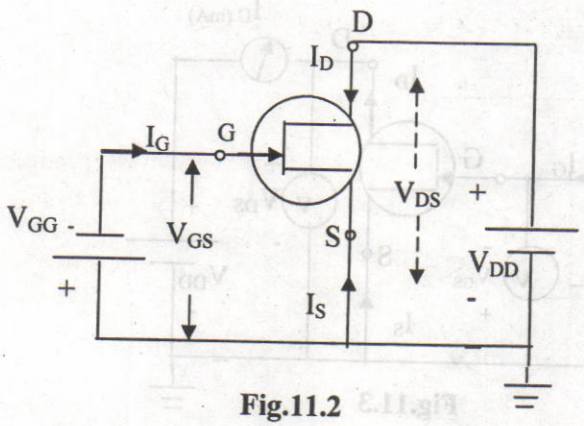


Fig.11.2

The application of V_{DD} will cause the electrons to flow through the channel from source to drain. The amount of drain current I_D will be determined initially by the voltage V_{DS}. The Gate supply voltage V_{GG} reverse biases the two PN-junctions formed between gate and source. These reverse biased PN-junctions develop depletion regions. These regions decrease the conductance of the channel between source and drain. As the reverse bias is increased, the thickness of the depletion region increases and the drain current is reduced. Hence the effective width of the channel will become progressively decreased with increasing reverse bias. So, for a fixed value of V_{DS}, I_D will be a function of the reverse-bias voltage across the gate junction. The term ***field effect*** is used because the mechanism of current control is the effect of the extension of the field associated with the region of uncovered charges in the depletion region.

When the reverse bias is large enough for the depletion regions to meet, the channel becomes pinched off and the drain current cuts off. The reverse bias required for pinch off is called the *Pinch-off voltage* V_P.

The drain current is given by

$I_D = I_{DSS}[1 - V_{GS}/V_P]^2$ → ***Shockley's equation.***

where I_{DSS} = Maximum drain current

The squared term of the equation will result in a non linear relationship between I_D and V_{GS} producing a curve that grows exponentially with increasing values of V_{GS}. The transfer curve can be obtained Schockley's equation or from the output characteristics.

11.4 FET CHARACTERISTICS

(1) OUTPUT OR DRAIN CHARACTERISTICS

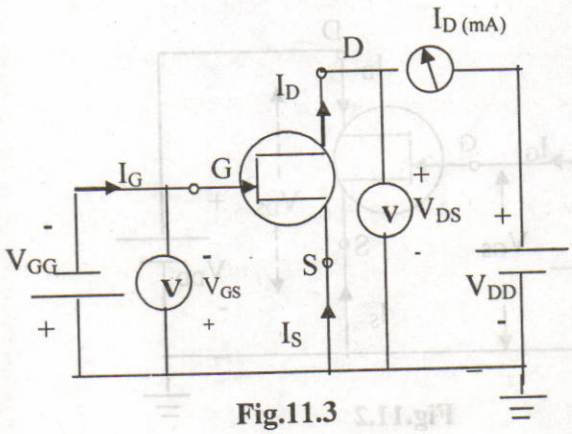


Fig.11.3

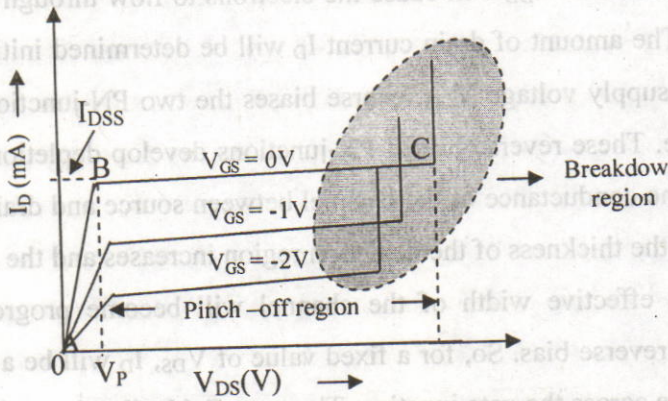


Fig.11.4

The curves obtained by plotting drain current (I_D) and drain to source voltage (V_{DS}) for different gate-to-source voltages (V_{GS}) are called the *Drain Characteristics*. The curves are shown in Fig.11.4. Fig.11.3 shows the circuit diagram used for determining the drain characteristics, V_{GG} is fixed at different values and the variation between V_{DS} and I_D is noted.

From the graph we note that:

(1) Drain current I_D varies directly with low values of V_{DS} following Ohm's law. The JFET behaves like a resistor, till the voltage V_P is reached.

(2) As V_{DS} is further increased, I_D begins to level off and approach a constant value (I_{DSS}). The voltage above which the drain current levels off is called the *Pinch off voltage* (Vp). The region BC is called the *Saturation region* (*pinch-off region*).

(3) As V_{DS} is increased beyond BC, the JFET enters the breakdown region. It is due to the avalanche breakdown of the gate junction.

(4) If a gate voltage, V_{GS}, is applied in the direction to provide additional reverse bias, pinch-off will occur for smaller values of $|V_{DS}|$ and the maximum drain current will be smaller.

Hence, we conclude that each characteristic curve has an Ohmic region for small values of V_{DS}, and also has a constant-current region for large values of V_{DS} where I_D responds slightly to V_{DS}.

TRANSFER CHARACTERISTICS

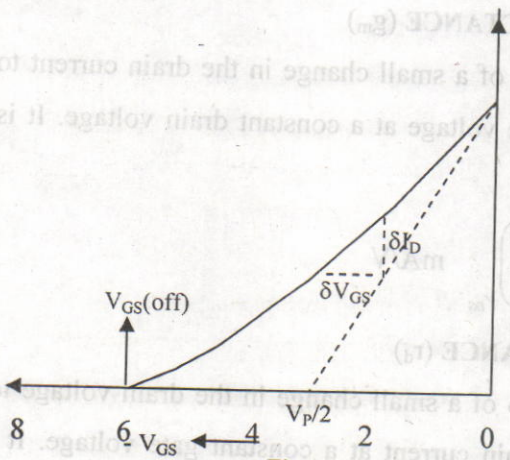


Fig.11.5

It is a plot of I_D verses V_{GS} for a fixed value of V_{DS} and is shown in figure. In this experiment V_{DS} is maintained constant at a suitable value greater than the pinch-off voltage. The gate voltage is decreased from zero in equal steps till I_D is reduced to zero. The drain current I_D is noted at each setting of V_{GS}. Now a graph is plotted with V_{GS} along X-axis and I_D along Y-axis. From the transfer characteristic (Fig.11.5) we can determine

(1) Gate-source cutoff voltage

(2) Trans conductance g_m.

(3) The value of V_{GS} at which $I_D = 0$ is the gate-source cutoff voltage, denoted by

$V_{GS(Off)} = |V_{GS(off)}| = V_P$.

(4) g_m is measured by

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}}.$$

Merits and demerits of FET

a) It has high input impedance.

b) It is less noisy.

c) It is thermally stable.

d) It is compatible for the fabrication in integrated circuits and occupies less space.

e) It can be used as a voltage variable resistor.

f) The gain-bandwidth product is small.

11.5 PARAMETERS OF JFET

(1) TRANS CONDUCTANCE (g_m)

It is the ratio of a small change in the drain current to the corresponding small change in the gate voltage at a constant drain voltage. It is obtained from the transfer characteristic.

$$g_m = \left(\frac{\delta I_D}{\delta V_{GS}}\right)_{V_{DS}} \quad \text{mA/V}$$

(2) DRAIN RESISTANCE (r_d)

It is the ratio of a small change in the drain voltage to the corresponding small change in the drain current at a constant gate voltage. It is reciprocal of the slope of the drain characteristics.

$$r_d \doteq \left(\frac{\delta V_{DS}}{\delta I_D}\right)_{V_{GS}} \quad \Omega$$

(3) **AMPLIFICATION FACTOR** (μ)

It is the ratio of a small change in the drain voltage to the corresponding small change in the gate voltage at a constant drain current. It is defined by μ and is given by

$$\mu = -\left(\frac{\delta V_{DS}}{\delta V_{GS}}\right)_{I_D}$$

RELATION BETWEEN PARAMETERS

Since I_D depends on V_{DS} and V_{GS}, we write

$I_D = f(V_{DS}, V_{GS})$

Suppose, V_{DS} changes from V_{DS} to $V_{DS} + dV_{DS}$ and gate voltage V_{GS} from V_{GS} to $V_{GS} + dV_{GS}$. Now small change in I_D is given by

$$dI_D = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} dV_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} dV_{GS}$$

Dividing both sides by dV_{GS}, we get

$$\frac{dI_D}{dV_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{dV_{DS}}{dV_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

If I_D is constant then $\frac{dI_D}{dV_{GS}} = 0$

$$\therefore 0 = \left(\frac{1}{r_d}\right)(-\mu) + g_m$$

or $\mu = r_d g_m$

In an n-channel FET, in common source configuration, Drain terminal is connected to V_{DD}, a voltage source up to 15V. The gate source junction is always reverse biased.

11.6 BIASING OF JFET

(1) VOLTAGE DIVIDER BIAS

The voltage divider gate bias arrangement shown in Fig.11.6. (In this circuit, gate is reversed biased). A voltage source V_{DD} is connected between drain and source to supply the charge carriers in the channel.

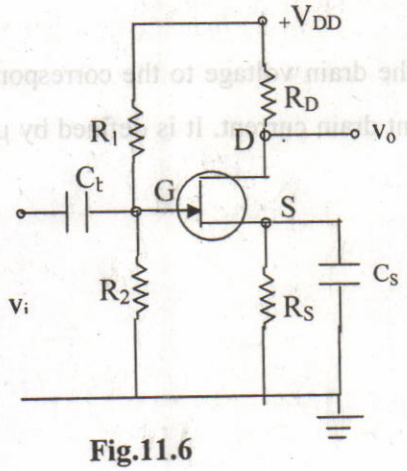


Fig.11.6

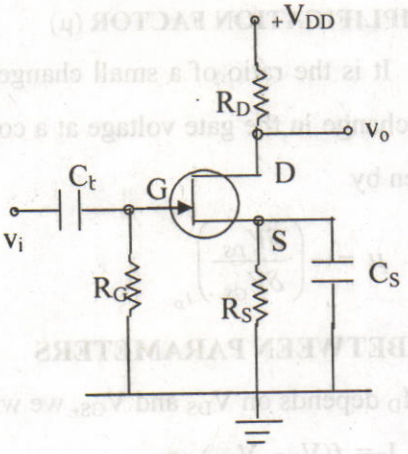


Fig.11.7

A voltage divider arrangement provides voltage V_G at the gate with respect to ground such that

$$V_G = \frac{R_2}{(R_1 + R_2)} V_{DD} \qquad \text{-------- (11.6.1)}$$

A by-passed source resistance R_S is used such that, the DC voltage at the source with respect to ground is

$V_S = I_D R_S$ (Since $I_C \approx 0$) --------- (11.6.2)

is negatively feedback to gate.

$$\therefore V_{GS} = V_G - V_S \qquad \text{---------- (11.6.3)}$$

The values of R_1 and R_2 are selected in such a way that V_{GS} is always a negative quantity. The capacitor C_S is used to ground AC negative feedback.

(2) SELF BIAS

Fig.11.7 shows the circuit diagram of self bias arrangement per an N-channel JFET. Since the gate is returned to ground through a high resistance (>1MΩ), there is no gate current, and voltage on the gate due to the presence of Rg is zero. It provides DC return path.

Hence voltage at source with respect to ground is

$$V_S = I_D R_S$$

$$\therefore V_{GS} = V_G - V_S$$

$$= 0 - I_D R_S = -I_D R_S$$

The capacitor C_S is used to by pass the AC signal voltages. The value of Rg is so chosen that the gate is reversed biased.

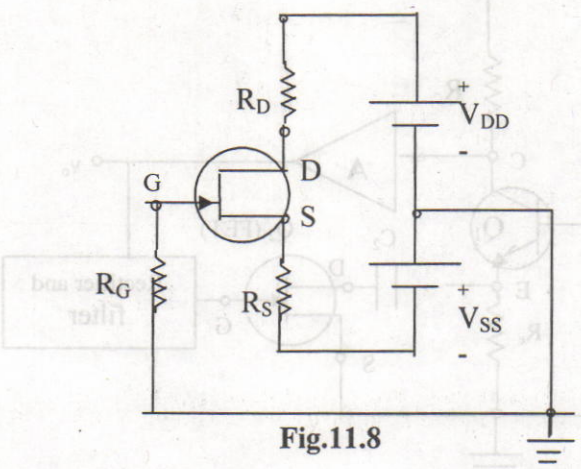


Fig.11.8

(3) SOURCE BIAS

The circuit diagram of source bias for N-channel JFET is shown in Fig.11.8. Here two independent power supplies are used, one for source and the other for drain.

11.7 APPLICATIONSS OF JFET

1. FET is used in the tuners of radio and TV receivers.
2. It is used in electronic voltmeters due to its high input impedance.
3. It is used as a buffer amplifier.
4. It is used in LSI circuits and computer memories due to their small size.
5. It is used in FM modulators.

FET as a Voltage Variable resistor (VVR)

FET can be operated like a variable passive resistor, it finds applications in many areas where this property is useful. The VVR can be used to vary the voltage gain of a multistage amplifier A as the signal level is increased. This action is called *Automatic Gain Control* (AGC). A typical arrangement is shown in Fig.11.8a. The signal is taken at a high level point, rectified, and filtered to produce a DC voltage proportional to the

output- signal level. This voltage is applied to the gate of FET transistor Q_2, thus causing the AC resistance between the drain and source to change. Thus the gain of the transistor Q_1 to decrease as the output signal level increases. The DC bias conditions of Q_1 are not affected by Q_2 since Q_2 is isolated from Q_1 by means of capacitor C_2.

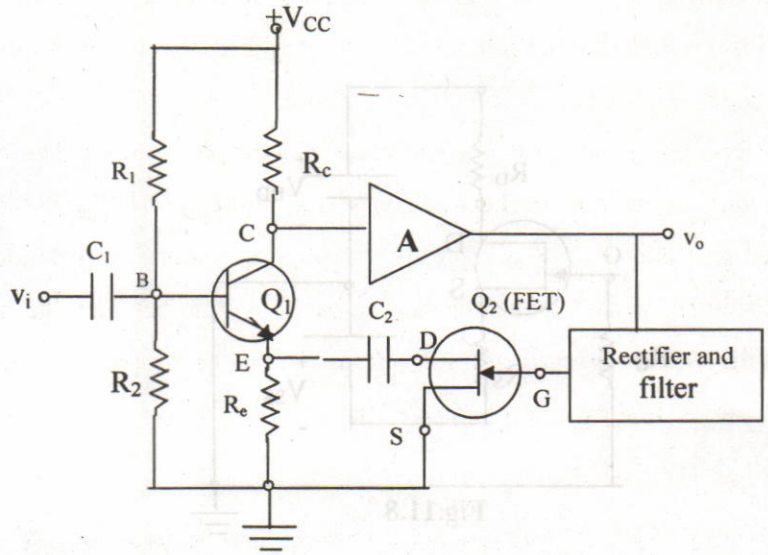


Fig.11.8a AGC amplifier using the FET as a VVR

11.8 ADVANTAGES (or DIFFERENCES) OF FET OVER BJT

FET	BJT
1. Operation depends on the flow of majority carriers.	1. Operation depends on the flow of majority as well as minority carriers.
2. FET is a unipolar device.	2. BJT is a bipolar device.
3. FET exhibits a very high input resistance of the order of MΩ.	3. BJT exhibits a relatively low input resistance of the order of few KΩ.
4. Less noisy.	4. More noisy.
5. Simpler to fabricate and occupies less space.	5. Relatively difficult to fabricate and occupies more space.
6. FET is a voltage driven device.	6. BJT is a current operated device.
7. Exhibits a high degree of isolation between input and output.	7. Exhibits low degree of isolation between input and output.
8. Consumes less power.	8. Needs comparatively more power.

11.9 THE FET SMALL SIGNAL MODEL

Fig.11.9 shows the low frequency small signal model of FET .This has a Norton's output circuit with a current generator whose current is proportional to v_{gs}. The proportionality constant is g_m, r_d is the output resistance. The input resistance between gate and source is infinite because the reverse-biased gate takes no current. Similarly, the resistance between gate and drain is assumed to be infinite.

At low frequencies, there is no feedback from output to input. The capacitor C_{gs} represents the barrier capacitance between gate and source, and C_{gd} is the barrier capacitance between gate and drain. C_ds represents the drain-to-source capacitance of the channel. Because of these internal capacitances, feedback exhibits between the input and output circuits and the voltage amplification drops rapidly as the frequency is increased. The high frequency circuit is shown in the Fig.11.10.

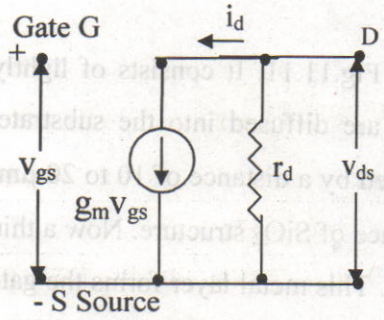


Fig.11.9 FET Low frequency model

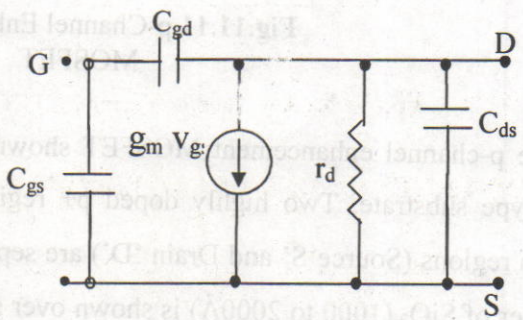


Fig.11.10 FET High-frequency small signal model

11.10 MOSFET (METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR)

MOSFET is the second category of FET. This uses a metal gate electrode separated from semiconductor by an insulating layer of SiO_2. The two types of MOSFETs are:

(1) The enhancement and

(2) The depletion MOSFET.

11.10.1 ENHANCEMENT MOSFET

CONSTRUCTION

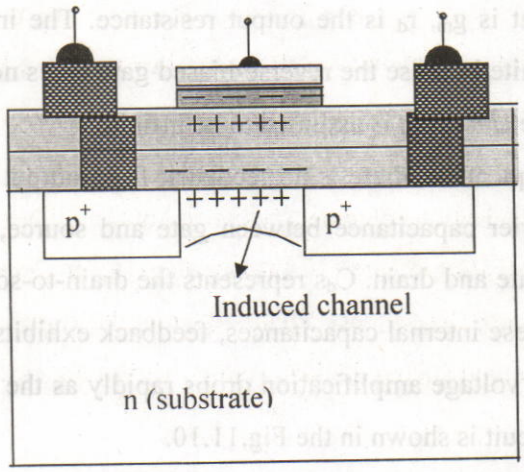
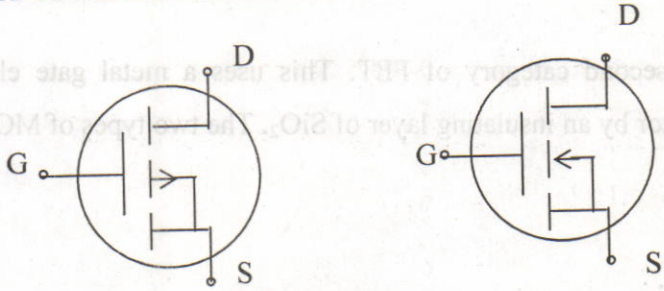


Fig.11.11 p-Channel Enhancement MOSFET

The p-channel enhancement MOSFET shown in Fig.11.11. It consists of lightly doped n-type substrate. Two highly doped p+ regions are diffused into the substrate. These two regions (Source'S' and Drain 'D') are separated by a distance of 10 to 20 μm. A thin layer of SiO_2 (1000 to 2000Å) is shown over surface of SiO_2 structure. Now a thin layer of meal aluminum is formed over the layer of SiO_2. This metal layer forms the gate 'G'. The metal area of the gate acts as one plate and the upper surface of the substrate between the p-regions act as another plate of a parallel plate capacitor and the SiO_2 layer acts as the dielectric.

CIRCUIT SYMBOLS OF MOSFET



p-channel MOSFET n-channel MOSFET

Fig.11.12

An n-channel MOSFET has a similar structure. It has a lightly doped p-type substrate in which two heavily doped n-regions are formed at the two ends by diffusion technique to serve as the source and the drain respectively.

OPERATION

If we ground the substrate as shown in Fig.11.13 and apply a negative voltage at the gate. An electric field will be directed perpendicularly through the sio_2 layer. When the magnitude of the negative voltage on the gate is increased, the induced positive charge in the region (channel) between source and drain is increased the region beneath the oxide has P-type carriers, the conductivity increases and current flows from source to drain through the induced channel. Thus the drain current is enhanced by the negative gate voltage and such a device is called an Enhancement-type MOSFET.

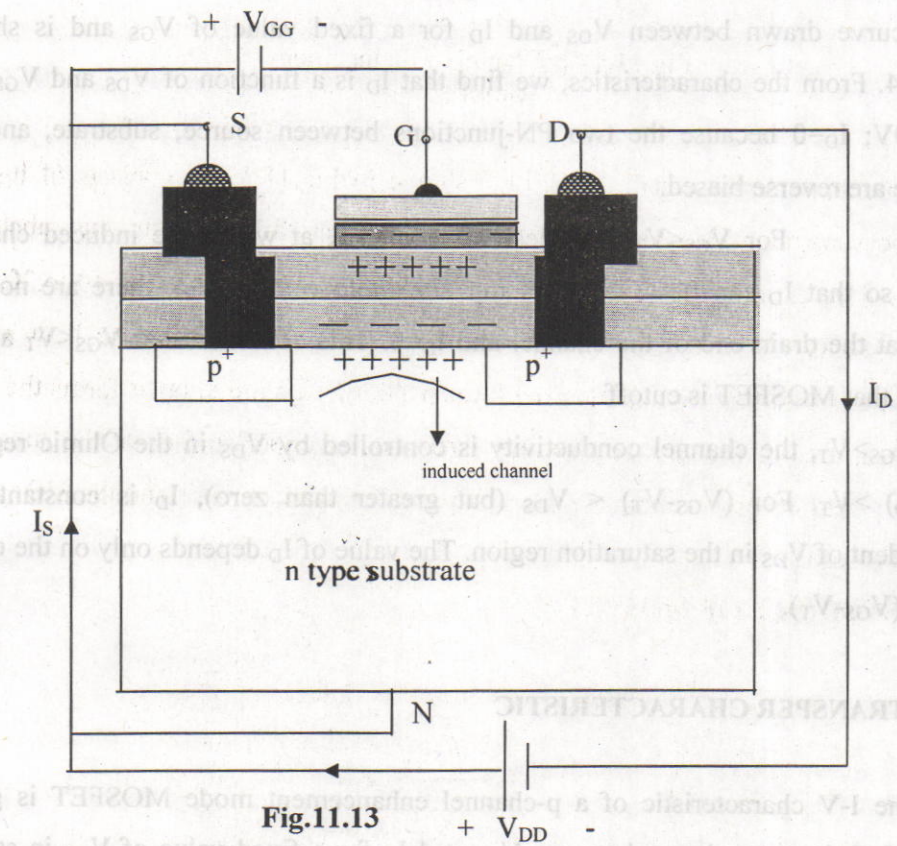


Fig.11.13

11.10.3 I-V CHARACTERISTICS

(1) OUTPUT/DRAIN CHARACTERISTICS

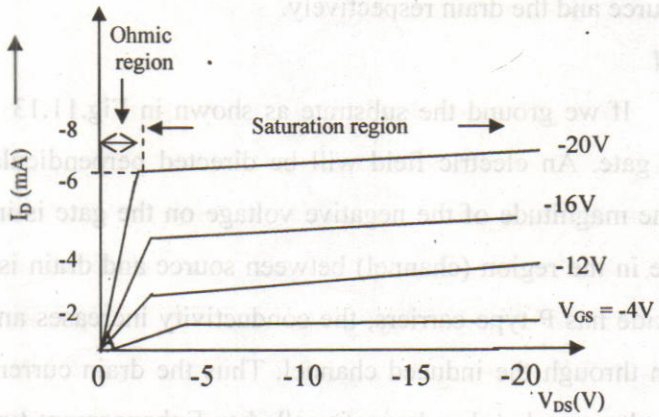


Fig.11.14

It is a curve drawn between V_{DS} and I_D for a fixed value of V_{GS} and is shown in Fig.11.14. From the characteristics, we find that I_D is a function of V_{DS} and V_{GS}. When V_{GS} = 0V; I_D=0 because the two PN-junctions between source, substrate, and drain, substrate are reverse biased.

For $V_{GS}<V_T$ (Smallest value of V_{GS} at which the induced channel is formed, so that I_D can flow, is called the *Threshold voltage* V_T), there are no mobile carriers at the drain end of the channel and I_D=0. This condition that $V_{GS}<V_T$ and I_D=0 signifies that MOSFET is cutoff.

$V_{GS}>V_T$, the channel conductivity is controlled by V_{DS} in the Ohmic region i.e. $(V_{GS}-V_D) > V_T$. For $(V_{GS}-V_T) < V_{DS}$ (but greater than zero), I_D is constant and is independent of V_{DS} in the saturation region. The value of I_D depends only on the effective voltage $(V_{GS}-V_T)$.

(2) TRANSPER CHARACTERISTIC

The I-V characteristic of a p-channel enhancement mode MOSFET is given in Fig.11.15. It is curve drawn between V_{GS} and I_D for a fixed value of V_{DS} in saturation region. The saturation drain current (I_{DSS}) at $V_{GS}\geq 0$ is very small (of the order of few nA). As V_{GS} is made negative, the current (I_D) increases slowly at first, and then much

more rapidly, with an increase in $|V_{GS}|$. The smallest value of $|V_{GS}|$ at which the induced channel is formed so that I_D can flow is called *Threshold voltage* V_{GST} (or V_T).

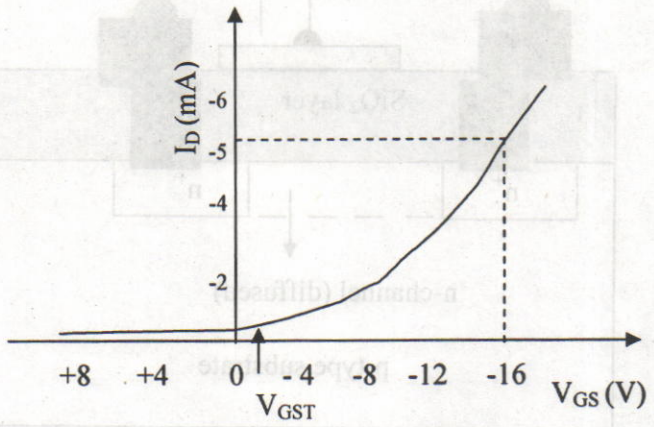


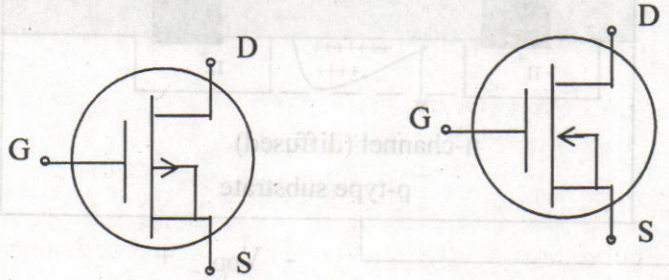
Fig.11.15

11.10.4 DEPLETION MOSFET

CONSTRUCTION

The construction of an n-channel depletion mode MOSFET is shown in Fig.11.17 It consists of a slightly doped substrate of p-type silicon. In the substrates, two highly doped (n+) regions are diffused. One region is known as the source 'S' and the other the drain 'D'. A lightly doped 'n' channel between source and drain regions, is formed by Diffusion. A thin layer of insulating sio2 is grown over the surfaces. Then this layer of metal aluminum is formed over the layer of sio_2. This metal layer covers the entire channel region and it forms the gate 'G' The metallic layer and the upper surface of the substrate between source and Drain regions act as the parallel plates of a capacitor and the sio_2 layer acts as the dielectric medium.

The symbols are shown in Fig.11.16.



p-channel depletion MOSFET

n-channel depletion MOSFET

Fig.11.16 Symbols of depletion MOSFET

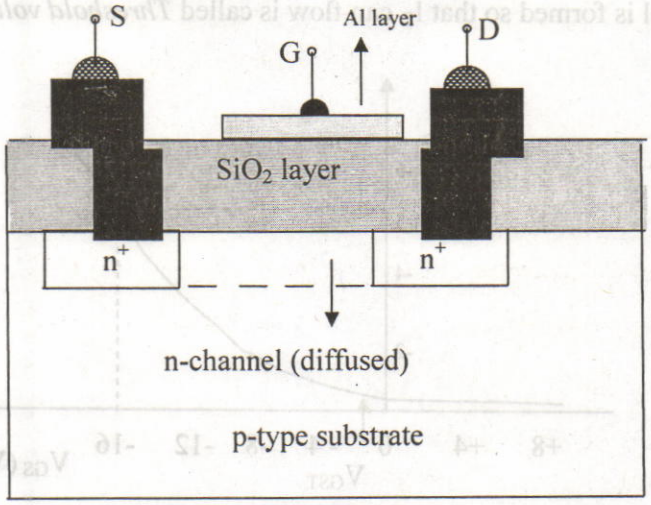


Fig.11.17 n-channel depletion mode MOSFET

11.10.5 OPERATION

The circuit is shown in Fig.11.18. In the depletion mode MOSFET, an appreciable drain current (I_{DSS}) flows for zero gate-to-source voltage ($V_{GS} = 0V$). Now if gate is made negative, positive charges are induced in the channel through the SiO_2 layer of gate capacitor. Since the current in a FET is due to the majority carriers, the induced positive

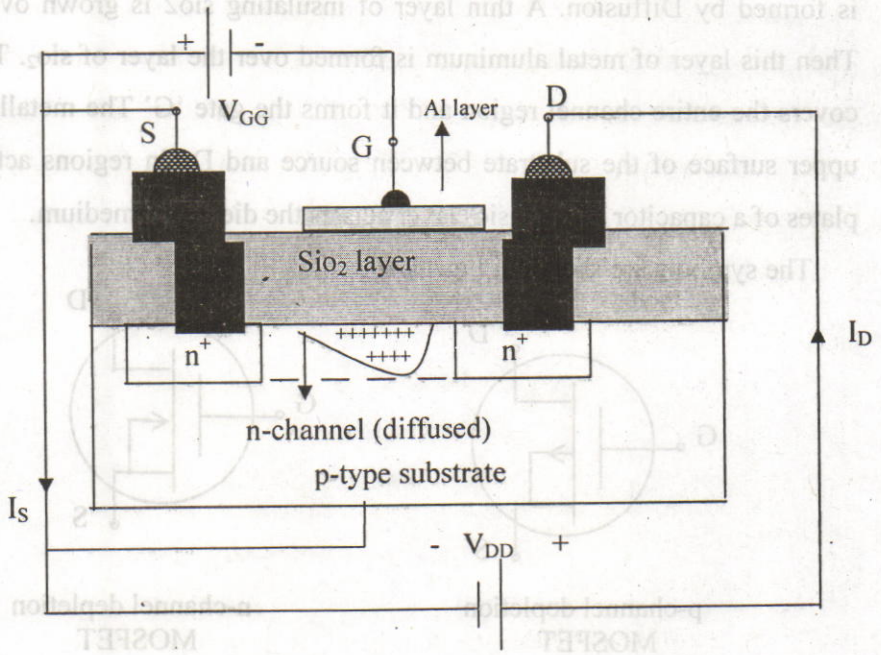


Fig 11.18. n-channel depletion mode MOSFET

charges made the channel less conductive and the drain current drops as V_{GS} is made more –ve. The redistribution of charge in the channel causes an effective depletion of majority carriers, which accounts for the name Depletion MOSFET.

This Depletion MOSFET can be operated even if the gate is made positive .Then these MOSFET can serve as Depletion as well as Enhancement Mode MOSFETs. Because of the voltage drop due to the drain current I_D, the channel region nearest the drain is more depleted than is the volume near the source.

11.10.6 I-V CHARACTERISTICS

(1) OUT PUT/DRAIN CHARACTERISTICS

It is a curve drawn between V_{GS} and I_D for a fixed value of V_{GS} as shown in Fig.11.19. It is seen that the N-channel Depletion mode MOSFET may be operated in either the enhancement mode or the depletion mode as shown in graph. The enhancement mode occurs for positive values of V_{GS} while the depletion mode occurs for negative values of V_{GS}. Hence we can call this MOSFET as the *Dual mode MOSFET.*

(i) **V_{GS} = 0V, V_{DS} is increased from zero**: With V_{GS} = 0V, and the drain is at a positive potential with respect to the source, the majority carriers (electrons) flow through n-channel from source to drain. As the gate is at –ve potential, positive charge of holes is induced in the channel through SiO_2. This positive charge removes mobile electrons from the channel. Hence, as V_{DS} is increased, I_D becomes practically constant.

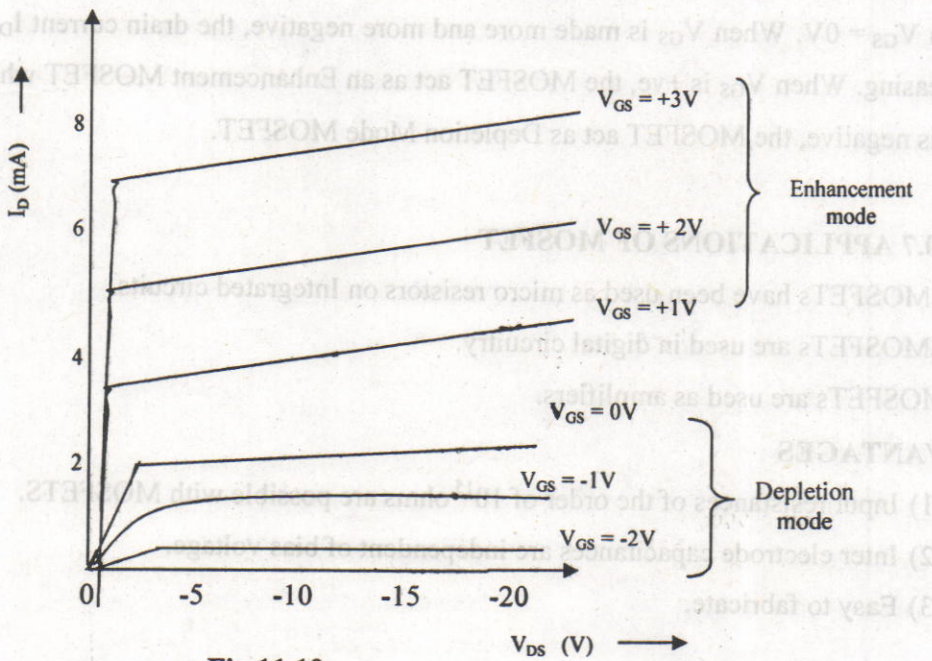


Fig.11.19

(ii) V_{GS} is negative and V_{DS} is increased: When gates is positive with respect to the source, the thickness of the depletion region increases, but the value of I_D is lower.

(iii) V_{GS} is positive and V_{DS} is increased: When gate is positive with respect to the source, the conductivity of the channel is increased due to the induction of negative charge. But now the value of I_D is more than that for V_{GS}=0V.

(2) TRANSFER CHARACTERISTICS

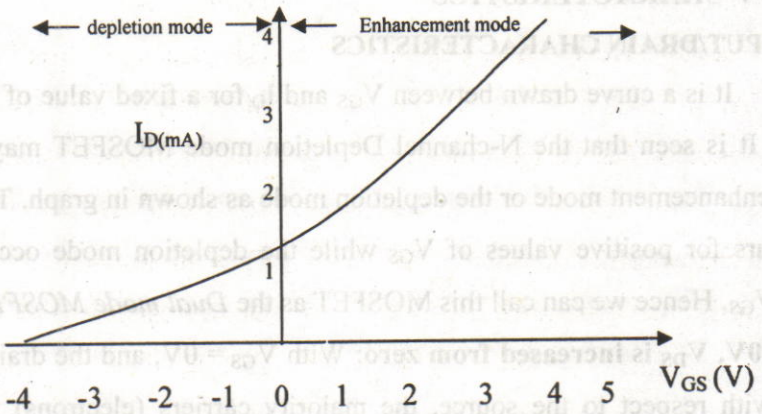


Fig.11.20

It is a curve drawn between V_{GS} and I_D with Drain maintained at +ve potential with respect to source, as shown in Fig.11.20. It may be seen that drain current flows even when V_{GS} = 0V. When V_{GS} is made more and more negative, the drain current I_D goes on decreasing. When V_{GS} is +ve, the MOSFET act as an Enhancement MOSFET while when V_{GS} is negative, the MOSFET act as Depletion Mode MOSFET.

11.10.7 APPLICATIONS OF MOSFET

(1) EMOSFETs have been used as micro resistors on Integrated circuits.

(2) EMOSFETs are used in digital circuitry.

(3) MOSFETs are used as amplifiers.

ADVANTAGES

(1) Input resistances of the order of 10^{15} ohms are possible with MOSFETS.

(2) Inter electrode capacitances are independent of bias voltage.

(3) Easy to fabricate.

11.10.9 DIFFERENCES BETWEEN JFET AND MOSFET

JFET	MOSFET
1. Conductivity of the channel is controlled by the transverse electric field across the reverse biased PN-junction.	1. Conductivity in the MOSFET is controlled by the transverse electric field induced across an insulating layer.
2. Gate leakage current is of the order of 10^{-9}A.	2. Gate leakage current is of the order of 10^{-12}A.
3. Input resistance is of the order of $10^{8}\ \Omega$.	3. Input resistance is of the order of 10^{10} to $10^{15}\ \Omega$.
4. Output characteristics are flatter.	4. They are less flat.
5. Drain resistance is between 0.1 to 1 MΩ.	5. Drain resistance is between 1 to 15KΩ.
6. JFET can be operated in depletion mode only.	6. It can be operated in depletion and enhancement modes.
7. Fabrication is difficult	7. Easy to fabricate

11.11 SUMMARY

FET is semiconductor device. It depends on electric field for the control of current. It has three terminals source that emits carriers, Drain that collects the carriers and gate that controls the carriers. It is a transistor and can work as an amplifier. Its input impedance is high as compared to BJT. It is of the order of MΩ. It can be either JFET or MOSFET. A FET can be used for Integrated Circuit (IC) manufacturing, because it occupies less space. It exhibits high degree of isolation between input and output. MOSFET exhibits still higher input impedance as compared to JFET or BJT. In JFET circuit, Gate is always to be reverse biased. The reverse voltage on the gate creates the depletion region whose thickness can be controlled with the help of reverse voltage changes. JFET possess three parameters like drain resistance, trans conductance,

amplification factor. FET/MOSFET can be used as Buffer amplifier due to its high input impedance and low output impedance. They are used in computer memories.

11.12 KEY TERMINOLOGY

JFET, MOSFET, Trans conductance, drain resistance, Amplification factor, pinch off voltage, Depletion MOSFET, Enhancement MOSFET, Gate, Source, Drain, Biasing, Small signal model.

SOLVED NUMERECAL PROBLEMS

Example.1

An N-channel JFET has a pinch-off voltage of -4.5V and I_{DSS} = 9mA. At what value of V_{GS} in pinch-off region, will I_D equal to 3mA?

Solution:

Given I_D=3mA=3×10^{-3}A ; I_{DSS} = 9mA=9×10^{-3}A; V_P = - 4.5V

From Shockley equation, $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$

Or $3\times10^{-3} = 9\times10^{-3}\left[1-\frac{V_{GS}}{-4.5}\right]^2$

Or $\frac{3}{9} = \left[1+\frac{V_{GS}}{4.5}\right]^2$

Or $\left[1+\frac{V_{GS}}{4.5}\right] = \frac{1}{1.732}$

Or $\frac{V_{GS}}{4.5} = \frac{1}{1.732} - 1$

$= \frac{-0.732}{1.732}$

or $V_{GS} = -4.5\times\frac{0.732}{1.732}$

$= -0.423V \times 4.5 = -1.9V$

Example.2

The Trans conductance of a FET used in voltage amplifier is 3mS and load resistance is 10KΩ. Calculate the voltage amplification of the circuit.

Solution:

Example.3

Following readings were obtained experimentally for a FET. Determine the parameters of FET.

V_{GS}	0V	0V	0.3V
V_{DS}	5V	10V	10V
I_D	8 mA	8.2 mA	7.6 mA

Solution:

(1) When $V_{GS} = 0V$ (constant)

$V_{DS} = 10\text{-}5 = 5V$

$\Delta I_D = 8.2mA\text{-}8mA = 0.2mA$

$$\therefore \text{Drain resistance } r_d = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{5}{0.2mA} = 25\ K\Omega$$

(2) When V_{DS} is constant at 10V

$\Delta V_{GS} = 0.3 - 0 = 0.3V$

$\Delta I_D = (8.2\text{-}7.6)\ mA = 0.6mA$

$$\text{Trans conductance } g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.6\times10^{-3}}{0.3} = 2\ mA/V = 2\ mS$$

(3) Amplification factor $\mu = r_d.g_m$

$$= 25\times10^3\times2\times10^{-3} = 50.$$

11.13 SELF ASSESSMENT QUESTIONS

(I) Long answer questions

(1) Draw and discuss the output and transfer characteristics of JFET?

(2) Explain the construction and working of a FET. How do you determine its characteristics?

(3) Differentiate between FET and BJT. Give the experimental set up to draw FET characteristics?

(4) Discuss the biasing circuits of JFET and define the pinch off voltage of JFET.

(5) Draw the structure of an N-channel MOSFET and explain how depletion region is formed in the channel? Can a depletion type MOSFET be operated in enhancement mode?

(6) Explain the operation of N-channel JFET. Also explain the terms pinch off voltage, on-resistance?

(II) Short answer questions

(1) Mention the advantages of FET over BJT,

(2) Sketch the basic structure of P-channels FET.

(3) Explain the Drain characteristics of FET.

(4) Show the biasing arrangement for a P-channel JFET.

(5) Sketch the small signal model of FET.

(6) Write the constructional details of a MOSFET.

(7) Draw the transfer and drain characteristics of FET.

(8) Give the differences between JFET and MOSFET.

NUMERICEL PROBLEMS

(1) A JFET circuit has the following values VGS = -2V, VDS = 10V.ID = 6 μ A calculate rd, g_m, μ. Ans: 1.66 MΩ, 3m S, 5

(2) Calculate the amplification factor of a JFET whole drain resistance is 32kΩ and trans conductance is 300mS. Ans: $\mu = 9.67 \times 10^3$

(3) For an n-channel JFET, find the values of

(i) I_D (ii)g_m (iii) g_m if I_{DSS} = 6.3mA; Vp =3V, V_{GS}= -1V

Ans: (i) 2.8mA (ii) 4.2mS (iii) 2.8mS

11.14 REFERENCES

(1) Electronic Devices and circuits

- Millman and Halkias (TMH)

(2) Basic Electronics and Linear integrated circuits

- N. N-Bhargava (TMH)

(3) Integrated Electronics

- Millman and Halkias (TMH)

(4) Principles of Electronics

- V.K.Mehta (S.Chand).

UNIT- IV LESSON-12

UNIJUNCTION TRANSISTOR (UJT)

OBJECTIVES OF THE LESSON

.This lesson explains the concepts of an injunction transistor, working current components, characteristics, construction of a basic model, experintal determination of UJT parameters, application of UJT as relaxation oscillator.

STRUCTURE OF THE LESSON

INTRODUCTION

As the name implies, a Uni Junction Transistor has only one PN-junction unlike bipolar junction transistor and unipolar Field Effect Transistor. It is basically a three terminal silicon diode with one emitter and two base terminals. However, it differs from an ordinary diode in that it has three leads. It resembles a FET because in that it has only one PN-junction, but differs from the FET because in normal operation that junction is forward biased in FET. The FET and UJT have also a constructional difference in that the gate surface of FET is much larger than the emitter junction of UJT. It also differs from a FET in that it has no ability to amplify.

Construction of UJT

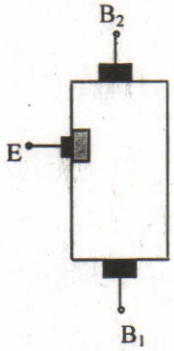


Fig.12.1

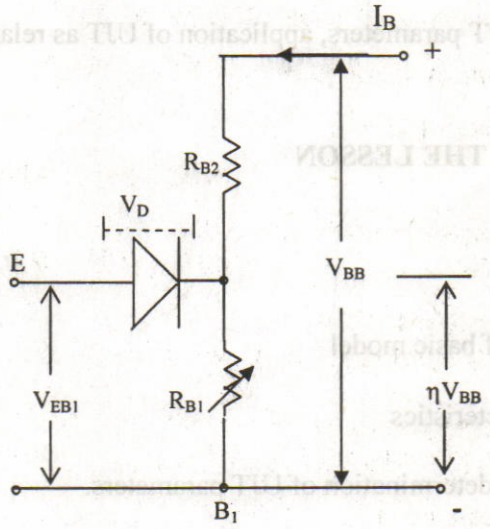


Fig.12.2

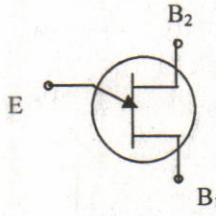


Fig.12.2a UJT Symbol

The UJT is a 3-terminal device, having one emitter junction and two base Ohmic contacts ($Base_1$ and $Base_2$). A PN-junction located between base B_1 and base B_2, is called the Emitter junction.

It consists of a lightly doped N-type silicon bar with a heavily doped P-type material alloyed to its one side (closer to B) for producing single PN- junction. As shown in Fig.12.1, there are 3-terminals, one emitter and two bases B_1 and B_2 at the top and bottom of Silicon bar. The emitter leg is drawn at angle to vertical and

arrow points in the direction of conventional current (*Filament transistor, Double base diode* are the other names of UJT).

A typical set of specifications for the UJT is provided below.

***Absolute maximum ratings* (25^0C):**

- Power dissipation 300 mW
- RMS emitter current 50 mA
- Peak emitter current 2 A
- Emitter reverse voltage 30 V
- Inter base voltage 35 V
- Operating temperature range -65^0C to $+125^0$C
- Storage temperature range -65^0C to $+150^0$C

***Electrical Characteristics* (25^0C):**

		Min.	Typ.	Max.
• Intrinsic stand-off ratio	η	0.56	0.65	
(V_{BB} = 10V)		0.56	0.65	0.75
• Inter-base resistance (kΩ) (V_{BB} = 3V, I_E = 0mA)	R_{BB}	4.7	7	9.1
• Emitter saturation voltage (V_{BB} = 10V, I_E = 50mA)	$V_{E(Sat)}$		2	
• Emitter reverse current (V_{BB} = 3V, I_{B1} = 0)	I_{BO}		0.05	12
• Peak point emitter current (V_{BB} = 25V)	I_P(μA)		0.05	5
• Valley point current (V_{BB} = 20V)	I_V (mA)	4		6

12.3 Explanation of basic model

Fig.12.2 shows the equivalent circuit of the resistance of the silicon bar is called the Inter-Base Resistance (R_{BB}). It is represented by two resistors R_{B1} and R_{B2} in series. R_{B2} is the resistance of Silicon bar between B_2 and the emitter junction. R_{B1} is the resistance of bar and emitter junction. This resistance is shown variable because its value depends upon the voltage across the PN- junction. The PN- junction is represented in the emitter by a diode D. If a voltage V_{BB} is applied between the bases with emitter open, the voltage will divide up across R_{B1} and R_{B2}.

Voltage across R_{B1} is given by

$$V_{RB1} = \frac{R_{B1}}{R_{B1} + R_{B2}} \times V_{BB} \qquad \text{Or} \qquad \frac{V_{RB_1}}{V_{BB}} = \frac{R_{B_1}}{R_{BB}} = \eta$$

The ratio R_{B1} / R_{BB} is called the "*Intrinsic Stand off Ratio*" and designated by η. The value of η lies between 0.51 to 0.82.

$\therefore$ Voltage across $R_{B_1} = \eta V_{BB}$

The voltage ηV_{BB} appearing across R_{B1} reverse biases the diode. Hence emitter current is zero.

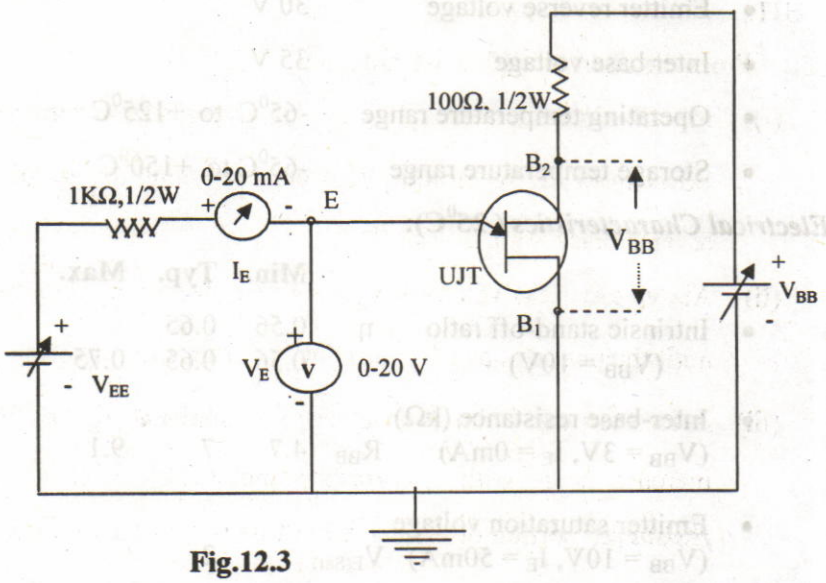


Fig.12.3

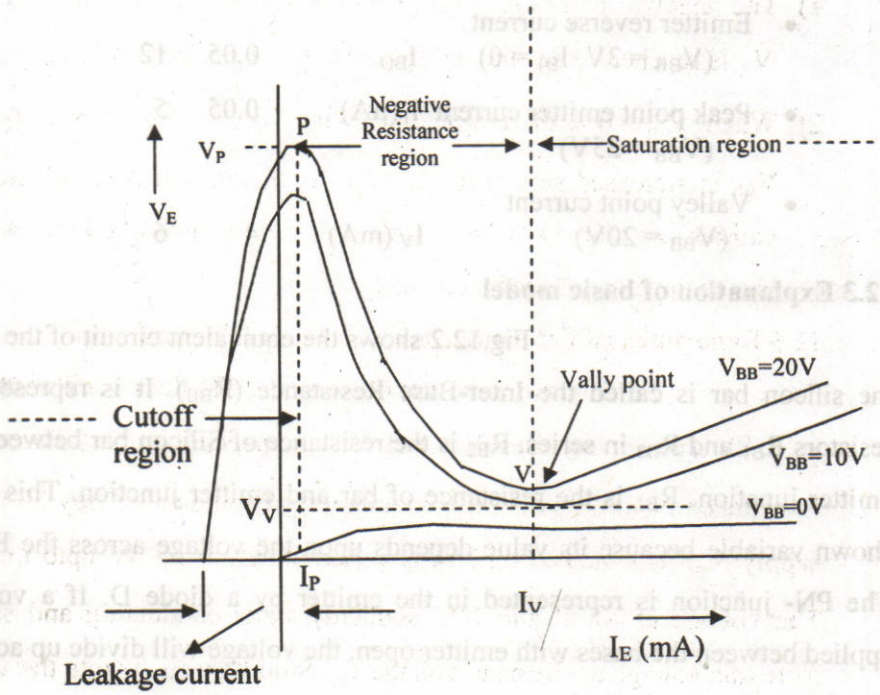


Fig.12.4 UJT Characteristics

The value of emitter voltage which causes the PN-junction to become forward biased is called V_p (peak point voltage), and is expressed as

$$V_P = \eta V_{BB} + V_D$$

Where V_D - forward voltage drop across Silicon diode.

Fig.12.3 shows the circuit diagram for plotting the I-V characteristics of UJT. Fig 12.4 shows the characteristics curves between V_E and I_E of a UJT at different voltages of VBB between two bases. These are kwon as emitter characteristics of UJT.

From the characteristics, we note that

(i) Initially, in the cutoff region, as V_E increases from zero, slight leakage current flows from B_2 to emitter. This current is due to the minority carriers in the reverse biased diode.

(ii) Above a certain value of V_E, forward current I_E begins to flow, increasing until the peak voltage V_P at point P is reached.

(iii) After the peak point P an attempt to increase V_E is followed by a sudden increase in I_E with a corresponding decrease in V_E. This is a ***Negative resistance*** portion of the curve because with increase in I_E , V_E decreases.

1) The negative resistance portion of the curve lasts until the valley point voltage V_V is reached. After the valley point V, the device is driven to saturation.

2) When $V_{BB} = 0V$, there will not be any voltage drop across the bar. But, when V_{EE} is increased slowly till $V_E = 0.7V$, the current is small. But after 0.7V, the emitter junction is strongly forward biased and acts as a perfect conductor. Hence the current shoots up suddenly.

11.5 Experimental determination of UJT parameters

To determine the parameters of UJT, the circuit shown in Fig.12.3 is used. Two power supplies V_{EE} and V_{BB} are needed. At first the power supply V_{BB} is switched on and its output is maintained at some value (say 5V). Now the power supply V_{EE} is switched on and is varied slowly from 0V upto the firing voltage (The voltage at which the UJT suddenly starts conducting and showing current). Note this voltage as the peak voltage V_P. Simultaneously note the valley voltage V_V up to which the peak voltage suddenly drops to. Repeat the above procedure with

other selected value of V_{BB} (say 10V). Tabulate the readings in Table-1 and estimate η using the formula

$$\eta = \frac{V_P - V_D}{V_{BB}}$$

Find the average value of η.

To estimate R_{BB} (another parameter of UJT), identify the $Base_1$ and $Base_2$ leads of UJT and connect an ohmmeter between the two terminals. Now measure the resistance between B_1 and B_2. It may be greater than $5K\Omega$.

Take V_D=0.7V for Silicon UJT.

Table.1

S.No.	V_{BB}	V_P	η
1.	5V		η_1 =
2.	10V		η_2 =

Average value of $\eta = \frac{\eta_1 + \eta_2}{2}$

12.6 UJT Application: Relaxation Oscillator

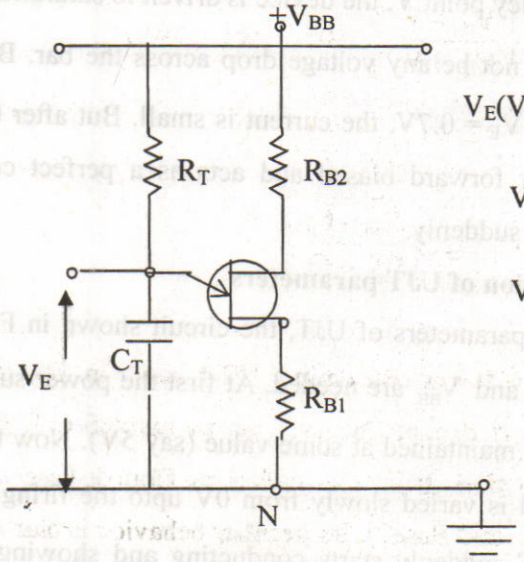


Fig.12.5 UJT Sawtooth generator

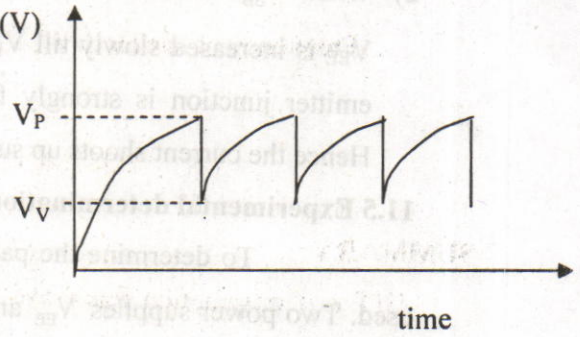


Fig.12.6 Sawtooth output across capacitor

UJT can be used to produce sawtooth waveform by using its negative resistance region as follows.

Fig.12.5 shows the circuit of Relaxation oscillator. Fig.12 .6 is the saw tooth output.

Working

When the power supply (V_{BB}) is switched on, the capacitor C_T charges exponentially through resistor R_T, until the voltage across it reaches the peak point voltage V_P . At this voltage, PN-junction (emitter junction) becomes forward biased and the UJT switches into negative resistance region (i.e. emitter voltage V_E decreases as emitter current I_E increases). The capacitor C_T then quickly discharges through the forward biased PN- junction and R_{B1}. When the voltage across the capacitor decreases to valley point voltage (V_V), the UJT turns off, the capacitor C_T begins to charge again and the process is repeated as shown in Fig.11.6. The frequency of sawtooth wave can be varied by changing either the value of C_T or R_T as they control the time constant R_TC_T of the capacitor changing circuit. Time period of sawtooth waveform (if η is known).

$$T = .R_T.C_T \log_e\left[\frac{V_{BB}-V_V}{V_{BB}-V_P}\right]$$

$$\text{Or } T=2.303R_TC_T \log_{10}\frac{1}{1-\eta} \text{ ---------- (12.6.1)}$$

$$T=2.303R_TC_T \log_{10}\left[\frac{V_{BB}-V_v}{V_{BB}-V_V}\right] \text{ (if } \eta \text{is not known)}$$

$\therefore$ Frequency of sawtooth waveform

$$f = \frac{1}{2.303.R_T.C_T \log_{10}\left[\frac{V_{BB}-V_V}{V_{BB}-V_P}\right]}$$

SUMMARY

UJT is a unijunction transistor. It has one emitter (PN) junction. But it can produce oscillations like transistor. It can not be used as an amplifier. It has a semiconductor bar and one PN-junction. It is also called as Double-base diode because it has two base leads (Base1, and Base2). Its peculiar behavior is that it can exhibit negative resistance region. This region is used to produce oscillations. It possesses two parameters: Intrinsic Stand Off Ratio η; Inter-Base resistance R_{BB}.

The Intrinsic stand off ratio may lie between 0.51 to 0.82. The inter-base resistance R_{BB} is the resistance of the semiconductor bar between $Base_2$ and $Base_1$ and may be greater than 5KΩ. UJT belongs to thyristor family. i.e. it can change from ON to OFF state. The UJT can be used mainly for producing sawtooth waveform. This waveform is used as the horizontal sweep in CRO. The UJT can also be used in timing circuits, in firing silicon controlled rectifiers and in voltage or current regulated power supplies etc.

11.8 KEY TERMINOLOGY

UJT, Intrinsic Stand off ratio, Inter-base resistance, ON state, OFF state, Negative resistance region, Sawtooth wave form.

SOLVED NUMERICAL PROBLEMS

Example.1

A Silicon UJT has 10V between its bases. If the intrinsic standoff ratio is 0.6, find the values of 1. Stand off voltage. 2. Peak-point voltage.

Solution:

Given $V_{BB} = 10$ V; $\eta = 0.6$; $V_D = 0.7$ V

To find Stand off voltage $= \eta V_{BB} = ?$

Peak point voltage $= V_P = ?$

Stand off voltage $= \eta V_{BB} = 0.6 \times 10$ V $= 6$V

$$V_P = \eta V_{BB} + V_D = 6V + 0.7\ V = 6.7\ V$$

Example.2

With a UJT, it is observed that when $V_{BB} = 10$V, $V_P = 7.2$V. Find its intrinsic stand off ratio?

Solution:

Given $V_P = 7.2$ V, $V_{BB} = 10$ V, $V_D = 0.7$ V

To find 'η' $= ?$

We know that $V_P = \eta V_{BB} + V_D$

$$7.2\ V = \eta \times 10 + 0.7$$

$$\therefore 10\,\eta = 7.2 - 0.7 = 6.5\ V$$

$$\therefore \eta = 6.5/10 = 0.65.$$

Example.3

A Silicon UJT has an intrinsic stand off ratio 0.6, intrinsic resistance of 10 KΩ. Find the value of R_{B_1} and R_{B_2} ?

Solution :

Given η=0.6 , R_{BB}= 10 KΩ

To find R_{B_1} = ? , R_{B_2} = ?

We know that $\eta = \frac{R_{B1}}{R_{BB}} \Rightarrow R_{B1} = \eta R_{BB} = 0.6 \times 10\,K\Omega = 6\,K\Omega$.

$\therefore R_{B_2} = R_{BB} - R_{B_1} = 10\,K\Omega - 6\,K\Omega = 4\,K\Omega$.

12.9 SELF ASSESSMENT QUESTIONS

(1) Long answer questions

(1) What is UJT ? Describe the volt-Ampere characteristics of UJT.

(2) Give the constructional details of UJT. Give the experimental setup for UJT characteristics and discuss the characteristics.

(3) Explain the action of UJT as a relaxation oscillator. Give the circuits and draw its output wave form.

(2) Short answer questions

(1) What is UJT ? Give its constructional details.

(2) Define the intrinsic stand-off ratio, inter base resistance. Explain how they are determined experimentally.

(3) Draw the UJT characteristics and mark various region.

(4) Draw the equivalent circuit of UJT and explain it.

NUMERICAL PROBLEMS

(1) A UJT has firing potential of 10V. It is connected across a capacitor if R-C circuit with R = 100KΩ; C = 100 μF. A DC source of 20V is applied to it. Calculate the time period of the saw tooth waveform generated by it.

Ans: 69.31

(2) The intrinsic standoff ratio a UJT is 0.62. If it's inter-base resistance is 7KΩ, what are the values of $R_{B1}$and R_{B2}.

(3) A UJT has 15V between the bases. If η=0.65 find the value of stand off voltage. What will be the peak point voltage if the forward voltage drop in the PN junction is 0.71?

Ans: 9.75

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UNIT -IV **LESSON 13**

SILICON CONTROLLED RECTIFIER

OBJECTIVES OF THE LESSON

This lesson explains the concept of a Silicon Controlled Rectifier, It's construction, Two-transistor representation of SCR; Working of SCR; V-I characteristics; Experimental setup to study the SCR characteristics, Application of SCR as power controller.

STRUCTURE OF THE LESSON

13.1 INTRODUCTION

Addition of third electrode (grid) to the gas diode (two electrode device), and of an electrical starter to the mercury pool tube, allows control of considerable electrical power at higher efficiency. These gas devices are now being superseded by the silicon controlled rectifier and other semiconductor devices, with characteristics similar to the controlled gas tubes, but with even higher efficiency and longer life.

The Silicon Controlled Rectifier (SCR), invented in 1957, is a three terminal semiconductor device and can be used as a controlled switch. It provides current only in one direction and hence it can be described as unidirectional, reverse blocking thyristor. The silicon controlled rectifier is a solid state equivalent of thyratron. The gate, anode, and cathode of SCR correspond to the grid, plate and cathode of thyratron. For this reason, SCR is sometimes called *Thyristor*. This device

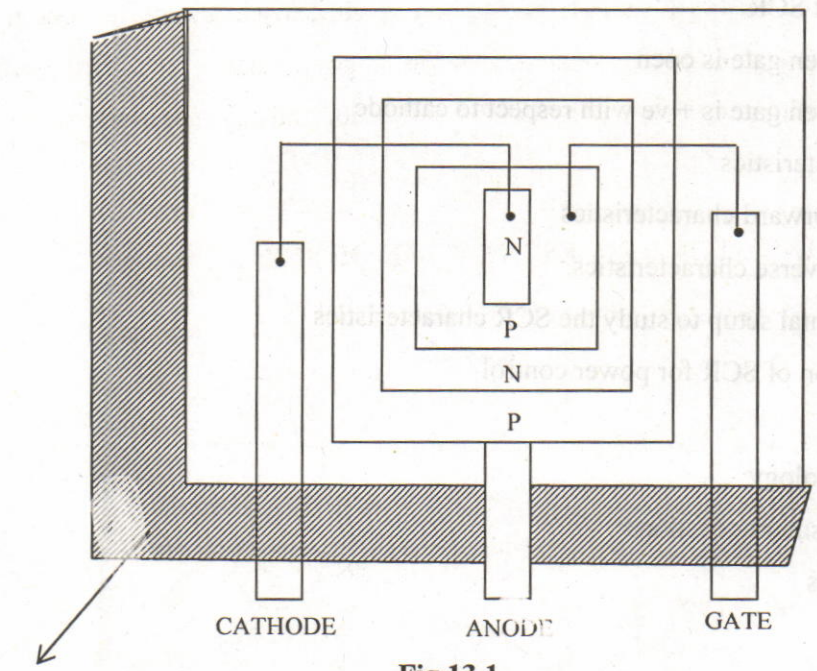

Fig.13.1

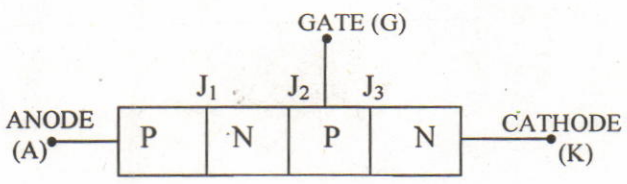

Fig.13.2a

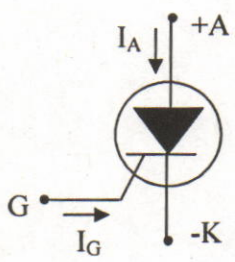

Fig.13.2b

permits the control of heavy alternating and rectified currents as required in welding, lighting, motor control and regulation of rectifiers. The silicon controlled device acts as an electronic switch. This device can handle currents up to hundreds of Amperes.

13.2 CONSTRUCTION

SCR is a four-layer, three-junction, three terminal device, possessing the properties of both diode and transistor. It consists of a four-layer pellet of P-and N-type semiconductor materials. From Fig.13.1, it is essentially an ordinary rectifier (PN junction) and a junction transistor (NPN) combined in one unit to form PNPN device. Three terminals are taken: one from the outer P-type material called *Anode A*, second from the outer N-type material called *Cathode K* and third from the base of the transistor section, called *Gate G*. Symbol is shown in Fig.13.2a. The device is made of Silicon because leakage current in Silicon is very small as compared to Germanium. Since the device is used as a switch, it will carry a leakage current in the off condition which should be as small as possible. It got the name controlled rectifier because it is a Silicon device and is used as a rectifier and that rectification can be controlled.

13.3 TWO TRANSISTOR REPRESENTATION OF SCR

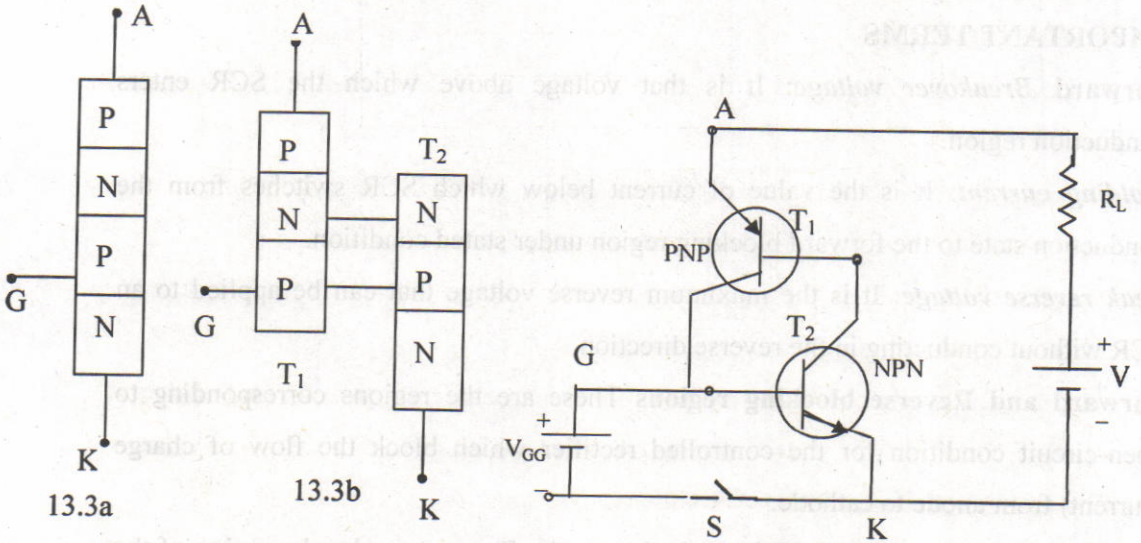

Fig.13.3

Fig.13.3c

The basic operation of an SCR can be described by using two transistor analogy. For this purpose, SCR is split into 3-layer transistor structures T_1 of PNP and T_2 of NPN which are interconnected together. From figure, it is clear that collector of each transistor is coupled to the base of the other, thereby making a positive feedback. The P-N-P-N diode when biased with anode positive has two stable states. One is a very high resistance state typically of the order of 100MΩ, and the other a very low resistance state typically less than 10Ω. When reverse biased this device acts like a typical P-N diode, having a very low leakage current.

Fig.13.3 shows the equivalent circuit of SCR with supply voltage V and load resistance R_L. Suppose the supply voltage V is less than breakover voltage. With gate open (i.e. switch 'S' is open), there is no base current in the transistor T_2. Therefore, no current flows in the collector of T_2 and hence that of T_1. Under such conditions, the SCR is *Open*. However, when switch 'S' is closed, a small gate current will flow through the base of T_2 which means its collector current will increase. The collector current of T_2 is the base current of T_1. Therefore, collector current of T_1 increases. But collector current of T_1 is the base current of T_2. This action is accumulative since an increase of current in one transistor causes an increase of current in the other transistor. As a result of this action, both transistors are driven to saturation and heavy current flows through the load R_L. Under such conditions, the SCR closes.

IMPORTANT TERMS

Forward *Breakover voltage*: It is that voltage above which the SCR enters conduction region.

Holding current: It is the value of current below which SCR switches from the conduction state to the forward blocking region under stated condition.

Peak reverse voltage: It is the maximum reverse voltage that can be applied to an SCR without conducting in the reverse direction.

Forward and Reverse blocking regions These are the regions corresponding to open-circuit condition for the controlled rectifier which block the flow of charge (current) from anode to cathode.

Reverse Breakdown voltage It is equivalent to the Zener or avalanche region of the fundamental two layer semiconductor diode.

12.4 WORKING OF SCR

In an SCR, load is connected in series with anode. The anode is always kept at positive potential with respect to cathode. The working of SCR can be understood under the following two cases.

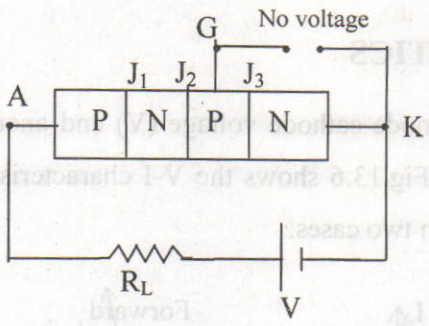

Fig.13.4a

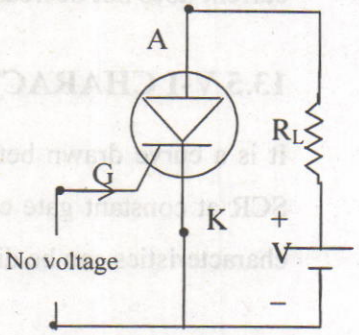

Fig.13.4b

(i) **When Gate is open**: Fig.13.4a shows SCR circuit with gate open, i.e. no voltage applied to the gate. Hence junction J_2 is reverse biased while junction J_1 and J_3 are forward biased. Consequently no current flows through the load R_L and the SCR is *cutoff*. However, if the applied voltage is gradually increased, a stage is reached when reverse biased junction J_2 breaks down. The SCR now conducts heavily and is l to be in the ON state.

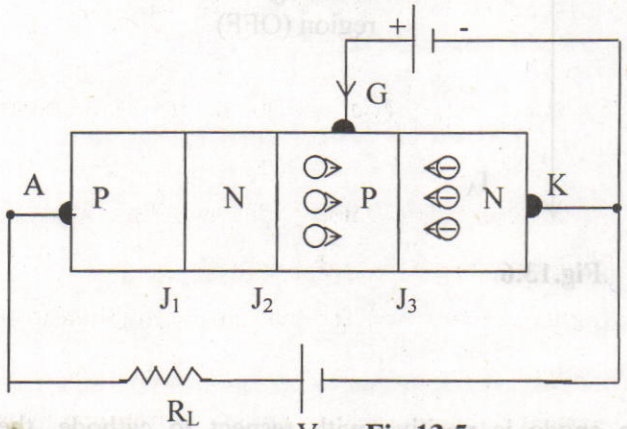

Fig.13.5a

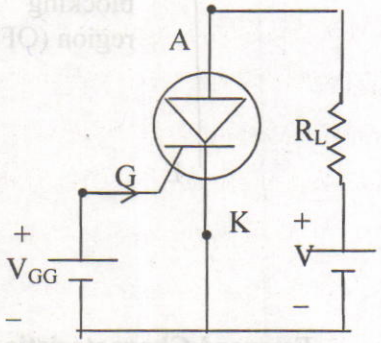

Fig 13,5b

(ii) **When gate is positive with respect cathode:** The SCR can be made to conduct heavily at smaller applied voltages by applying a small positive potential to the gate as shown in Fig13.5a. Now junction J_3 is forward biased and junction J_2 is reverse biased. So the electrons from junction J_3 are attracted towards J_2 and gate current starts flowing. Hence anode current increases. This increased anode current in turn

makes more electrons available at J_2. This process continues and with a small time, junction J_2 breaks down and SCR starts conducting heavily. Once SCR starts conducting, the gate loses all control. Even if gate voltage is removed, the anode current does not decrease at all.

13.5 V-I CHARACTERSTICS

It is a curve drawn between anode-cathode voltage (V) and anode current (I) of an SCR at constant gate current. Fig.13.6 shows the V-I characteristic of an SCR. The characteristics can be divided in two cases.

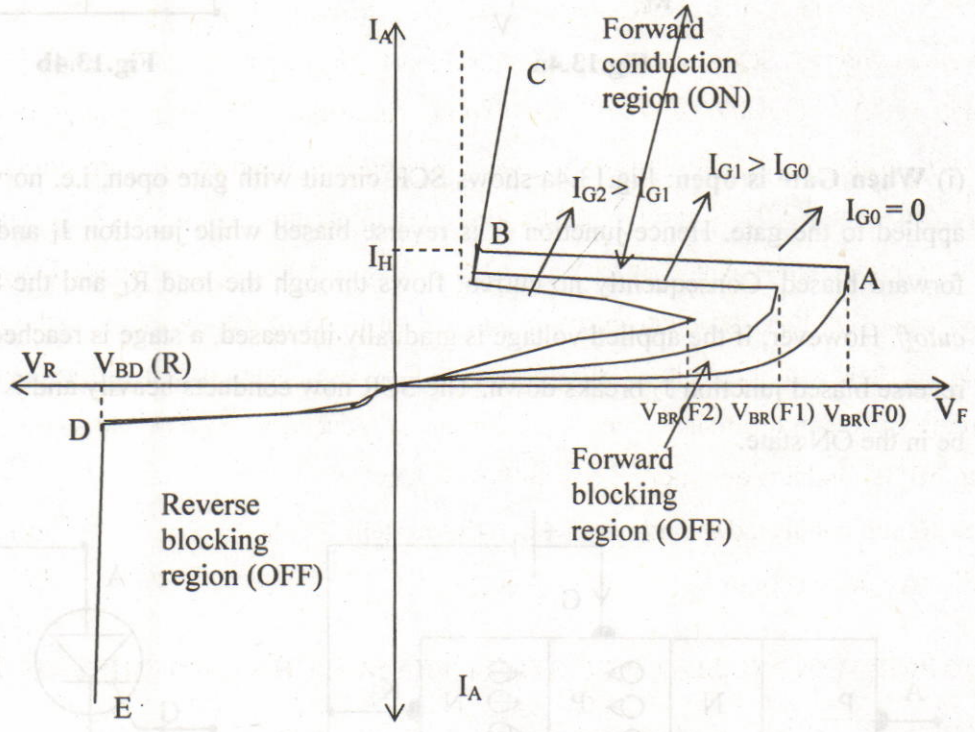

Fig.13.6

Forward Characteristic

When anode is positive with respect to cathode, the curve between voltage (V) and current (I) is called the *Forward characteristic*. In Fig.13.6, OABC is the forward characteristic of SCR at $I_G = 0$. If the supply voltage is increased from zero, a point A is reached when the SCR starts conducting. Under this condition, the voltage across SCR suddenly drops as shown by dotted curve AB. Now most of the supply voltage appears across the load resistance R_L. If proper gate current is

made to flow, the SCR can conduct at much smaller supply voltages. This means that gate current controls the value of forward voltage required to turn ON the SCR.

Reverse Characteristic

When anode is negative with respect to cathode, the curve between voltage (V) and current (I) is called the *Reverse characteristic*. In Fig.13.6, ODE is the reverse characteristic of SCR. If the reverse voltage is gradually increased from zero, at first the anode current (leakage current) remains small and at some reverse voltage, avalanche breakdown occurs and the SCR starts conducting heavily in the reverse direction. This behaviour is shown in the curve by DE. The maximum reverse voltage at which SCR starts conducting heavily is known as Reverse Breakdown voltage. SCRs with currents in excess of 100A and operating voltage up to about 1000V are available. The holding voltage is of the order of magnitude 1V. The ratio of the continuous allowable anode current to the forward gate current required to switch ON is rarely less than several thousands. For example a gate current of less than 50mA will turn on an anode current of 100A. As can be seen from the above discussion, the characteristics of SCR are controlled by anode-cathode voltage and gate–cathode voltage. It is turned on by proper gate current and without exceeding breakdown voltage. The anode current is reduced to holding value while turning off. It conducts only during one half of each cycle

Two SCRs are connected in anti parallel and this system is called a TRIAC. It is used for full wave power control.

12.6 EXPERIMENTAL SETUP TO STUDY THE SCR CHARACTERISTICS

Fig.13.7 shows the circuit diagram of an SCR to draw its anode characteristics. With switch S open, the anode power supply V_{AA} is varied and the anode to cathode voltage V_{AK} is measured as a function of anode current I_A.

The switch S is closed and the experiment is repeated for different gate currents. The readings are noted in the following table. The observations are marked on an ordinary graph paper taking anode voltage V_{AK} values along X-axis and the anode currents (I_A) along Y-axis.

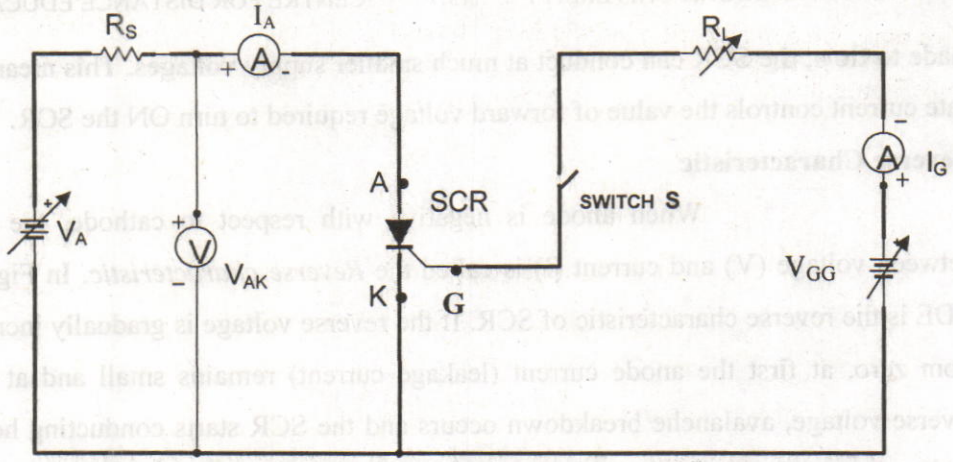

Fig.13.7

Observation table

S.No.	$I_G = 0\ \mu A$		$I_G = 50\ \mu A$		$I_G = 75\ \mu A$		$I_G = 100\ \mu A$	
	V_{AK}	I_A	V_{AK}	I_A	V_{AK}	I_A	V_{AK}	I_A
1.								
2.								
3.								
4.								
5.								
6.								

13.7 APPLECATION OF SCR

SCR for power control

Fig.13.8 shows a common circuit for controlling power in the load R_L. During the positive half-cycle of A.C supply, end A is positive and end B is negative. Therefore capacitor C_2 is charged through $AD_1RC_2D_4B$. The charge on capacitor C_2 depends upon the value of potentiometer R. When the capacitor C_2 is charged to a sufficient voltage, it discharges through the Zener diode. This gives a pulse to the primary and hence to the secondary of transformer T_2. This pulse turns on SCR_2 which conducts current through load R_L. During negative hale cycles, it discharges through the Zener diode and fires SCR_1 which conducts current through the load.

The angle of conduction can be controlled by the potentiometer R. The greater the resistance of R, lesser is the voltage across C_1 or C_2 and hence smaller will be the time during which SCR_1 and SCR_2 will conduct in a full cycle. In

this way, we can control a large power of several KW in the load R_L with the help of a small potentiometer "R"

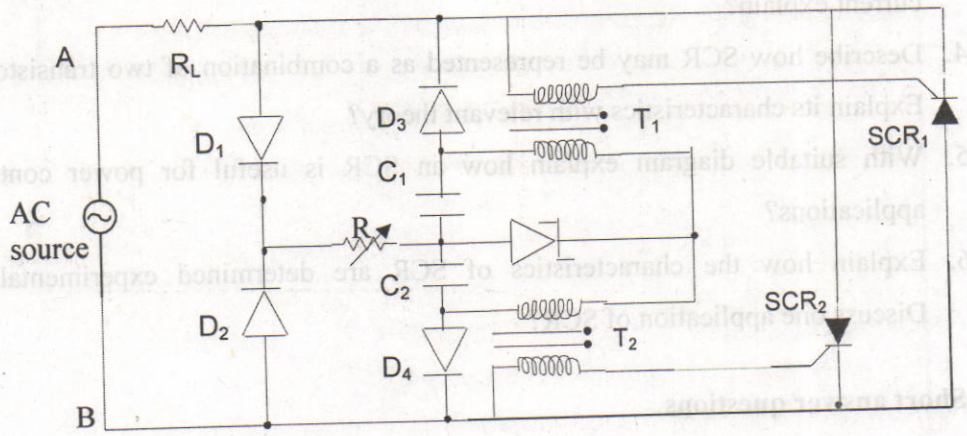

Fig.13.8

Other applications of SCR are in light dimming circuits, battery chargers, phase control systems, temperature control etc.

SUMMARY

SCR is a silicon controlled rectifier. It is a silicon four layer, three terminal device. It is a rectifier, whose characteristics are controlled by anode-cathode voltage and gate-cathode voltages. SCR is a single polarity device. It conducts only during one half-cycle of each cycle and energy is wasted in the other half cycle. It is used as a static switch in phase control system, for temperature control, in energy lighting circuits, in battery charger for regulation, to supply rectified current and in light dimming circuits.

13.9 KEY TERMINOLOGY

SCR, breakdown voltage, forward breakover voltage, reverse breakdown voltage, holding current, gate, anode, and cathode.

13.10 SELF ASSESSMENT QUESTIONS

I. Long answer questions

1. Describe the construction and working of SCR. What do you infer from the characteristics?

2. What is an SCR? Give its symbol and two transistor representation. Mention the applications?
3. Draw the VOLT-AMPERE characteristics of the SCR as a function of gate current explain?
4. Describe how SCR may be represented as a combination of two transistors. Explain its characteristics with relevant theory?
5. With suitable diagram explain how an SCR is useful for power control applications?
6. Explain how the characteristics of SCR are determined experimentally. Discuss one application of SCR?

II. Short answer questions

1. What is the basic function of SCR?
2. Describe the construction of SCR and its characteristics?
3. Sketch the V-I characteristics of SCR?
4. What is the principle of SCR?
5. Give two applications of SCR?
6. Explain how SCR is used for power control?
7. Draw the experimental set up to obtain SCR characteristics?
8. Draw two transistor representation of SCR. Mention two applications?

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UNIT IV **LESSON -14**

PHOTO ELECTRIC DEVICES

OBJECTIVES OF THE LESSON

This lesson explains the Photoelectric effect and its theoretical background; Photoconductive cell (or LDR), working characteristics and spectral response; Photo voltaic cells, their construction, working; Concept of Photo diode, Photo transistor, LED, Solar cell; their construction, characteristics, applications.

STRUCTURE OF THE LESSON

14.1 INTRODUCTION

Optoelectronics is an area that combines electronics with optical technology. The emergence of the field of electronics has produced a variety of devices that either produces light or respond to light. These devices are classified as either light emitting [ex: LED] or light activated. [Ex: LDR, solar cell, photo diode]

14.2 PHOTO ELECTRIC EFFECT

Definition: The liberation of electrons from matter under the influence of light is known as ***P***hoto ***E***lectric ***E***ffect.

This phenomenon was first observed by Hertz in 1847. Photo electric effect includes the liberation of electrons from a metallic surface and also the generation of electron-hole pairs in semiconductor when these materials are subjected to radiation.

The photoelectric effect was successfully explained by Einstein in 1905 with the help of quantum theory of light.

THEORY

Planck made the fundamental assumption that radiant energy is not continuous but can exist only in discrete quantities called ***Quanta*** or ***Photons***. He also assumed that associated with the light of frequency f, there are number of photons, each of which has an energy hν Joules. The greater the intensity of light, the larger the numbers of photons present, but the energy of each photon remains unchanged.

Consider a monochromatic radiation of frequency (ν) and energy hν, incident on a metal/photo sensitive surface. When a photon strikes the electron on the surface, it absorbs part of energy to get released from the atom. This energy is known as the *Photo Electric Work Function* of the metal W_0. The remaining energy is taken up by the electron in the form of kinetic energy. Hence, we can write

$$h\nu = W_o + \frac{1}{2}mv^2 \qquad \text{.....(14.2.1)}$$

Eq.(14.2.1) is the Einstein photo electric equation.

$$h\nu = h\nu_o + \frac{1}{2}mv^2$$

$$= h\nu_o + eV_r$$

or $$eV_r = h\nu - h\nu_o$$

$$= h\left[\frac{C}{\lambda} - \frac{C}{\lambda_0}\right] = hC\left[\frac{1}{\lambda} - \frac{1}{\lambda_0}\right]$$

Or $$V_r = \frac{hC}{e}\left(\frac{1}{\lambda} - \frac{1}{\lambda_0}\right)$$ ---------- (14.2.2)

When the metal is given a negative potential, it repels electrons. The negative potential given to metal (plate), which stops the most energetic photo electron from reaching the plate is called the "*Stopping Potential* ". V_r is given by the Eq.(14.2.2).

EXPERIMENTAL ARRANGEMENT TO STUDY PHOTO ELECTIC EFFECT

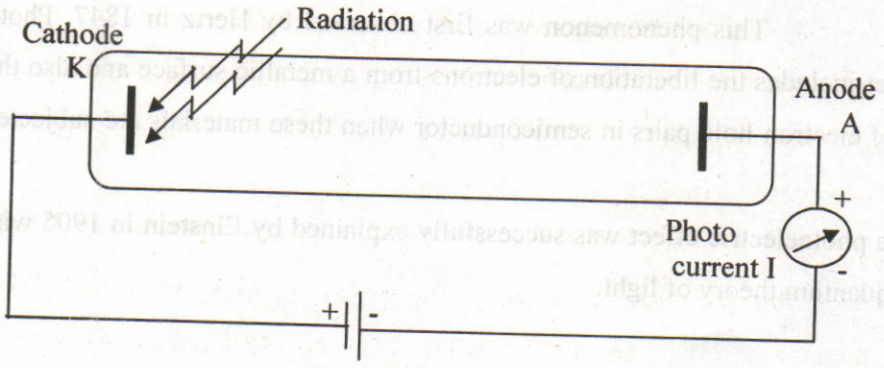


Fig.14.1

Consider the arrangement shown in Fig.14.1. When light falls on the surface of the photo metal (cathode), the photo electrons are emitted by the surface. These electrons reach the anode and results in a current. This photo electric effect depends upon

i. The potential difference between the electrodes

ii. The intensity of radiation.

iii. The frequency of radiation.

iv. The photo metal (cathode) used.

WORK FUNCTION

The work function of a photo metal is defined as the minimum amount of energy required to liberate electron from the atom.

PHOTO CONDUCTIVE EFFECT

Definition: The phenomenon of increase in electrical conductivity of a semiconductor when exposed to radiation is known as **Photo Conductivity**.

Explanation: If radiation falls upon a semiconductor, its conductivity increases. This is explained as follows.

The conductivity σ of a semiconductor increases with the increase of concentration of charge carriers, according to the relation

$$\sigma = (n\mu_n + p\mu_p)e$$

where n = magnitude of free electron concentration

p = magnitude of hole concentration

μ_p = hole mobility

μ_n = electron mobility

e = electron charge

If the radiation, possessing energy hν (greater than E_g), falls on a semiconductor, this will be utilized to break the covalent bonds. As a result, new electron-hole pairs are created in excess of those generated thermally. These increased current carries decrease the resistance of the material and hence such a devise is called a ***Photo Resistor*** or a ***Photo Conductor*** or a ***Light Dependent Resistor*** (*LDR*).

Consider the case of a semiconductor containing both donor and acceptor impurity atoms. Fig.14.2 shows the energy band diagram of such a semiconductor. If photons of sufficient energy illuminate this material, the following three transitions are produced.

(a) An electron-hole pair can be created by a high energy photon in an intrinsic excitation.

(b) A photon may excite a donor electron into the conduction band.

(c) Valence electron may go into an acceptor state.

These transitions [(b) & (c)] are known as *Impurity excitations*. Since the density of states in conduction band and valance band greatly exceeds the density of impurity states, photo conductivity is due to intrinsic excitation.

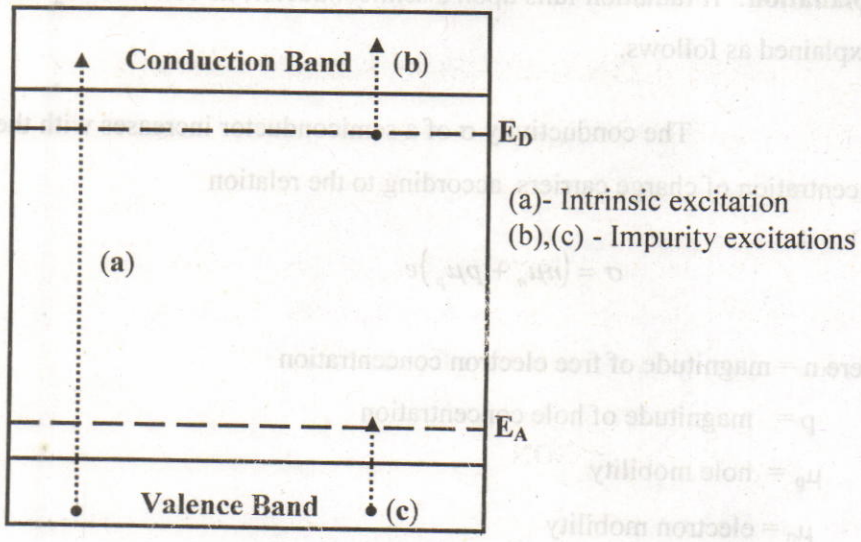


Fig.14.2

14.4 PHOTO CONDUTIVE CELL

Photo con ıctive cell is a semiconductor device whose resistance varies inversely with intensity of light that falls upon its photo sensitive material. Photo conductive cells are made up of CdS, PbS or Se.

The mostly used cell is the CdS (Cadmium Sulphide) cell. The sensitive area of this device consists of a layer of chemically deposited CdS, which may contain a small amount of Silver, Antimony or Indium impurities. Following Fig.14.3 shows its constructional details.

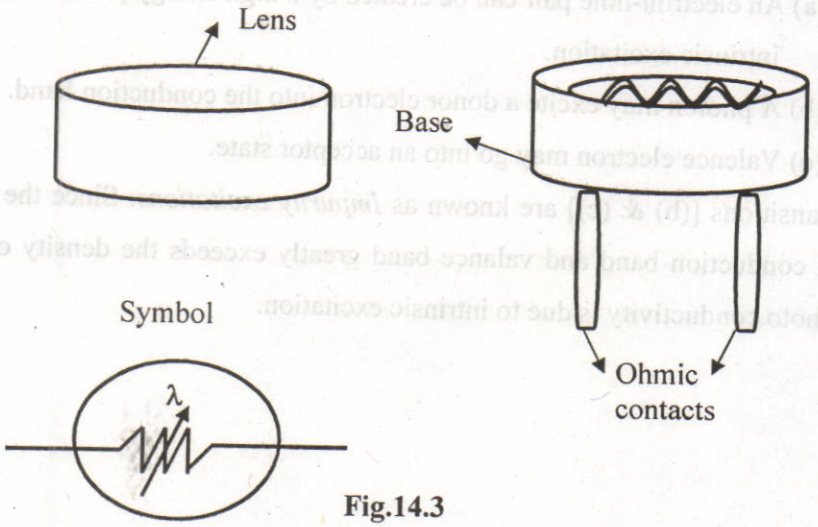


Fig.14.3

WORKING

When the cell is not exposed to any radiation, its resistance is maximum called the ***dark resistance***. It may be as high as 20MΩ or more. When stimulated with strong light, the cell resistance may be less than 10Ω. Fig.14.4 shows the behaviour of a photo conductive cell at various light intensities.

GRAPH

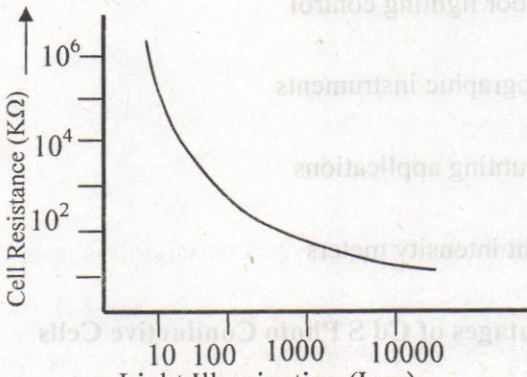


Fig.14.4

14.4.1 SPECTRAL RESPONSE OF CdS CELL

Any opto electronic device that is light activated rather than light emitted, responds to a certain range of wavelength. This characteristic is known as the ***Spectral response***. The spectral response of the CdS photo conductor is shown in Fig.14.5. Like human eye, the response is best over the visible spectrum.

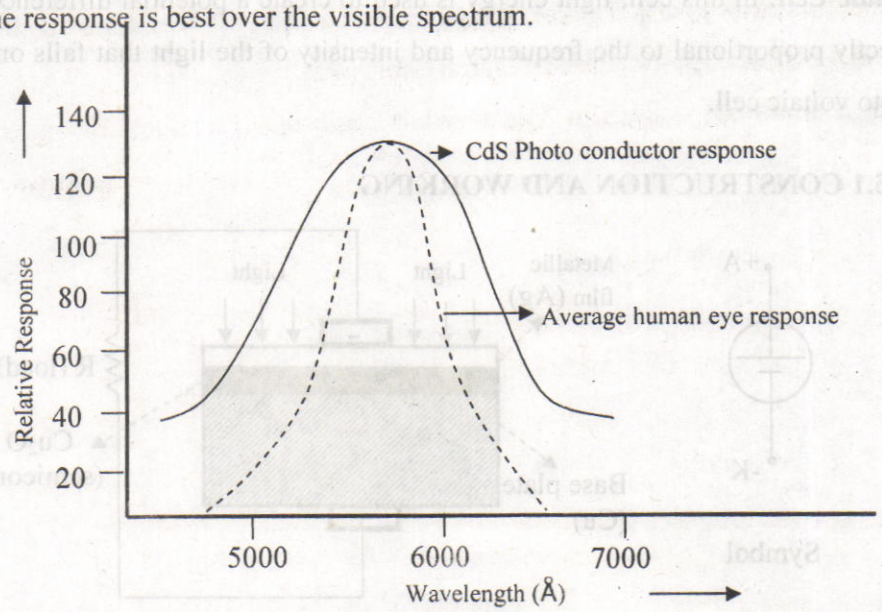


Fig.14.5

17,

14.4.2 APPLICATIONS

Photo conductive cells are used in

1 Smoke detectors

2 Burglar Alarms

3 Outdoor lighting control

4 Photographic instruments

5 In counting applications

6 In light intensity meters

14.4.3 Advantages of Cd S Photo Conductive Cells

1. High dissipation capability
2. Low resistance when stimulated by light

14.5 PHOTO VOLTAIC CELLS

The process of converting light energy directly to electrical energy is called the ***Photo Voltaic Effect.*** The device or cell, which is based on this property, is called a ***Photo Voltaic Cell.*** In this cell, light energy is used to create a potential difference which is directly proportional to the frequency and intensity of the light that falls on the basic photo voltaic cell.

14.5.1 CONSTRUCTION AND WORKING

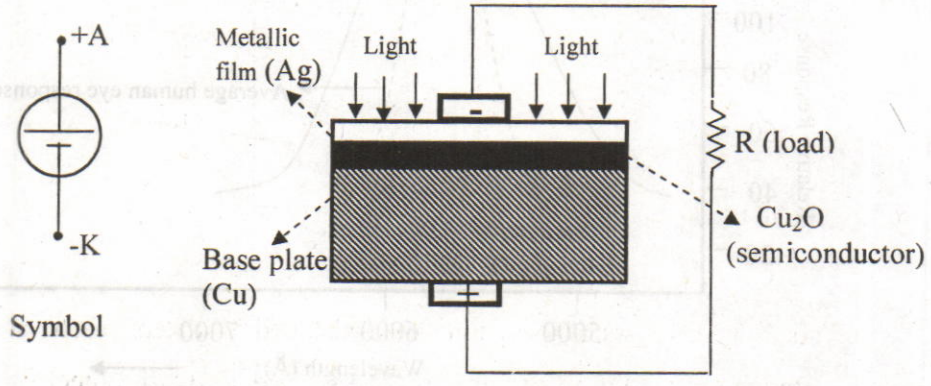


Fig 14.6 Photo voltaic cell

A photo voltaic cell consists of a thin metallic film of silver, gold or platinum deposited on a semiconducting layer [like cuprous oxide]. The whole arrangement is then attached to a metal base plate (copper) as shown in Fig.14.6

WORKING

When light falls on a metallic film 'F' at the barrier layer between the metallic film and the semiconductor, photo electric emission occurs. The photo electrons so emitted from the layer move towards the metallic film. Consequently, the metallic film F becomes negatively charged. Hence a potential difference is developed between the two and current flows in the external circuit. The strength of this current is proportional to the intensity of light and flows without any bias.

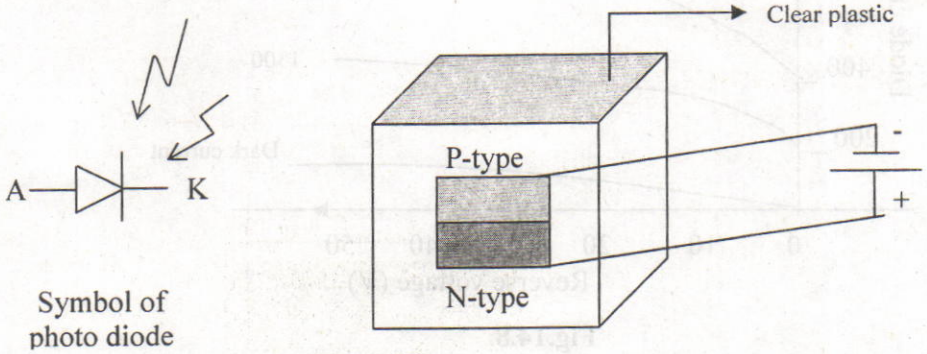
14.5.2 APPLICATIONS

1. In photographic exposure meter
2. For operation of relays
3. Direct reading illumination meters

14.6 PHOTO DIODE

The photo diode is a PN- junction device that depends on reverse bias. If this reverse biased PN junction is illuminated, the current varies almost linearly with the light.

14.6.1 CONSTRUCTION



Symbol of photo diode

Fig.14.7

This diode consists of a PN junction embedded in a clear plastic as shown in Fig.14 . Radiation is allowed to fall upon one surface across the junction through a small transparent window. The remaining sides of the plastic are either painted black

or enclosed in a metallic case. The entire unit is extremely small and has dimension of the order of one tenth of an inch.

14.6.2 WORKING

With no incident light, if reverse voltages [> few tenths of a Volt] are applied, an almost constant current independent of the magnitude of the reverse bias is obtained. This dark current corresponds to the reverse saturation current due to the thermally generated minority carriers. These minority carriers "fall down" the potential hill at the junction, whereas this barrier does not allow majority carriers to cross the junction.

Now, if light falls upon the surface, additional electron-hole pairs are formed (since the concentration of majority carriers greatly exceeds that of minority carriers, the percent increase in majority carriers is much smaller than the percent increase of minority carriers). Hence, we consider the radiation solely as a minority-carrier injector. These injected minority carriers (i.e in P-side) diffuse through the junction, cross it and contribute to the current. The I-V characteristics of a photo diode are shown in Fig.14.8.

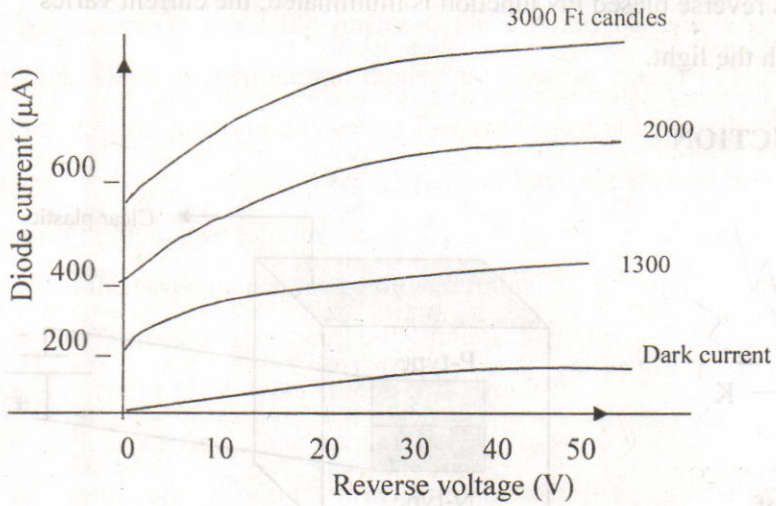


Fig.14.8

The curves do not pass through the origin. The slope of the curves corresponds to a dynamic resistance of MΩ to hundreds of MΩ.

14.6.3. DIFFERENCES BETWEEN A PHOTODIODE & ORDINARY DIODE

Photo diode	Ordinary diode
1. Transparent in appearance.	1. Opaque in appearance.
2. Junction is exposed to radiation.	2. Junction is not exposed to radiation.
3. Reverse current is a function of light intensity.	3. Reverse current is a function of temperature.
4. Always used in reverse bias condition.	4. Mostly used in forward bias condition.

14.6.4 APPLICATIONS

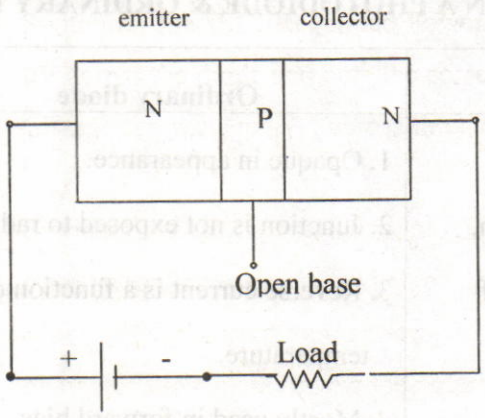
1. A photo diode can be used as a variable resistance device controlled by light intensity.
2. It is used in light operated switches.
3. It is used in optical communication system.
4. It is used in instrumentation.

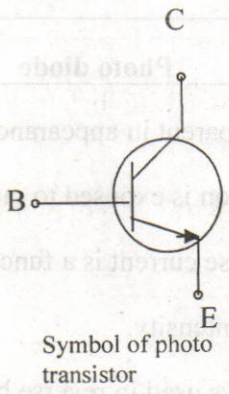
14.7 PHOTO TRANSISTOR

Definition: A photo transistor is an optoelectronic device that has more sensitivity to light than a photo diode.

14.7.1 Construction

Photo transistors have a large base-collector junction as the light collecting element. A transistor with an open base has a small collector current, consisting of thermally generated minority carriers. By exposing the collector junction to light, a manufacturer can produce a photo transistor. They have a lens built into the package to focus radiation on to the collector junction, as shown in Fig.14.9c.





Symbol of photo transistor

Fig.14.9a

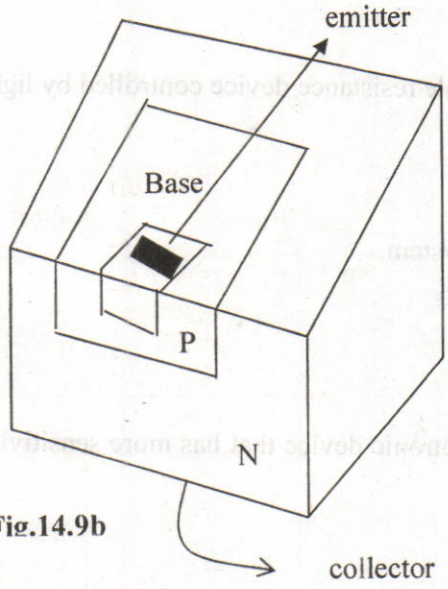


Fig.14.9b

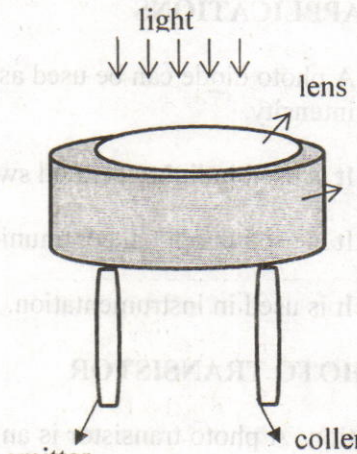


Fig.14.9c

14.7.2. Working

The photo transistor has a light-sensitive collector-to-base PN-junction. It is exposed to incident light through lens-opening in the transistor package.

When there is no incident light, there is a small thermally generated collector-to-emitter leakage current, I_{CEO}. This is called the *dark current* and is in the mA range. When light strikes the collector-base P-N junction, a base current I_{λ} is produced. This is directly proportional to the light intensity. This action produces a

collector current which increases linearly with I_λ according to the relation in equation

$I_C = \beta I_\lambda$

The photo transistor behaves as a conventional BJT. In many cases, there is no connection to base.

14.7.3 Characteristics of a photo transistor

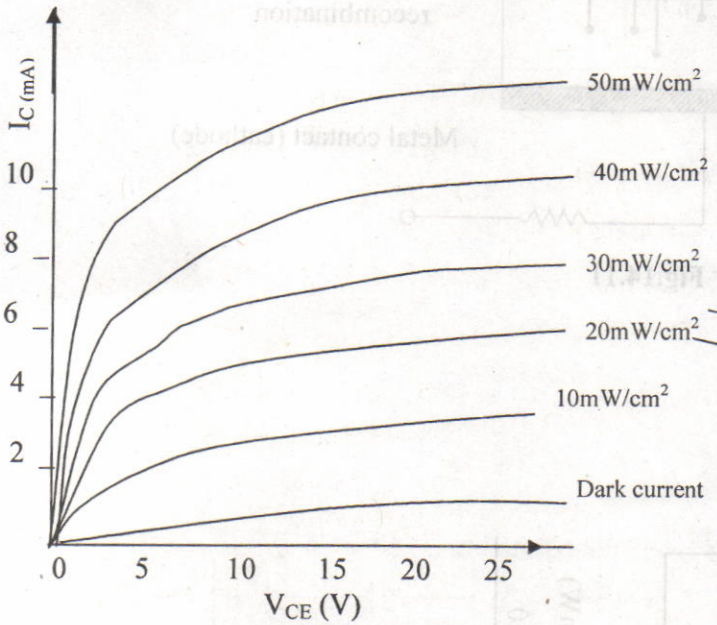


Fig.14.10 b

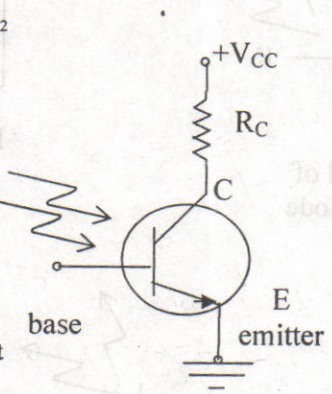


Fig.14.10a

14.8 LIGHT EMMITING DIODE [LED]

LED:LED stands for Light Emitting Diode. It is a forward biased PN junction which emits visible light when energized. The amount of light output is proportional to the forward current

14.8.1 CONSTRUCTION

An N-type layer in grown on a substrate and a P-type layer is deposited on it by diffusion. The metal anode connections are made at the outer edges of P-layer so as to allow more central surface area for the light to escape. A metal film is applied to the bottom of the substrate for reflecting as much light as possible to the surface of the device and also to provide cathode connection. LEDs are manufactured with domed lenses. The semiconductor material used in LED are Gallium Arsenide (GaAs)

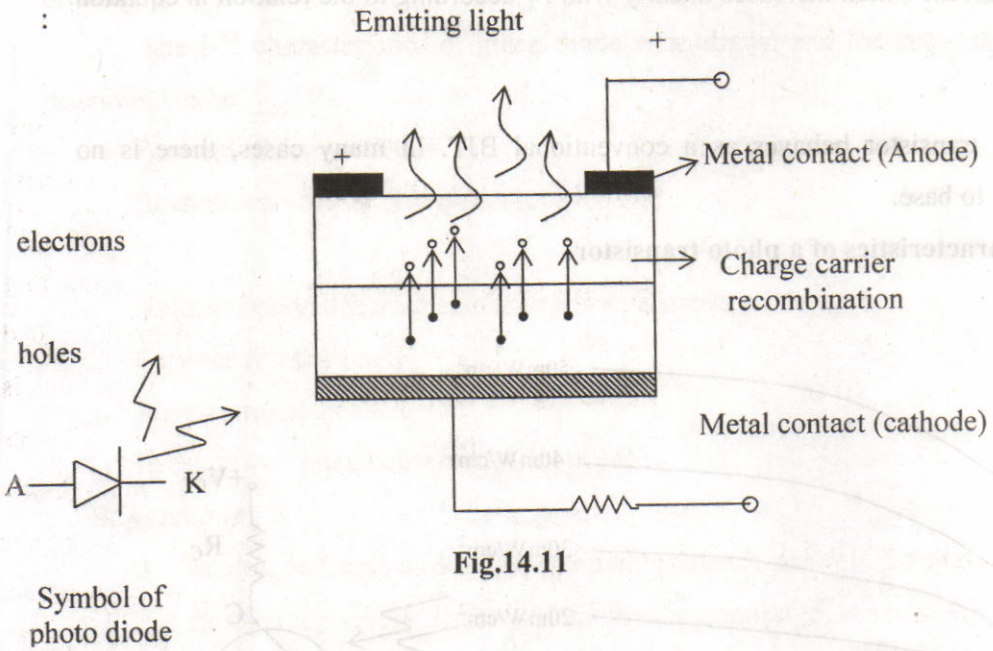


Fig.14.11

Symbol of
photo diode

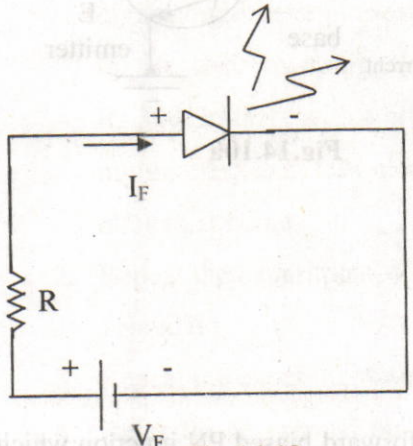


Fig.14.12

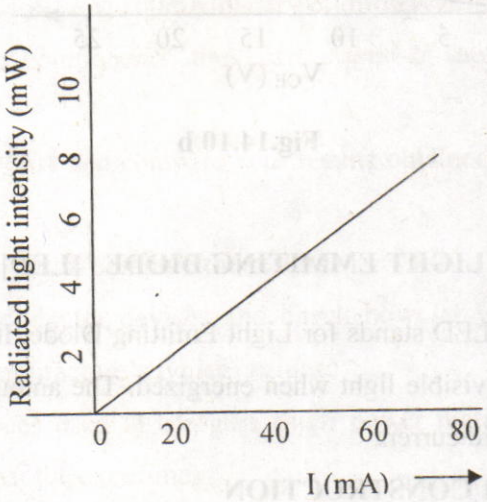


Fig.14.13 Light output vs forward current

Gallium Arsenide Phosphide (GaAsP) or Gallium Phosphide (Ga P) and these materials are semi transparent [Silicon and Germanium are not used because they are essentially heat-producing materials and are opaque to light]. The construction is shown in Fig.14.11

GaAs LEDs emit infrared radiation, GaAsP produces either red or yellow light and GaP emit red or green light.

14.8.2 THEORY AND WORKING

FORWORD BIASED OPERATION

As shown in Fig.14.12, when the device is forward biased, electrons cross the PN junction from the N- type material and combine with holes in the P-type material when recombination takes place, the recombining electron release energy in the form of heat and light. A larger exposed surface area on the layer of the semiconducting materials permits the light photons to be emitted as visible light. This process is called *Electro luminescence*. The emitted light is proportional to forward current and is shown in Fig.14.13. A typical LED has a voltage drop of 1.5 to 2.55V for currents between 10 and 50mA. For safe operation, a series resistor is often used in the circuit. A resistance of 330Ω is usually used in series with LED as in Fig.14.12. LEDs have low reverse voltage ratings. A typical value is 3.5V. Excessive high voltage or current burns out the LED. Under certain conditions, the emitted light is coherent (essentially monochromatic). Such a diode is called an Injection Junction Laser.

14.8.3 APPLICATIONS

LEDs are commonly used

1. For indicator lamps and for read out displays on a wide variety of instruments.
2. In seven segment displays in calculators and digital clocks.
3. In optical switching and also in optical coupling applications.
4. In solid state video displays.
5. In opto-isolation circuits

14.9 SOLAR CELL

Solar cell or Solar battery is basically a P-N Junction diode which converts solar energy directly into electrical energy. It is a photo diode operated at zero bias voltage.

A solar cell consists of a P-N junction diode made of Si or Ge (other materials are Ga As, In, Cd). The bottom surface that is always away from the light (dark side) is covered with a continuous conductive contact to which a wire lead is attached. The upper surface has a maximum area exposed to sunlight with a small contact, often along one edge as shown in Fig.14.14.

14.9.1 CONSTRUCTION

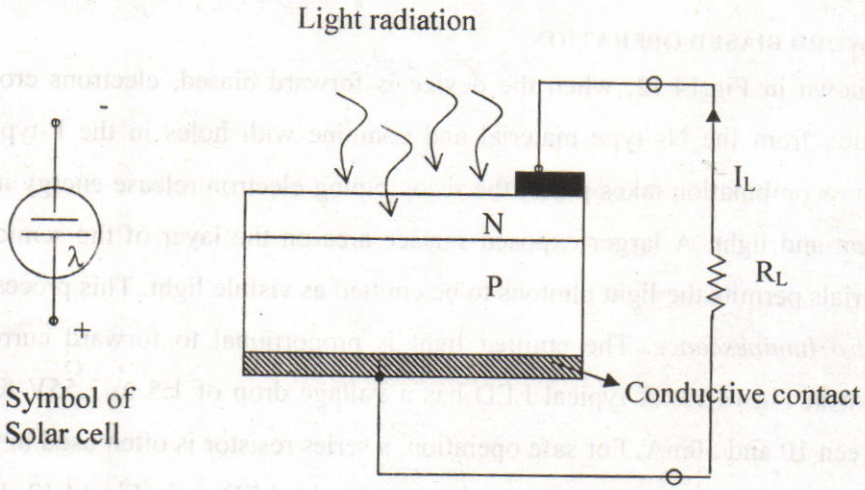


Fig.14.14

WORKING

When the solar cell is illuminated, electrons within the semi conducting material absorb energy from sunlight photons that penetrate the exposed surface. Many of these electrons acquire sufficient energy to break away from the parent atoms, those creating electron – hole pairs. An electric field is established in the vicinity of PN- junction by the positive and negative ions created. The number of electrons–hole pairs far exceeds the number needed for thermal equilibrium. Therefore, many of the electrons are pulled across the junction by the force of the electric field. Those carriers that cross the PN-junction, contribute to the current in the cell and through the external load. Solar cell generates 0.4V or less with currents ranging from μA to mA, depending upon external load. A solar cell behaves like a zero voltage biased photo diode.

14.9.3 I-V CHARACTERISTICS

Fig.14.15 shows the I-V characteristics of solar cell. The power delivered to a load is indicated by the product VI. This power is the maximum for a specific load resistance. We can call the values of voltage and current which give the maximum power as

Short circuit current (I_{SC})

It is the current which is obtained for zero applied voltage or when $R_L = 0\,\Omega$.

Open-circuit voltage (V_{oc})

It is the voltage which is obtained at the output terminals without load or open circuit condition.

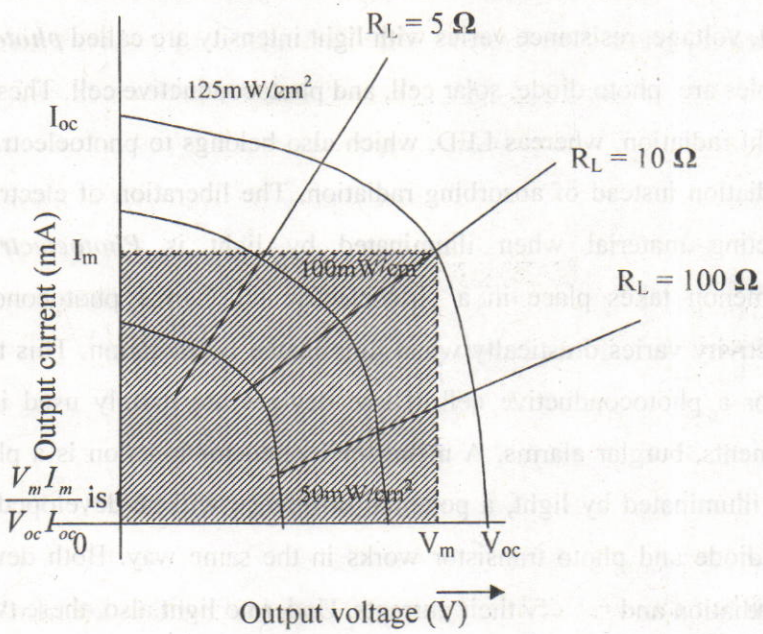


Fig.14.15

It is called a ***cell*** because it gives a small d.c voltage at its output. Such cells are connected in series and in parallel to produce required electric power. An array containing a number of series connected or series – parallel connected solar cells mounted on a flat plate is called a solar panel. The typical open-circuit voltage of a Silicon cell is 0.5V. The power conversion efficiency of is about 15%. Attempts are being made worldwide to promote solar energy a alternative electrical power source using Solar panels to meet the energy shortage and in places creation or transporting conventional source of electricity are not economically viable.

14.9.4 APPLICATIONS

1 In satellite, in photo voltaic panels.

2 In calculators to provide DC voltage

3 In remote areas, for power generation.

4 In photovoltaic light sensors.

5 To charge auxiliary storage batteries.

14.10 SUMMARY

Photo means light, electric means current. The devices whose variables like current, voltage, resistance varies with light intensity are called ***photoelectric devices***. Examples are: photo diode, solar cell, and photoconductive cell. These devices absorb the light radiation, whereas LED, which also belongs to photoelectric devices, emits the radiation instead of absorbing radiation. The liberation of electrons from a semi conducting material when illuminated by light is ***Photoelectric Effect***. This phenomenon takes place in a photoelectric tube. In a photoconductive cell, the conductivity varies drastically when illuminated by radiation. This takes place in an LDR or a photoconductive cell. These devices are mainly used in light sensitive instruments, burglar alarms. A metal-semiconductor junction is a photo voltaic cell. When illuminated by light, a potential difference will be developed across its ends. Photo diode and photo transistor works in the same way. Both devices receive the light radiation and m··fy their currents. Under no light also, these two devices allow certain current to fl· ...rough them. This is known as ***Dark Current***. Solar cell is a PN-junction diode but it develops a potential difference across its terminals when illuminated by light radiation. Si and Ge are the mostly used semiconducting materials for manufacturing solar cells. Solar cells are widely used in satellites and in calculators for providing DC potentials to operate electronic circuits. Solar cells are also used to provide power in remote areas.

14.11 KEY TERMINOLOGY

Photoelectric effect, photoconductive effect, photo voltaic effect, light emitting diode, spectral response, work function.

14.12 Self assessment questions

(I) Long answer questions

1. Explain the Einstein theory of photoelectric effect. Give the experimental arrangement.
2. Explain the photoconductive effect. Describe the construction and working of photoconductive cell. Mention its applications.
3. What is photo voltaic effect? Discuss the construction and working of photovoltaic cell. Mention its applications.

4. What is a photo diode? Discuss its construction, working and characteristics of photo diode. Differentiate between photo diode and ordinary diode.
5. What is a photo transistor? Discuss its construction, working and characteristics.
6. What is an LED? Discuss its construction, working and characteristics. Mention its applications.

(II) Short answer questions

1. Discuss about the photo conductive effect.
2. What is a solar cell? Discuss its working.
3. What is spectral response? Discuss the working of photoconductive cell.
4. Draw the characteristics of photodiode and explain.
5. Explain photoelectric effect.

14.13 REFERENCES

1. Electronic Devices and Circuits – Millman and Halkias (TMH)
2. Electronic Devices – Floyd (PHI)
3. Electronic Devices and Circuits – Boylestad and Nashelsky (PHI)

PRACTICAL LAB MANUAL (Paper-2)

INDEX

B.Sc. II YEAR ELECTRONICS PRACTICALS

1. Volt-Ampere characteristics of a junction diode-To find the cutin voltage.
2. Zener diode characteristics- To study the action of Zener diode as a voltage regulator.
3. Clipping and clamping circuits- Observation of output waveform for sinusoidal input.
4. BJT input and output characteristics – Determination of h-parameters.
5. FET-Transfer and Drain characteristics.
6. UJT- a) Volt-Ampere characteristics- Determination of its parameters.
   b) As an oscillator for generating two frequencies.
7. a) Single stage RC-couple amplifier-frequency response. b) Effect of negative feedback in the above circuit and comparison of two circuits w.r.t. gain and bandwidth.
8. LDR characteristics.
9. Phase shift oscillator- Design and construction-determination of frequency.
10. Design and Construction of Colpitts/Hartley oscillator.
11. Astable multivibrator- Design and determination of frequency.
12. Determination of energy gap of a junction diode using reverse saturation current.
13. Voltage doubler using diodes.
14. Simulation experiments.

(Any ten experiments)

GUIDE LINES FOR PERFORMING ELECTRONICS PRACTICALS

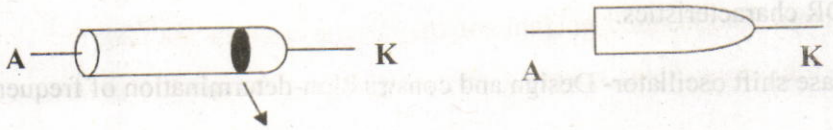
In order to conduct experiments with/using electronic devices like diode, transistor, UJT, SCR, JFET, LED, etc., first of all their leads are to be identified and their good condition is to be checked.

Diodes can be checked by using a digital or analog multimeter, component tester, curve tracer. Similarly, a transistor can be checked for its good condition by using an Ohmmeter (Digital multimeter), curve tracer, component tester, or by using a digital multimeter having h_{fe} (or β) measurement facility. The type of the transistor can also be known.

PN-Junction diode:

Diode symbol and Cases: Generally Silicon diode appears opaque, whereas Germanium diode appears transparent.

(a) Symbol



Silver band

(b) Cases

Fig.1.1

Generally a silver band is marked close to one end on the body of the diode which indicates that the electrode close to it is cathode and the other electrode is anode. Diodes are generally specified with some values in data hand books or data sheets. They are:

1. The forward voltage V_f at a specified current and temperature.
2. Maximum forward bias current I_f, at a specified temperature.
3. Reverse saturation current I_r, at a specified voltage and temperature.

4. The peak inverse voltage PIV, at a specified temperature.
5. The maximum power dissipation level at a particular temperature.
6. Capacitance value.
7. Reverse recovery time.
8. Operating temperature range.
9. Application of the diode.

1.1 DIODE TESTING

1.1.1 Ohmmeter tests

One of the simplest and quickest tests can be made using an ohmmeter to measure the forward and reverse resistance of a diode. Fig.1.2 shows the way. Take a digital multimeter and convert it into an ohmmeter. Connect the +ve terminal (Ohm/V) to one of the diode leads and the –ve terminal (Com) to the other lead of the diode. If the ohmmeter shows low resistance, then the diode is said to be in Forward bias. In this case, the diode lead that is connected to +ve terminal of the multimeter is to be treated as Anode and the other lead is Cathode. On the other hand, if the ohmmeter shows high resistance, then the diode is said to be in Reverse bias. In this case, the diode lead that is connected to +ve terminal of the multimeter is to be treated as Cathode and the other lead is Anode. In both forward and reverse directions, if the diode shows a low resistance, the diode is said to be Short-circuited. In both forward and reverse directions, if the diode shows a high resistance, the diode is said to be Open-circuited.

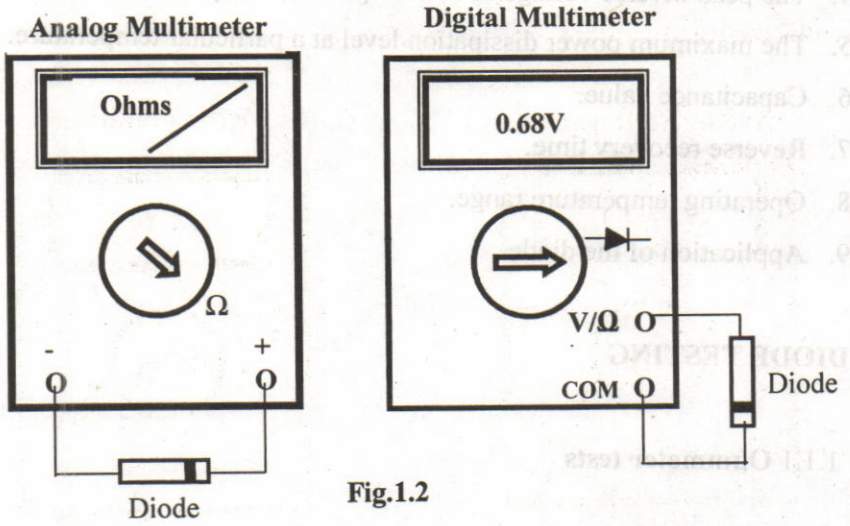


Fig.1.2

USE OF A DIGITAL MULTIMETER

Many handheld digital multilmeters have a diode testing facility which displays the forward voltage drop across the diode (Ex. 0.68V as shown in the Fig.1.2)., when the terminals are connected positive to anode and negative to cathode. When reverse connected, a functioning diode produces an OL display. If OL display occurs with both forward and reverse connections, the diode is open-circuited. When the display is 000, the device is short-circuited.

1.2 TRANSISTOR TESTING

Transistor is a three terminal semiconductor device. It possesses three leads, namely emitter, base and collector. The manufacturer may prepare a transistor either with plastic case or with a metal case. Plastic case transistors are cheaper as compared to metal case. The leads of a transistor can be identified by using its bottom view. The data sheet or data manual provide us the way in which the leads are to be identified using the bottom view. The correct functioning of a transistor can be known either by using a digital multimeter, possessing β (h_{fe} or current gain) measurement facility) or by Ohmmeter tests.

Ohmmeter tests

An Ohmmeter may be used for checking the transistor's emitter-base and collector-base junctions. The measured resistance between the collector and emitter terminals of a good transistor should be high regardless of the Ohmmeter terminal polarity.

With an analog Ohmmeter, a good forward-biased PN-junction (may be emitter-base or collector-base) indicates half scale as shown in Fig.1.3.

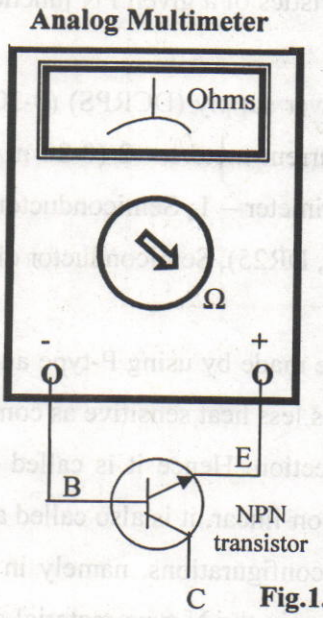


Fig.1.3

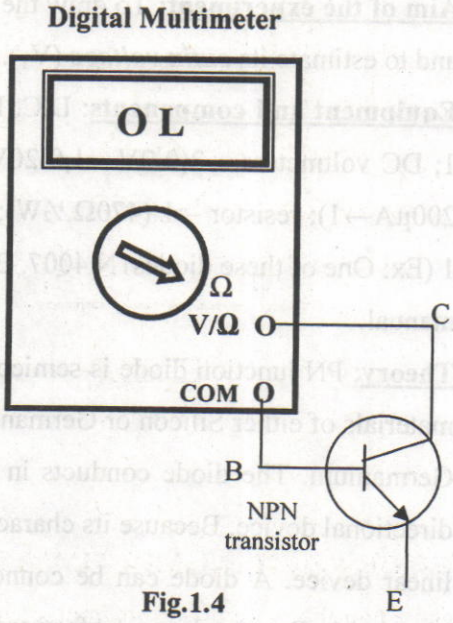


Fig.1.4

A digital multimeter may show a resistance of few Kilo Ohms when measuring a good forward-biased junction (Emitter-base or Collector-base) and an open-circuit indication (OL) for a reverse-biased junction as shown in Fig.1.4.

BOTTOM VIEW OF A SILICON TRANSISTOR

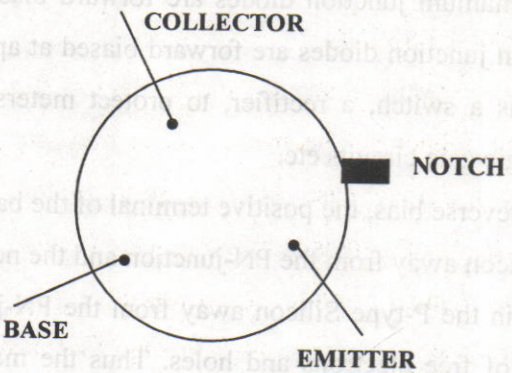


Fig.1.5

EXPERIMENT 1

DIODE CHARACTERISTICS

Aim of the experiment: To draw the I-V characteristics of a given PN junction diode and to estimate its ***cutin voltage*** (V_T).

Equipment and components: D.C. Regulated power supply (DCRPS) (0-30V, 1A)-1; DC voltmeters – 2(0-2V→1,0-20V→1); DC current meters – 2 (0-20 mA→1, 0-200μA→1); resistor – 1 (470Ω,½W); Digital Multimeter – 1; Semiconductor diode – 1 (Ex: One of these diodes1N 4007, BY127, OA79, DR25), Semiconductor diode data manual.

Theory: PN junction diode is semiconductor diode made by using P-type and N-type materials of either Silicon or Germanium. Silicon is less heat sensitive as compared to Germanium. The diode conducts in only one direction. Hence it is called as a Uni directional device. Because its characteristics are non-linear, it is also called as a Non-linear device. A diode can be connected in two configurations, namely in Forward bias and in Reverse bias. In forward bias, electrons in the N-type material and holes in the P-type material are pushed towards the junction. When the applied voltage is progressively increased from zero, the barrier voltage gets smaller until it effectively disappears. Now the charge carriers easily flow across the junction. As more number of charge carriers cross the junction, the forward current is of the order of milli Amperes. Germanium junction diodes are forward biased at approximately at 0.3V whereas Silicon junction diodes are forward biased at approximately at 0.7V. Diodes can be used as a switch, a rectifier, to protect meters and devices, in DC power supplies, in logic gate circuits etc.

In the reverse bias, the positive terminal of the battery attracts free electrons in the N-type Silicon away from the PN-junction and the negative terminal of the battery attracts holes in the P-type Silicon away from the PN-junction. Hence there are no combinations of free electrons and holes. Thus the majority current carriers in the diode do not support current flow. In the reverse bias connection, there is a minute current in the diode. This current is due to the minority carriers (holes in the N-type and free electrons in the P-type materials). Only a few micro Amperes of current will flow as a result of the minority carriers. The reverse bias connection results in a high reverse resistance in the diode.

Circuit diagrams

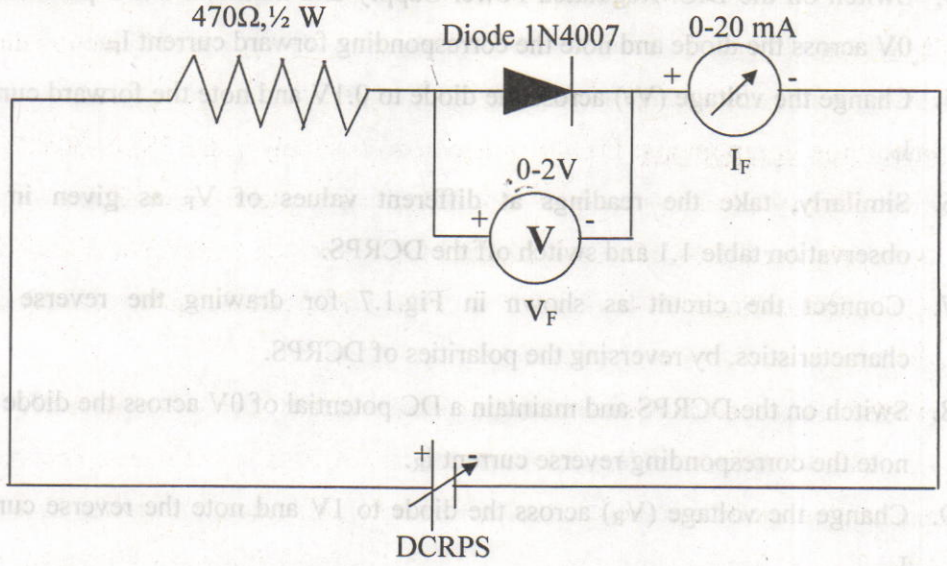


Fig.1.6

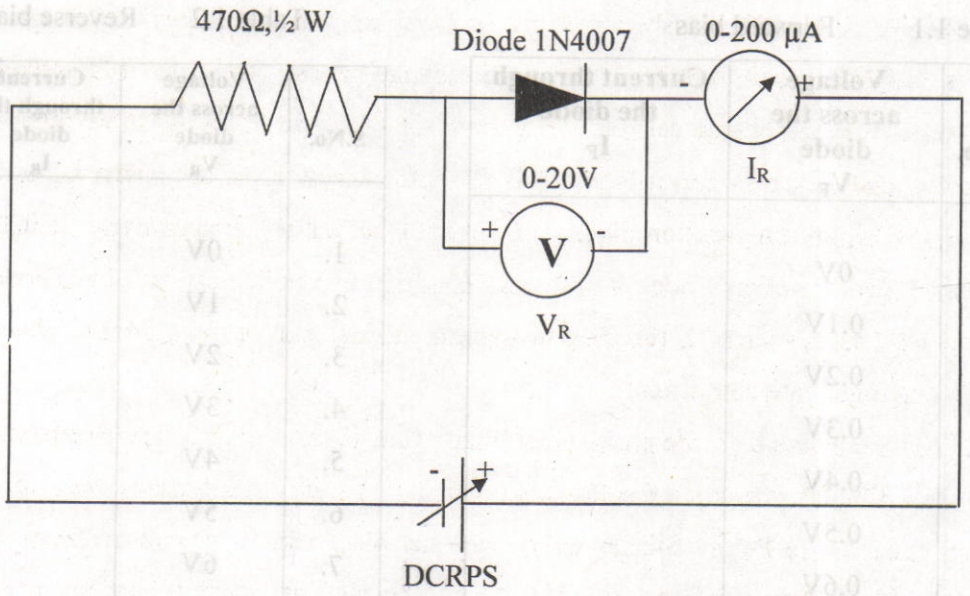


Fig.1.7

Steps to follow

1. Identify the components (resistor and diode) given.
2. Identify the leads (anode and cathode) of given diode.
3. Connect the circuit as shown in Fig.1.6 for drawing the forward bias characteristic.

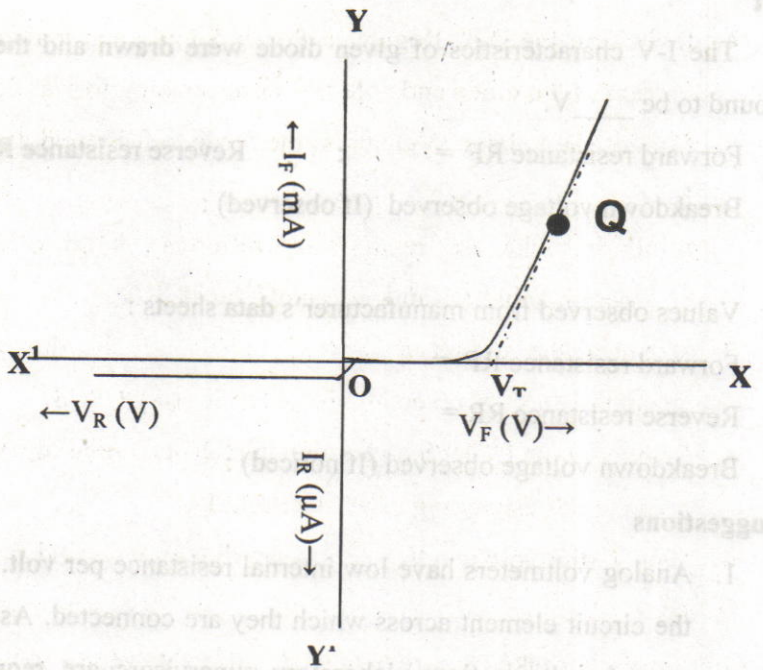
4. Switch on the D.C. Regulated Power Supply and maintain a DC potential of 0V across the diode and note the corresponding forward current I_F.
5. Change the voltage (V_F) across the diode to 0.1V and note the forward current I_F.
6. Similarly, take the readings at different values of V_F as given in the observation table 1.1 and switch off the DCRPS.
7. Connect the circuit as shown in Fig.1.7 for drawing the reverse bias characteristics, by reversing the polarities of DCRPS.
8. Switch on the DCRPS and maintain a DC potential of 0V across the diode and note the corresponding reverse current I_R.
9. Change the voltage (V_R) across the diode to 1V and note the reverse current I_R.
10. Similarly, take the readings at different values of V_R as given in the observation table 1.2 and switch off the DCRPS.

Table 1.1 Forward bias

S.No.	Voltage across the diode V_F	Current through the diode I_F
1.	0V	
2.	0.1V	
3.	0.2V	
4.	0.3V	
5.	0.4V	
6.	0.5V	
7.	0.6V	
8.	0.65V	
9.		

Table 1.2 Reverse bias

S.No.	Voltage across the diode V_R	Current through the diode I_R
1.	0V	
2.	1V	
3.	2V	
4.	3V	
5.	4V	
6.	5V	
7.	6V	
8.	7V	
9.	8V	
10.	9V	
11.	10V	



Graph

1. Draw a graph by taking the variable *Forward Voltage (V_F)* along +ve X-axis and the *Forward Current (I_F)* along +ve Y-axis; similarly *Reverse Voltage (V_R)* along -ve X-axis and the *Reverse Current (I_R)* along +ve Y-axis.
2. Mark the observations obtained and draw the graph. If the observations are all correct you will get a smooth curve..Otherwise draw a smooth curve such that maximum number of points fall on it or most of the points spread on either side of the curve. Select a point (operating point or Q point) in the middle of the linear portion of the forward characteristic.
3. Draw a tangent at this point and extend it to intercept the X-axis as shown in Fig.1.8. The voltage at this point of intersection will give us the *Cutin voltage* (V_T).
4. Determine the slope of this tangent line. It gives the forward resistance of given diode.
5. Draw a similar tangent to the reverse bias characteristic at the centre of the characteristic and determine its slope. It gives the reverse resistance of the diode

ð Compare the R_F and R_R values.

Result

The I-V characteristics of given diode were drawn and the cut - in voltage was found to be ____V.

Forward resistance RF = : Reverse resistance RR =

Breakdown voltage observed (If observed) :

Values observed from manufacturer's data sheets :

Forward resistance RF =

Reverse resistance RR =

Breakdown voltage observed (If noticed) :

Suggestions

1. Analog voltmeters have low internal resistance per volt. So they will load the circuit element across which they are connected. As this will result in error in observations, laboratory supervisors are requested to provide digital multimeters instead of analog meters. Students may be encouraged to use their own digital multimeter as they are available at less than Rs.300. In fact , with a bread board,12 V 100mA battery eliminator, digital multimeter, and few electronic components, they can assemble several circuits at home.
2. Repeat the experiment with 1N4001 and compare your results obtained on 1N4007.
3. Repeat the experiment with OA79 and compare the results.
4. Refer to the manual on semiconductor devices and check how far your results are in agreement with manufacture's typical values.
5. Enquire about the rectifier diodes used in chargers (high power rectifier diodes). Try to get one and repeat the experiment.
6. Enquire about diode used in high voltage applications and repeat the experiment. Compare the results of experiments conducted on signal diode, with a general purpose medium power rectifier diode, a high power rectifier diode and a high voltage application diode.

Precautions

1. Keep the coarse and fine knobs of voltage variation of DCRPS in minimum position before switching on and switching off the DCRPS.

2. Keep the current limit knob of the DCRPS in maximum position before the commencement of experiment.
3. Avoid loose connections if any.
4. Select appropriate ranges in the meters.
5. If you are provided with a D.C regulated power supply with no current and voltage meters, select meters of suitable range and connect them with proper polarity. Analog meters (with moving coil pointers) connected in wrong polarity get spoiled and / or damaged permanently. Remember to connect current meters in series by breaking at a point of interest and voltmeters across the power supply. Connecting the current meters in shunt will short circuit the supply. Connecting voltmeters in series will amount to placing a very high resistance in series and you will no get proper observation
6. DMMs work more reliably and are economical in long run. They have over range protection also. If analog meters given in practical check the analog voltmeter readings with digital multimeter for agreement.

Viva Questions

1. What is a PN-junction diode?
2. What is a *barrier potential*? What is its significance? Mention its values in case of Silicon and Germanium.
3. Give the applications of diode.
4. What is *cutin* voltage? Why it is named so?
5. What is *reverse saturation current*?
6. What are forward and reverse bias?
7. Why diode is a non-linear device?
8. How a diode is prepared?
9. Though barrier potential is present in a diode but we do not see any potential difference across an open circuited diode. Why?
10. What is the reverse breakdown potential of 1N4007 diode?
11. What is the reverse breakdown potential of OA79 diode?
12. What are the values forward resistance and reverse resistances of 1N4007 diode?
13. What precautions do you take if you perform the experiment with Germanium diode?

2. ZENER DIODE CHARACTERISTICS

AIM OF THE EXPERIMENT

To draw the I-V characteristics of a given Zener diode and to estimate its *breakdown voltage* ($V_{Z(BR)}$).

EQUIPMENT AND COMPONENTS

DCRPS (0-30V, 1A, voltage covered in several steps)-1; DC voltmeters – 2(0-2V→1, 0-20V→1); DC current meter – 1 (0-200 mA→1); Resistor – 1 (470Ω, ½W); Zener diode – 1 (BZ 147, FZ 6.3 or any other value). (Digital multimeters are recommended). Single strand wires of suitable gauge for use with given breadboard, patch cords, nose pliers, tweezers to remove plastic sleeve on the wires, Soldering iron (if group board is given), a nose plier and a wire cutter.

THEORY

The characteristics of a semiconductor diode depend on the material, construction, doping and diode dimensions. Zener diode is also a semiconductor device just like an ordinary junction diode. But it is a heavily doped diode and is mostly used in reverse bias configuration. When a junction diode is reverse biased, only a small reverse saturation current flows. When the reverse voltage is sufficiently increased, the junction breaks down and large reverse current flows. If the reverse current is limited by means of a suitable series resistor, the power dissipation in the junction can be kept to a level that will not destroy the device. In this case, the diode may be operated continuously in reverse breakdown region. When the reverse voltage is lowered below the reverse breakdown level, the reverse current returns to its normal level.

Diodes designed for operation in reverse breakdown are found to have a breakdown voltage that remains extremely stable over a wide range of current levels. This property gives breakdown diode many useful applications as a voltage reference source. There are two mechanisms that cause breakdown in a reverse biased PN-junction. With a very narrow depletion region, the electric field strength (Volts/width) produced by a reverse bias voltage can be very high. The high intensity electric field causes electrons breakaway from their atoms thus converting the depletion region from an insulating material into a conductor. This is ionization by electric field, also called Zener breakdown and usually occurs with reverse bias voltages less than 5V.

In cases where the depletion region is too wide for Zener breakdown to occur, the electrons in the reverse saturation current can be given sufficient energy to cause other electrons to break free when they strike atoms within depletion region This is termed *Ionization by Collision*. The electrons released in this way collide with other atoms to produce more free electrons in an avalanche effect. Avalanche effect is normally produced by reverse voltages above 5V.

CIRCUIT DIAGRAMS

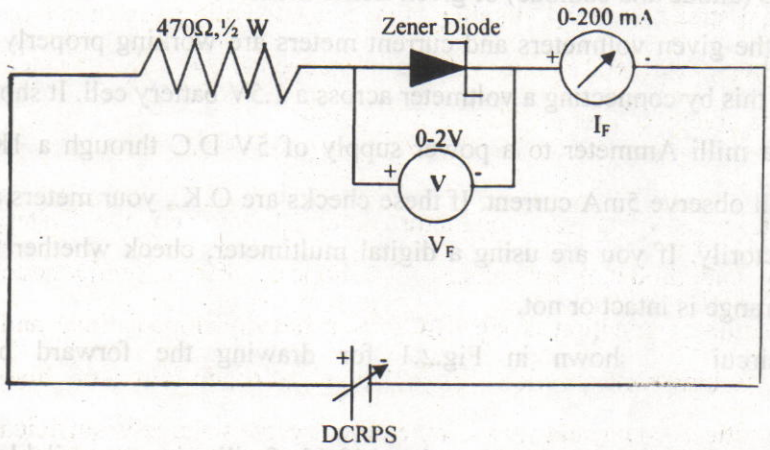


Fig.2.1

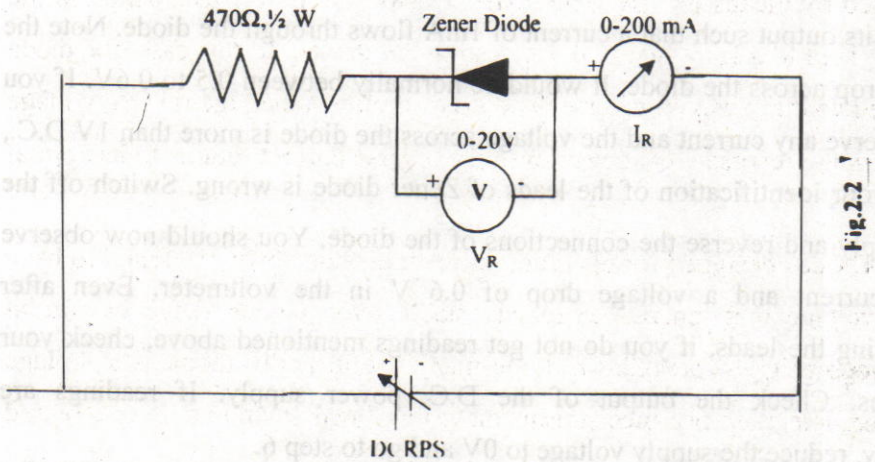


Fig.2.2

CALCULATION OF SAFE CURRENT OF ZENER DIODE

Manufacturers specify the maximum safe power for a given Zener diode of specific number. They also specify the breakdown voltage. We get the approximate maximum current by dividing the power specified by the breakdown voltage.

Ex: BZ 147 has the following ratings:

Breakdown voltage = 6.2V; Power dissipation = 750mW; I_z max = 100mA

Zener diodes can be used as a voltage regulator to provide a constant voltage output, as a reference voltage source, to protect meters, for calibration of meters and as a peak clipper.

a) Zener diode characteristics

STEPS TO FOLLOW

1. Identify the components (resistor and the Zener diode) given.
2. Identify the leads (anode and cathode) of given Zener diode.
3. Check whether the given voltmeters and current meters are working properly or not. You can do this by connecting a voltmeter across a 1.5V battery cell. It shows 1.5V. Connect a milli Ammeter to a power supply of 5V D.C through a 1KΩ resistor. You will observe 5mA current. If these checks are O.K., your meters are working satisfactorily. If you are using a digital multimeter, check whether the fuse for current range is intact or not.
4. Connect the circui shown in Fig.2.1 for drawing the forward bias characteristic.
5. Switch on the DCRPS, keep it in 0-2V setting (if this facility is not available in the power supply, then use a potentiometer arrangement to tap required voltage), and adjust its output such that a current of 1mA flows through the diode. Note the potential drop across the diode. It would be normally between 0.5 to 0.6V. If you do not observe any current and the voltage across the diode is more than 1V D.C., probably your identification of the leads of Zener diode is wrong. Switch off the power supply and reverse the connections of the diode. You should now observe 1mA of current and a voltage drop of 0.6 V in the voltmeter. Even after interchanging the leads, if you do not get readings mentioned above, check your connections. Check the output of the D.C. power supply. If readings are satisfactory, reduce the supply voltage to 0V and go to step 6.
6. Change the voltage (V_F) across the diode to 0.1V and note the forward current I_F.
7. Similarly, take the readings at different values of V_F as given in the observation table 2.1 and switch off the DCRPS.
8. Connect the circuit as shown in Fig.2.2 for drawing the reverse bias characteristic, by reversing the diode connections.
9. Switch on the DCRPS and keep it at 0V DC and go to step 10.

10. Change the voltage (V_R) across the diode to 1V and note the reverse current I_R.
11. Similarly, take the readings at different fixed values of V_R till the approximate value of breakdown voltage is reached.
12. Now change the voltage across the diode in very small steps until the current reaches 10mA maximum value, noting voltage and current for each setting. Record the observations in table 2.2.

* If the breakdown voltage of the given diode is 6.3V, then vary voltage in steps of 1V until we reach 6V and then small steps above this. If the breakdown voltage is other than 6.3V (say 9.1V), then vary the voltages across the diode instep of 1V up to 8.5V and then in small steps until the current reaches a maximum of 10mA.

Table 2.1 Forward bias

S.No.	Voltage across the diode V_F	Current through the diode I_F
1.	0V	
2.	0.1V	
3.	0.2V	
4.	0.3V	
5.	0.4V	
6.	0.5V	
7.	0.6V	
8.	0.65V	
9.		

Table 2.2 Reverse bias

S.No.	Voltage across the diode V_R	Current through the diode I_R
1.	0V	
2.	1V	
3.	2V	
4.	3V	
5.	4V	
6.	5V	
7.	6V	
8.	6.1V	
9.	6.2V	
10.	6.3V	
11.	6.4V *	

GRAPH

1. Draw a graph by taking the variable *Forward Voltage (V_F)* along +ve X-axis and the *Forward Current (I_F)* along +ve Y-axis; similarly *Reverse Voltage (V_R)* along -ve X-axis and the *Reverse Current (I_R)* along +ve Y-axis.
2. Mark the observations obtained and join them by a smooth curve.
3. Select a point on the linear portion of the reverse characteristic.

4. Draw a tangent at this point and extend it to intercept the –ve X-axis as shown in Fig.2.3. The voltage at this point of intersection will give us the *Zener breakdown voltage* ($V_{Z(Br)}$).

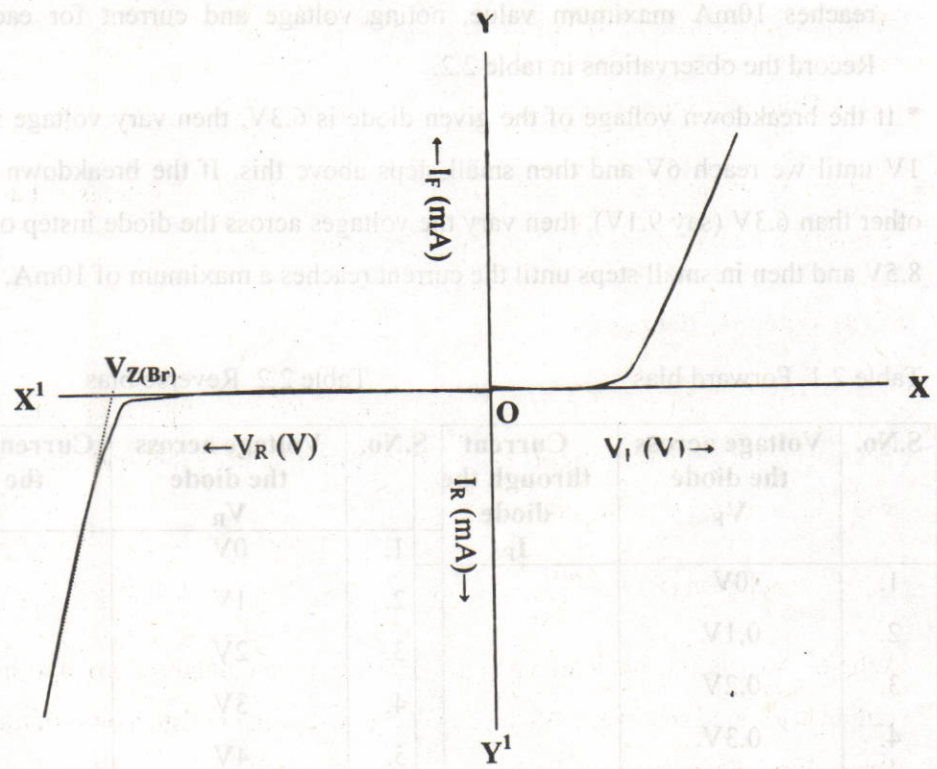


Fig.2.3

RESULT

The I-V characteristics of given Zener diode were drawn and the breakdown voltage was found to be ____V.

V_Z value specified on the diode or the value quoted for the number on the diode

---- Volts

Regulation characteristics of Zener diode

CIRCUIT

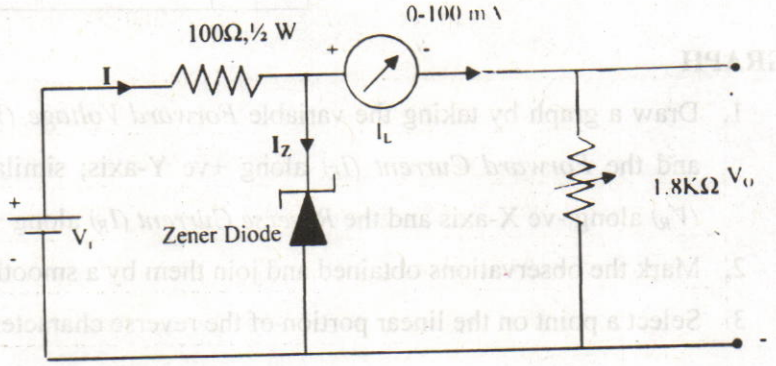


Fig.2.4

THEORY

Regulation : It is a measure of circuits ability to maintain a constant, output voltage even when either the input voltage or load current varies. A Zener diode when working in the breakdown region can serve as a voltage regulator.

When V_{IN} is constant, R_L is varied.

(a) When R_L increases

When R_L increases, load current I_L decreases. Hence I_Z increases but IR drop across the load remains constant. So V_O remains unchanged.

(b) When R_L decreases

When R_L is decreased, the load current I_L increases and hence I_Z decreases, there by keeping IR drop (voltage drop) across the load constant. In this way, V_O remains unchanged.

$$\% \text{ regulation (R)} = \frac{V_{NL} - V_L}{V_{NL}} \times 100$$

Where V_{NL} is the no load voltage (open circuit voltage or voltage across the output with load removed). V_L is the voltage with load resistance (variable).

Procedure (Steps to follow):

1. Connect the circuit as shown in Fig 2.4
2. Measure the output voltage with digital multimeter.
3. For V_i slightly greater than V_z vary the load resistance and note load currents I_L and V_O.
4. Tabulate the results in table 2.3.

Table.2.3

S.No.	I_L (mA)	V_O (Volts)	% regulation $= \frac{V_{NL} - V_L}{V_{NL}} \times 100$
1	0		
2	5		
3	10		
,			
.			
11	50		

Graph: Plot the variation of % regulation (R) with load current (I_L).

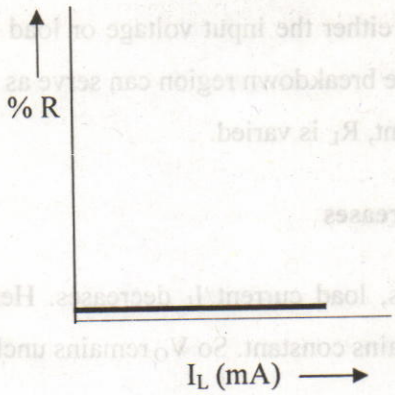


Fig.2.4

PRECAUTIONS

1. Keep the coarse and fine knobs of voltage variation of DCRPS in minimum position before switching on and switching off the DCRPS.
2. Keep the current limit knob of the DCRPS in maximum position before the commencement of experiment.
3. Avoid loose connections if any.
4. Select appropriate ranges in the meters.

SUGGESTIONS

1. If you are using a breadboard for making connections, use single strand wire of suitable gauge. Don't try to insert thick wires into the holes in breadboard.
2. Don't use multi strand wires while doing practical using breadboard. Use them to connect power supply to the circuit. Use patch cords with suitable probes to measure voltages currents and resistances.
3. Don't use a single color wire to make all the connections. Follow some color code. For example Positive D.C. supply carrying leads or anode or collector or drain leads red. Negative or ground wires black Cathode or emitter or source leads blue. Signal generator positive leads or Base or Gate leads green. Signal generator ground leads black. Intermediate connections yellow. This will enable one to identify the different areas of the circuit for fault finding.
4. If you are using a group board and soldering iron to make connections, follow the suggestion 4 while selecting wires for making connections. Try

to have your own personal soldering iron of good quality as it will help you in making good connections in less time.

5. Except for connecting to Signal generator to DMMs, and CRO wires exceeding1foot are rarely required. Make as short connections as possible. This will make your circuit look neat and it will avoid unwanted problems which you will understand latter. Examiner gets good impression on the students who could assemble neatly arranged circuits. Don't scatter soldering lead all around the work table. Make it a point to clear the work table before leaving the class.
6. Before inserting the leads of components like resistors, see that its leads are scraped to remove any oxidation coating, If there are any kinks on the leads, straighten them with a nose plier. Don't insert high Wattage resistors into the bread board.
7. Similarly straighten the leads of diodes, transistors and other components before inserting them into a bread board.
8. From the data manual, identify the Zener diodes of different make with same V_Z.
9. From the data manual, identify Zener diodes with larger V_Z values.
10. From the data manual, identify Zener diodes that give larger I_Z.

VIVA QUESTIONS

1. What is a Zener diode?
2. What do you mean by doping?
3. What are the differences between an ordinary diode and a Zener diode?
4. What are the uses of a Zener diode?
5. What is an avalanche mechanism?
6. What is Zener breakdown mechanism?
7. How a Zener diode acts as a voltage regulator?
8. Under what conditions, a Zener diode can act as a voltage regulator? An unregulated voltage of 10 V is given to a Zener of V_Z = 5V through a limiting resistance R. If the load current is 50mA and Zener current is 5 mA, what is the suitable value and wattage for the series resistor?

3. CLIPPING AND CLAMPING CIRCUITS

AIM OF THE EXPERIMENT: To study the operation of some clipping and clamping circuits and to draw their input and output waveforms.

EQUIPMENT AND COMPONENTS: CRO-1; Function Generator-1; Bread board-1; Diode (1N 4007)-1; Capacitor (0.1μF)-1; Resistor (10KΩ,1/2W)-1; DMM-1;

CIRCUIT DIAGRAMS

1) Positive Clipper

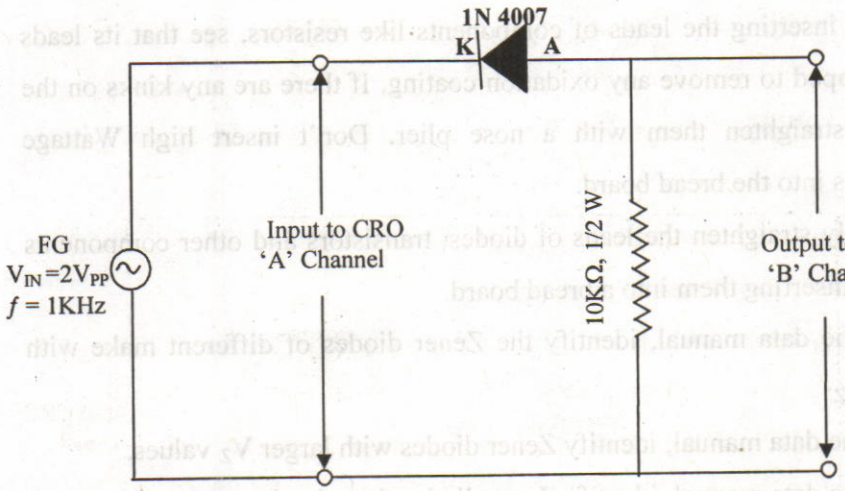


Fig.3.1

2) Negative Clipper

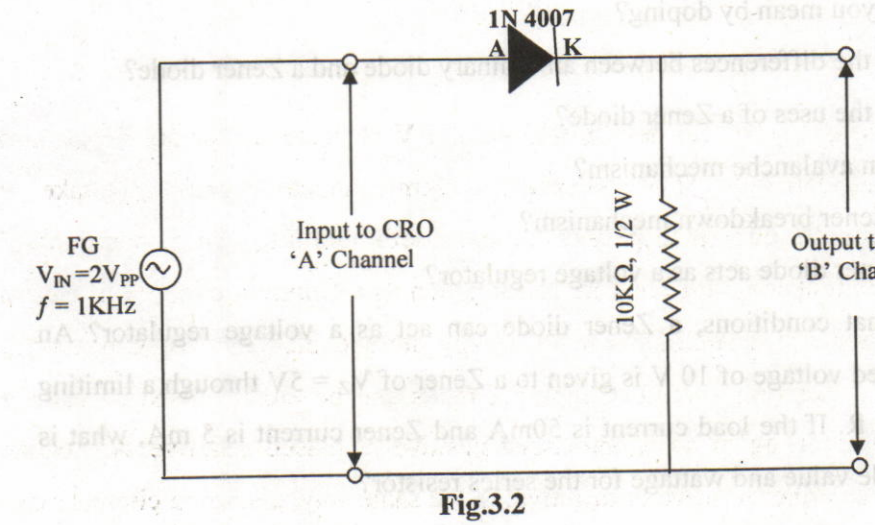


Fig.3.2

3) Positive Clamper

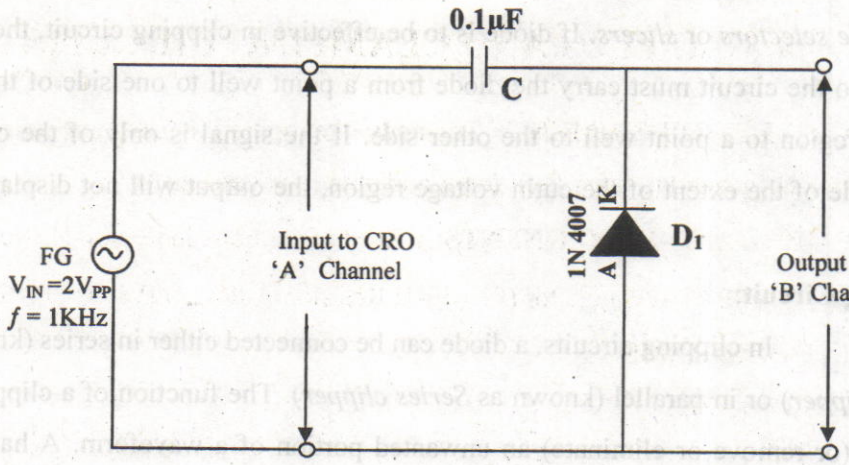


Fig.3.3

4) Negative Clamper

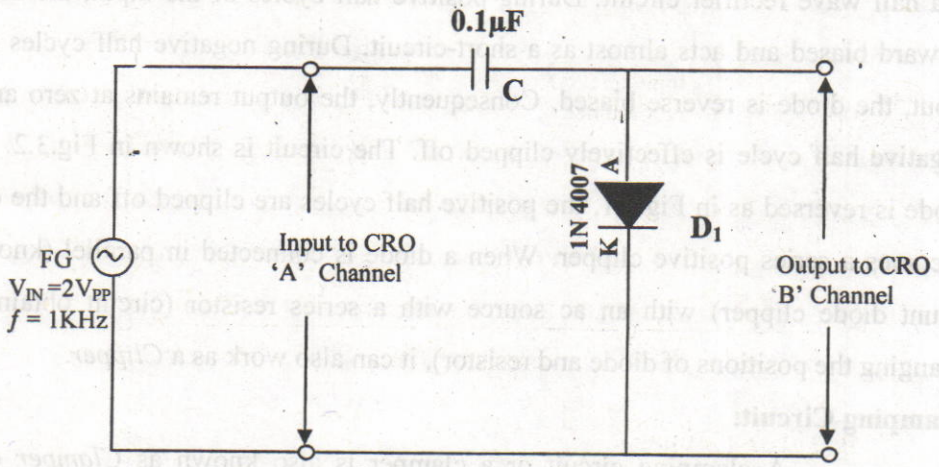


Fig.3.4

THEORY

Diode is a nonlinear device because its I-V characteristic is not linear; also it does not obey Ohm's law. The nonlinearity of semiconductor diode can be taken into advantage in pulse circuits to perform several useful and interesting operations. The diodes in combination with resistors can function as a Clipping circuit. On the other hand, the diode in combination with energy storage element like capacitor can function as a clamping circuit. Clipping circuits can be either biased or unbiased. Biased clipper can again be either biased positive or biased negative. An unbiased clipper may be either positive or negative. In the same way, clamping circuits may be either positive or negative. Clipping circuits are used to select for transmission, that part of an arbitrary waveform, which lies above or below some particular reference

voltage level. Clipping circuits are also referred to as *voltage (current) limiters, amplitude selectors* or *slicers*. If diode is to be effective in clipping circuit, the signal applied to the circuit must carry the diode from a point well to one side of the cutin voltage region to a point well to the other side. If the signal is only of the order of magnitude of the extent of the cutin voltage region, the output will not display sharp limiting.

Clipping Circuit:

In clipping circuits, a diode can be connected either in series (known as *Shunt clipper*) or in parallel (known as *Series clipper*). The function of a clipper is to clip off (or remove or eliminate) an unwanted portion of a waveform. A half wave rectifier (i.e. a simple diode) can be described as a clipper of an alternating waveform (sine, square, triangle) and clips off the other half cycle. In fact, a diode series clipper is a half wave rectifier circuit. During positive half cycles of the input, the diode is forward biased and acts almost as a short-circuit. During negative half cycles of the input, the diode is reverse biased. Consequently, the output remains at zero and the negative half cycle is effectively clipped off. The circuit is shown in Fig.3.2. If the diode is reversed as in Fig.3.1, the positive half cycles are clipped off and the circuit becomes a series positive clipper. When a diode is connected in parallel (known as Shunt diode clipper) with an ac source with a series resistor (circuit obtained by changing the positions of diode and resistor), it can also work as a *Clipper*.

Clamping Circuit:

A clamping circuit or a clamper is also known as *Clamper* or *DC restorer*, changes the DC voltage level of a waveform but does not affect its shape. In Fig.3.4, when the AC input is positive, diode D_1 is forward biased and the output voltage equals the forward voltage drop V_F. During the positive half cycle of the input, the voltage on the right side of the capacitor is $+V_F$, while that on the left side is +E. Thus C_1 is charged with the polarity shown to a voltage $V_{C1} = E - V_F$. When the input goes negative, the diode is reverse biased, and has no further effect on the capacitor voltage. While the input is negative, the output voltage is the sum of the input and capacitor voltages. Since the polarity of the capacitor voltage is the same as the input, the output is

$$V_0 = -[E + V_{C1}] = -[E + E - V_F] = -[2E - V_F]$$

The peak-to-peak output voltage ($V_{O(PP)}$) is the difference between the positive output peak (V_F) and negative output peak (i.e. $-(2E-V_F)$) . It is seen that peak-to-peak

amplitude of the output waveform of clamping circuit is exactly same as the peak-to-peak input.

INPUT AND OUTPUT WAVEFORMS

(i) Positive Clipper

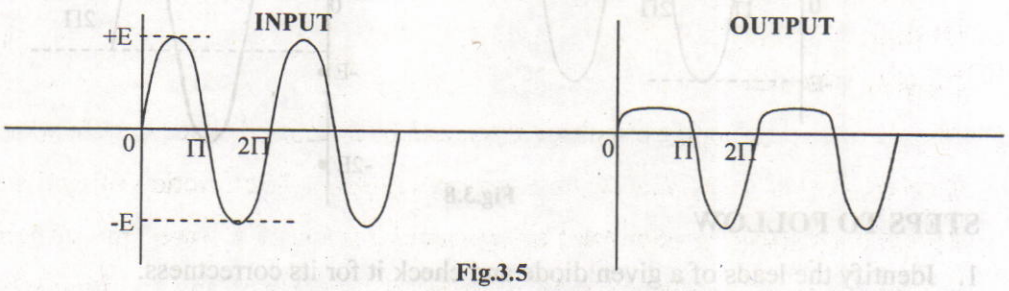


Fig.3.5

(ii) Negative Clipper

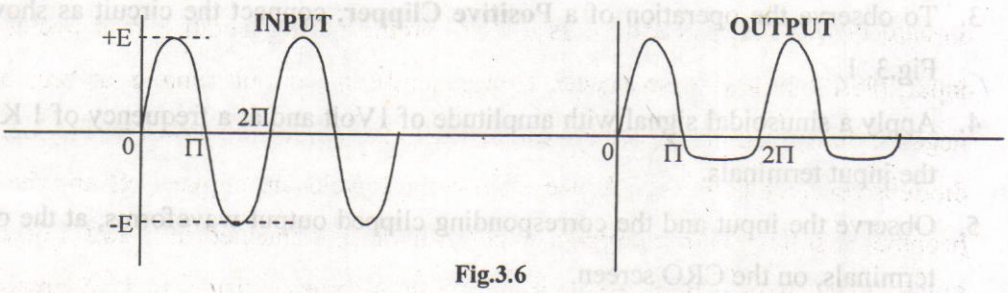


Fig.3.6

(iii) Positive Clamper

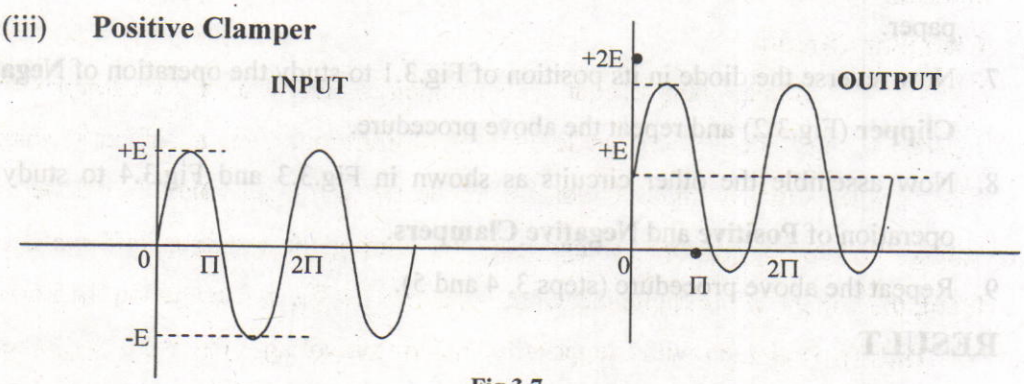


Fig.3.7

(iv) Negative Clamper

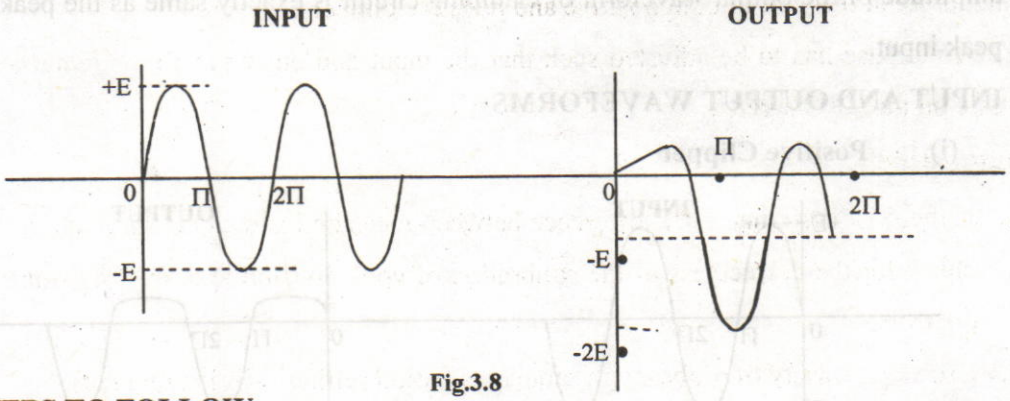


Fig.3.8

STEPS TO FOLLOW

1. Identify the leads of a given diode and check it for its correctness.
2. Check the working condition of diode and meters as is suggested in practical on Zener diode characteristics.
3. To observe the operation of a **Positive Clipper**, connect the circuit as shown in Fig.3. 1.
4. Apply a sinusoidal signal with amplitude of 1Volt and at a frequency of 1 KHz at the input terminals.
5. Observe the input and the corresponding clipped output waveforms, at the output terminals, on the CRO screen.
6. Measure the amplitudes and draw the waveforms on a graph paper or tracing paper.
7. Now reverse the diode in its position of Fig.3.1 to study the operation of **Negative Clipper** (Fig.3.2) and repeat the above procedure.
8. Now assemble the other circuits as shown in Fig.3.3 and Fig.3.4 to study the operation of **Positive** and **Negative Clampers**.
9. Repeat the above procedure (steps 3, 4 and 5).

RESULT

The operation of simple clipping and clamping circuits was studied and the waveforms were drawn on a tracing paper.

PRECAUTIONS

1. The AC/DC coupling slide switch of CRO B-channel is to be positioned at DC for observing the output wave form. While for A-channel, it is to be at AC for observing the input waveform.

2. Suitable adjustments are to be made for getting the same amplitude half cycles in the output in the case of both positive and negative clippers.
3. The time base has to be adjusted such that the input and out wave forms remain static on the CRO screen.

Suggestions

1. If there is more than 10% difference between measured and calculated values, check for the correctness of the calibration of volts/division and time/division controls.
2. Use same variety of probes with same attenuation setting (If it is provided).
3. Trigger control and/or sync control may have to be adjusted for old CROs to make the picture static.
4. Learn about the use of various controls and their effect on the signal. You should not try all the controls blindly. By this, you will be spoiling other proper settings. Also, the life of delicate controls gets reduced.
5. **To check the working status of CRO**, give a 2V peak-to-peak 1 KHz sine wave from a good function generator to the A and B inputs of a CRO. Put the same Volts/div. setting on the two channels of the CRO and adjust the required controls to see one cycle of sine wave on both the channels. Compare the two waveforms. They must look identical. Also, see whether you measure 2V peak-to-peak amplitude and 1KHz frequency. If you do not get them, report to the lab assistant for rectification or replacement with another CRO. If the CRO is alright for Sine waveform, change the function generator setting to square wave. See whether there is undue rise time and fall time. (Square wave looks like a trapezium)and any sag on the top of square wave. Sometimes you may see overshoot and undershoot on the waveform. These indicate poor response of the CRO. Try the procedure with another function generator and another CRO and if the response is good, something is wrong either with your CRO or function generator. Report the matter to the lab assistant and ask for good setup. All the above checking can be completed in 5 minutes. If you ignore them you may end up with incorrect observations.
6. Connect electrolytic capacitors after observing the polarity. Capacitors are labeled with working voltage. The peak-to-peak voltage across the capacitor should not exceed this value.

4. TRANSISTOR CHARACTERISTICS

AIM OF THE EXPERIMENT

To draw the input and output characteristics of a transistor connected in CE configuration and to determine its h-parameters.

EQUIPMENT AND COMPONENTS

D.C.R.P.S (0-30V; 1A)-2 {or a Dual DC power supply with two channels}; DC current meters (0-200μA→1, 0-20mA→1)-2; DMM-1; DC voltmeters (0-2V→1, 0-20V→1)-2; Transistor (Any transistor will do Ex: BC107, BC109, BC147, BC547, BF194, AC126 etc.,)-1; Resistor (33KΩ, 1/2W-1); Breadboard -1.

THEORY

A transistor consists of a Silicon (or Germanium) crystal in which a layer of N-type Silicon is sandwiched between two layers of P-type Silicon. A transistor may consist of a layer of P-type between two layers of N-type material. In the former case, the transistor is referred to as PNP transistor and in the later case, as an NPN transistor. This semiconductor assembly is extremely small and is sealed against moisture inside a metal or plastic case. The transistor is a three-layer (electrode) semiconductor device. The three electrodes are the emitter, the base and the collector. The emitter injects the charge carriers into the base. The base controls the charge carriers. There are two types of transistors: PNP and NPN. In NPN transistor, the emitter and collector are N-type and the base is P-type; while in PNP transistor, the emitter and collector are P-type and the base is N-type. In both types, to make the transistor work as an amplifier, emitter-base junction is forward biased and the collector-base junction is reverse biased.

When the transistor is used as an amplifier, the input is signal is given between a pair of terminals and the output is taken from another pair of terminals. Since the transistor has only three terminals, we have to make one of the terminals common to the input and output. The BJT can be used with any one of its three terminals as the common lead. Hence we have Common Emitter (CE), Common Base (CB) and Common Collector (CC) configurations. When the emitter junction is forward biased, emitter current I_E flows towards the junction. Due to recombination of charge carriers in base region, part of I_E will appear as base current I_B and the remaining of I_E reaches the collector and constitute collector current I_C. Hence we can write $I_E = I_B + I_C$.

Two families (sets) of characteristic curves specify the transistor parameters in any of the configurations. One set, the input characteristics, concerns the V-I relationship at input terminals for different values of the voltage or current at the third terminal. The second set, the output characteristics, gives the V-I relationship at output terminals for different values of input current. The behaviour of a transistor in circuit can be graphically analyzed with the help of these two families of curves. From the characteristic curves, we can determine the h-parameters of the given transistor. For example for transistor used in CE configuration , from input characteristics h_{ie} and h_{re} parameters and from the output characteristics h_{oe} and h_{fe} parameters can be determined. The h-parameters are defined as follows.

$$h_{ie} = \left.\frac{\Delta v_{be}}{\Delta i_b}\right|_{V_{CE=Constant}} \quad \text{----- (1)} \qquad h_{re} = \left.\frac{\Delta v_{be}}{\Delta v_{ce}}\right|_{I_{B=Constant}} \quad \text{----- (2)}$$

$$h_{fe} = \left.\frac{\Delta i_c}{\Delta i_b}\right|_{V_{CE=Constant}} \quad \text{----- (3)} \qquad h_{oe} = \left.\frac{\Delta i_c}{\Delta v_{ce}}\right|_{I_{B=Constant}} \quad \text{----- (4)}$$

BOTTOM VIEW AND SIDE VIEW OF TRANSISTORS (BC 107 OR BC 108 OR AC 126) (Metal Case)

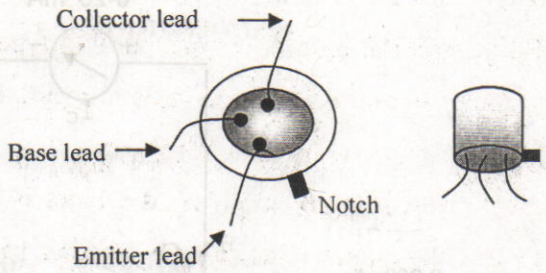


Fig.4.1

SPECIFICATIONS

STEPS TO FOLLOW

1. Identify the leads of given transistor leads with the help of notch provided on the body of the transistor.
2. Measure its β value using a digital multimeter possessing β(h_{fe}) measurement facility. Compare it manufacturer specified typical value. If the value is nearby the transistor under test is good. Use it for experiment.

3. First observe input characteristics by connecting the circuit as shown in the Fig.4.2
4. Switch-on the $DCRPS_2$ and maintain a potential of 0V at the collector.
5. Switch –on the $DCRPS_1$ and maintain a potential of 0V at the base (V_{BE}).
6. Note the corresponding base current (I_B).
7. Repeat the step-6 by maintaining V_{BE} at different potentials (i.e. 0.1V, 0.2V, ----- 0.7V) as given in Table.4.1.
8. Change the voltage at the collector (V_{CE}) to 1V and repeat the above procedure (Steps 5, 6 and 7).
9. Change the voltage at the collector (V_{CE}) to 2V and repeat the above procedure (Steps 5, 6 and 7). Note the readings in the Table.4.1
10. Switch-off the two power supplies $DCRPS_1$ and $DCRPS_2$.
11. For observing output characteristics, switch-on the $DCRPS_1$ and maintain the base current (I_B) at 10μA.
12. Now switch-on the $DCRPS_2$ and maintain the voltage (V_{CE}) at 0V and note the corresponding collector current (I_C).
13. Now take similar readings by maintaining the voltage at the collector (V_{CE}) at different fixed voltages i.e. 0.5V, 1V, 2V, 3V, ------10V, as given in the Table.4.2.
14. Change the base current I_B to 20μA and repeat the procedure (Steps12 & 13).
15. Again change the base current I_B to 30μA and repeat the above procedure (Steps12 and 13).

CIRCUIT

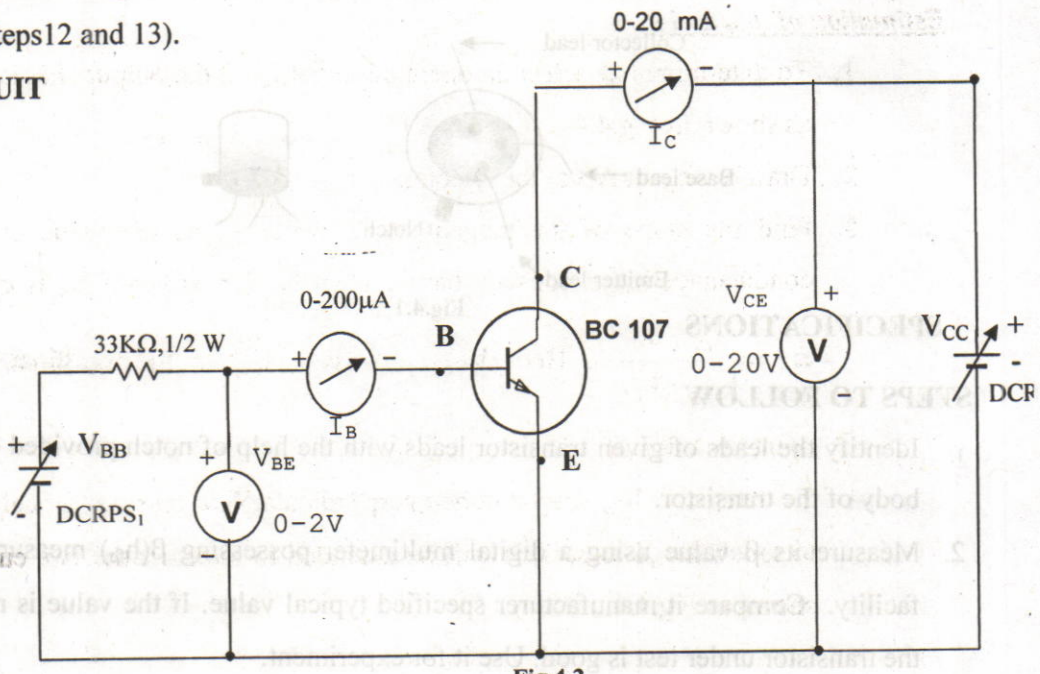


Fig.4.2

GRAPH

To draw the input characteristics, mark the variable 'V_{BE}' along X-axis and the variable 'I_B' along Y-axis on an ordinary graph paper. Mark the observed points and join them with smooth curves. Similarly to draw the output characteristics, mark the variable 'V_{CE}' along X-axis and the variable 'I_C' along Y-axis on another graph paper. Mark the observed points and join them with smooth curves.

Estimation of h_{ie} and h_{re}

1. To determine h_{ie}, select an operating point Q on the input characteristics as shown in Fig.4.3.
2. Draw a tangent RS at the Q point.
3. Find the slope of the tangent at Q.
4. The reciprocal of the slope of the tangent gives the value of input resistance h_{ie} (Eq.(1)).
5. To determine h_{re}, draw a horizontal line through Q and extend it to intersect the two curves as shown in Fig.4.3.
6. From the values of points of intersection of the I_B=constant line, with the curves, estimate the value of reverse voltage gain h_{re} using Eq.(2) i.e.

$$h_{re} = \frac{V_{BE_2} - V_{BE_1}}{V_{CE_2} - V_{CE_1}}$$

Estimation of h_{oe} and h_{fe}

1. To determine h_{oe}, select an operating point Q on the output characteristics as shown in Fig.4.4.
2. Draw a tangent AB at the Q point.
3. Find the slope of the tangent at Q, which gives the value of output conductance h_{oe} at constant base current I_B. The value of h_{oe} is given by

$$h_{oe} = \frac{I_{C_2} - I_{C_1}}{V_{CE_2} - V_{CE_1}}$$

. Here (V_{CE2}, I_{C2}), (V_{CE1}, I_{C1}) are the coordinates of the points A and B.

4. To determine h_{fe}, draw a dotted perpendicular line passing through Q and to touch the X-axis. This will be extended to intersect the two curves as shown in Fig.4.4.

5. From the values of points of intersection of the V_{CE} = constant line, with the curves, estimate the value of forward current transfer ratio or current gain h_{fe} using Eq.(3) 1.e. $h_{fe} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}}$

OBSERVATION TABLES

1) Input Characteristics

Table 4.1

S.No	V_{BE}	V_{CE} = 0V I_B	V_{CE} =1V I_B	V_{CE} =2V I_B
1	0V			
2	0.1V			
3	0.2V			
4	0.3V			
5	0.4V			
6	0.5V			
7	0.6V			
8	0.6 V			
9	0			

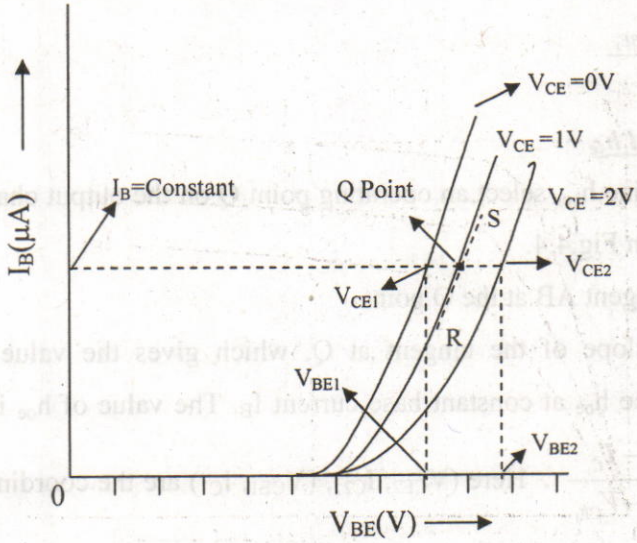


Fig.4.3

2) OUTPUT CHARACTERISTICS

Table 4.2

S.No.	V_{CE}	I_B =10μA	I_B =20μA	I_B =30μA
		I_C	I_C	I_C
1	0V			
2	1V			
3	2V			
4	3V			
5	4V			
6	5V			
7	6V			
8	7V			
9	8V			
10	9V			
11	10V			

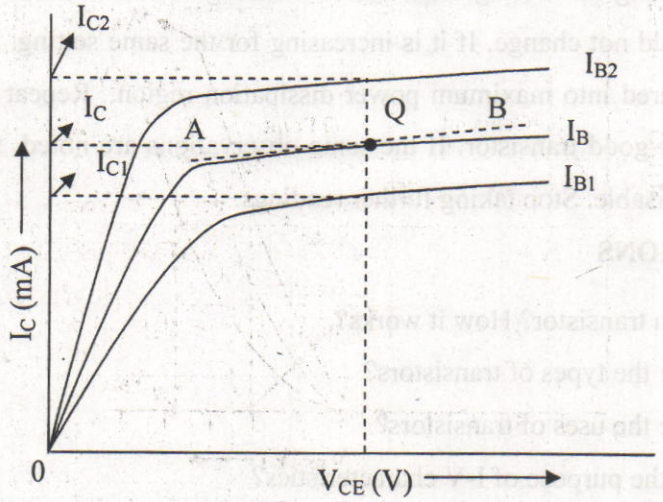


Fig.4.4

RESULT

The input and output characteristics of a given transistor in CE configuration were drawn and its h-parameters were estimated from the curves.

Parameter	Calculated value :	Standard values
h_{ie}	.....	.....
h_{re}	.....	.....
h_{fe}	.....	.....
h_{oe}	.....	.....

PRECAUTONS

1. For observing variation between input and output variables, it is to be ensured that the input/output variable must remain constant for that set of observations.Suppose you are taking observations for a given base current. As VCE is changed, sometimes IB also changes. As we are taking observations at constant IB, we have to bring back the IB value to the constanr=t value chosen by us. And then only we have to note Voltage and corresponding current readings.
2. The coarse and fine knobs of voltage variation of power supply are to be positioned in minimum before the commencement and termination of the experiment.
3. The current limit knob of DCRPS must be kept in maximum position before the commencement of experiment.
4. After increasing the Voltage take current reading and wait for about 1minit. The current should not change. If it is increasing for the same setting, the transistor is hot and entered into maximum power dissipation region.. Repeat the experiment with another good transistor. If the same observations are noted, further increase in is not advisable. Stop taking further readings.

VIVA QUESTIONS

1. What is a transistor? How it works?
2. What are the types of transistors?
3. What are the uses of transistors?
4. What is the purpose of I-V characteristics?
5. What are various configurations of the transistor?
6. Why a transistor is called a BJT?
7. What are h-parameters? What is their use?
8. Why h-parameters are more preferred as compared to other parameters?
9. Why the h-parameters are named as hybrid parameters?.

5. FET CHARACTERISTICS

AIM OF THE EXPERIMENT

To draw the drain and transfer characteristics of a given FET.

EQUIPMENT AND COMPONENTS

D.C.R.P.S (0-30V; 1A)-2 {or a Dual DC power supply with two channels}; DC current meter (0-20mA→1)-1; DMM-1; DC voltmeters (0-2V→1, 0-20V→1)-2; FET (BFW 10, BFW11)-1; Resistors (220KΩ, 1/2W-1, 470Ω, 1/2W)-2; Breadboard - 1.

THEORY

Field Effect Transistor (FET) is a semiconductor device which depends for its operation on the control of the current by an electric field. The two types of FETs are Junction Field effect Transistor (JFET) and the Insulated Gate field Effect Transistor (IGFET) or Metal-Oxide Semiconductor Field Effect Transistor [MOSFET]. The JFET is also called a *unipolar transistor* because in it the current is carried by only one type of carries (either electrons or holes). It is a transistor because its characteristics are similar to that of the transistor. It can also act as an amplifier. It exhibits only output and transfer characteristics. Another version of JFET is MOSFET, but it has much more input impendence than JFET or BJT. It can work in two modes Enhancement and Depletion. JFET is a three terminal device like BJT. The three terminals are: Source, Drain and Gate. The source S is a terminal through which through which majority carriers enter the bar. Conventional current entering the bar at S is designated by I_S. The source is similar to the emitter in BJT. The drain D is the terminal through which the majority carriers leave the bar. Conventional current entering the bar at D is designated by I_D. The JFET consists of a semiconductor bar, through which charge carriers move from source to drain. This path is called the Channel. On both sides of the bar, heavily doped regions have been formed by alloying or diffusion. These regions are called the Gate. FET possesses output and transfer characteristics. It can not exhibit input characteristics. This is because its input is always reverse biased. FET has advantages over BJT. They are: 1) Its operation depends upon the flow of majority carriers only. 2) It is a unipolar device (one carrier device) 3) It is simpler to fabricate and occupies less space in integrated form. 4) It exhibits high input resistance (many Mega Ohms). 5) It is less noisy than BJT.

BOTTOM VIEW AND SIDE VIEW OF FET (BFW 10)

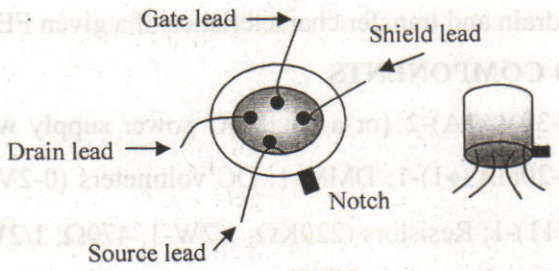


Fig.5.1

CIRCUIT

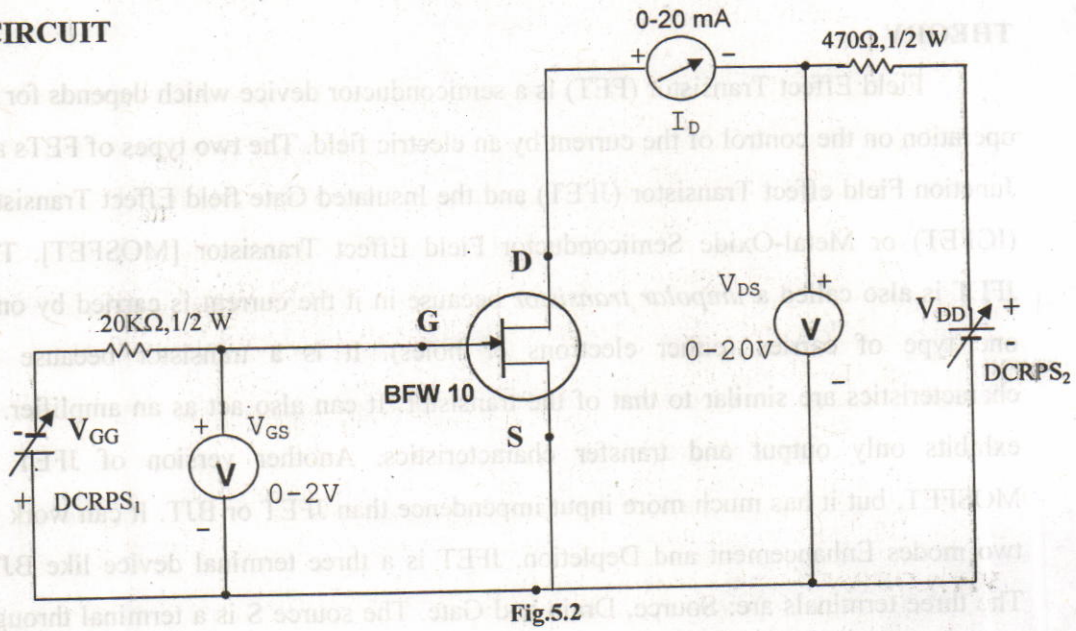


Fig.5.2

MODEL GRAPHS

i) Drain characteristics

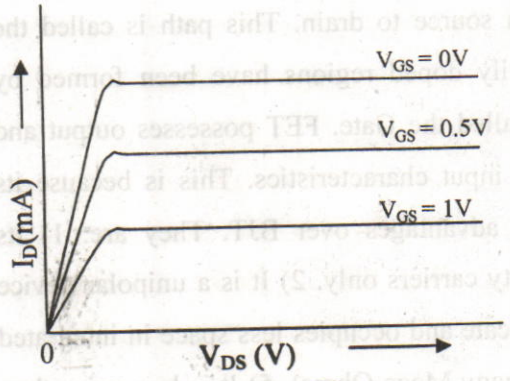


Fig.5.3

ii) Transfer characteristics

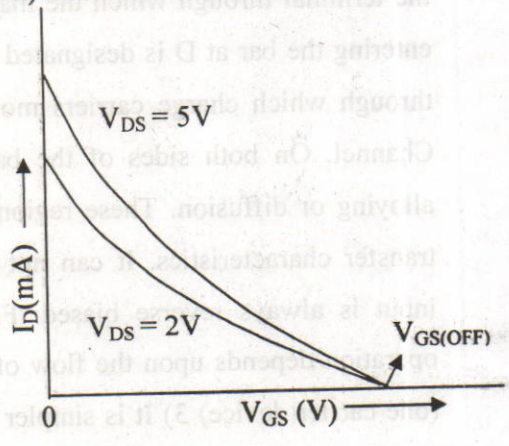


Fig.5.4

STEPS TO FOLLOW

i) Drain Characteristics

1. Identify the leads of given FET with the help of bottom view, shown in Fig.5.1.
2. Connect the circuit to draw the drain characteristics as shown in Fig.5.2.
3. Switch on the $DCRPS_1$ (Gate supply voltage V_{GG}) and set the voltage V_{GS} at 0V.
4. Now switch on the $DCRPS_2$ (Drain supply voltage V_{DD}) and set the voltage V_{DS} at 0V and note the corresponding drain current I_D.
5. Take similar readings by maintaining the voltage V_{DS} at different fixed values as given in the Table.5.1.
6. Repeat the above procedure twice at different values of V_{GS} (say at 0.5V and 1V).
7. Bring coarse and fine voltage variation knobs of both power supplies to minimum position and switch off them.
8. Take an ordinary graph paper; mark the variable V_{DS} along X-axis and the variable I_D along Y-axis.
9. Mark the observed points and join them by smooth curves as shown in Fig.5.3.

ii) Transfer Characteristics

1. Use the above circuit (Fig.5.2) to draw the transfer characteristics.
2. Switch on the $DCRPS_2$ (Drain supply voltage V_{DD}) and set the voltage V_{DS} at 2V.
3. Now switch on the $DCRPS_1$ (Gate supply voltage V_{GG}) and set the voltage V_{GS} at 0V and note the corresponding drain current I_D.
4. Take similar readings by maintaining the voltage V_{DS} at different fixed values as given in the Table.5.2.
5. Repeat the above procedure with other value of V_{DS} (say 5V).
6. Bring coarse and fine voltage variation knobs of both power supplies to minimum position and switch off them.
7. Take an ordinary graph paper; mark the variable V_{GS} along X-axis and the variable I_D along Y-axis.
8. Mark the observed points and join them by smooth curves as shown in Fig.5.4.

PRECAUTIONS

1. The coarse and fine knobs of voltage variation of power supply are to be positioned in minimum before the commencement and termination of the experiment.
2. The current limit knob of DCRPS must be kept in maximum position before the commencement of experiment.
3. Slow variation of power supply knobs is to be done.

OBSERVATION TABLES

Table 5.1 Drain characteristics

S.No.	V_{DS}	V_{GS} = 0V I_D	V_{GS} = 0.5V I_D	V_{GS} =1V I_D
1	0V			
2	0.25V			
3	0.50V			
4	0.75V			
5	1V			
6	2V			
7	3V			
8	4V			
9	5V			
10	6V			
11	7V			
12	8V			
13	9V			
14	10V			

S.No.	V_{GS}	V_{DS}=2V I_D	V_{DS}=2V I_D
1	0V		
2	0.5V		
3	1V		
4	1.5V		
5	2V		
6	2.5V		
7	3V		
8	3.5V		
9	4V		
10	4.5V		

Table 5.2 Transfer characteristics

VIVA QUESTIONS

1. Give the differences between FET and BJT.
2. Why FET is a Unipolar device?
3. What is the magnitude of input impedance of the FET?
4. What is the difference between JFET and MOSFET?
5. What is the purpose of the channel in JFET?
6. What do you mean by JFET?
7. Mention the uses of JFET?
8. What is the purpose of reverse biasing the Gate in JFET?

RESULT

The transfer and drain characteristics of FET were drawn.

6.a UNI JUNCTION TRANSISTOR (UJT)

AIM OF THE EXPERIMENT

To draw the V-I characteristics of given UJT and to estimate its parameters: i) Inter Base Resistance (R_{BB}) and ii) Intrinsic Stand off Ratio (η).

EQUIPMENT AND COMPONENTS

D.C.R.P.S(0-30V,1A)-2 { or a dual DC power supply - 1); DC-Voltmeter (0-20V)-1; DMM-1; DC-Current meter (0-20mA)–1; UJT (2N2646) – 1; Resistors (1KΩ, 1/2W-1; 100Ω, 1/2W-1)-2.

FORMULA

Intrinsic stand off ratio

$$\eta = \frac{V_P - V_D}{V_{BB}}$$

V_P = Peak point voltage

V_D = Emitter junction voltage drop (0.7V for Silicon UJT); V_{BB} = Inter base voltage.

SYMBOL OF UJT

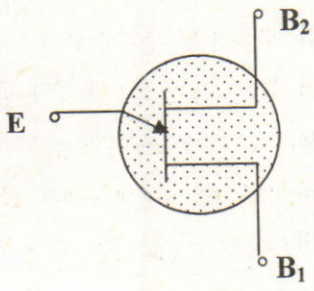


Fig.6.1a

BOTTOM VIEW OF UJT 2N 2646

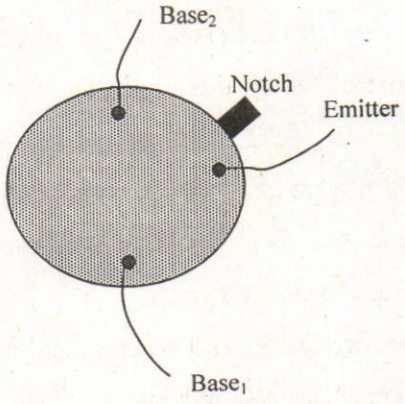


Fig. 6.1b

THEORY

A Uni Junction Transistor has only one PN-junction unlike bipolar junction transistor and unipolar Field Effect Transistor. It is basically a three terminal silicon diode with one emitter and two base terminals. However, it differs from an ordinary diode in that it has three leads. It resembles a FET because in that it has only one PN-junction, but differs from the FET because in normal operation that junction is forward biased in FET. The EET and UJT have also a constructional difference in that

the gate surface of FET is much larger than the emitter junction of UJT. It also differs from a FET in that it has no ability to amplify.

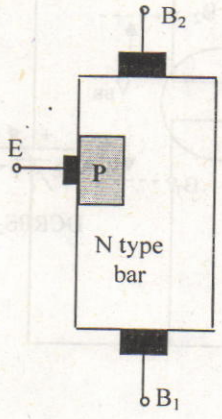


Fig.6.2

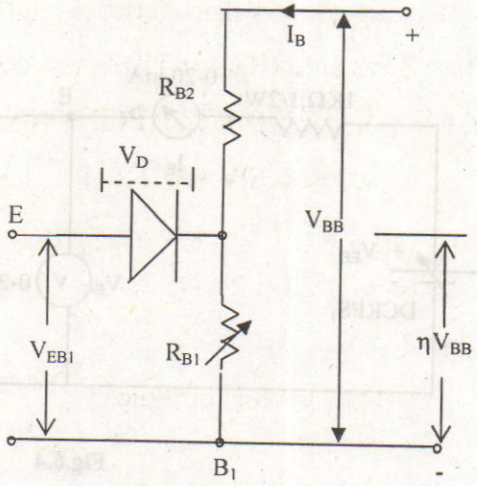


Fig.6.3

The UJT is a 3-terminal device, having one emitter junction and two base Ohmic contacts ($Base_1$ and $Base_2$). A PN-junction located between base B_1 and base B_2, is called the Emitter junction.

It consists of a lightly doped N-type silicon bar with a heavily doped P-type material alloyed to its one side (closer to B) for producing single PN- junction. As shown in Fig.6.2, there are 3-terminals, one emitter and two bases B_1 and B_2 at the top and bottom of Silicon bar. The emitter leg is drawn at angle to vertical and arrow points in the direction of conventional current (Filament transistor, Double Base Diode are the other names of UJT). Fig.6.3 shows the equivalent circuit. The resistance of the Silicon bar is called the Inter-Base Resistance (R_{BB}). It is represented by two resistors R_{B1} and R_{B2} in series. R_{B2} is the resistance of Silicon bar between B_2 and the emitter junction. R_{B1} is the resistance of bar and emitter junction. This resistance is shown variable because its value depends upon the voltage across the PN- junction. The PN- junction is represented in the emitter by a diode D. If a voltage V_{BB} is applied between the bases with emitter open, the voltage will divide up across R_{B1} and R_{B2}.

CIRCUIT

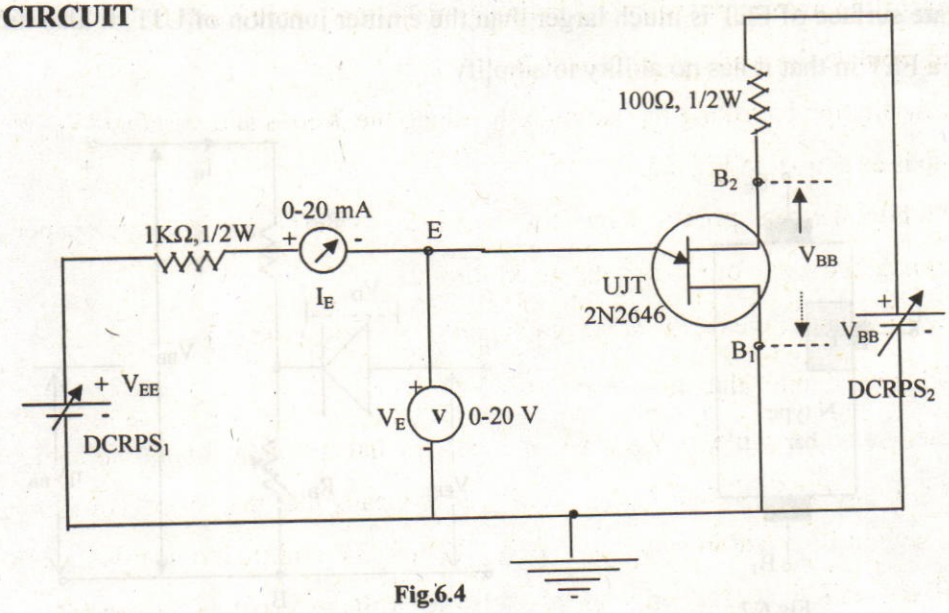


Fig.6.4

STEPS TO FOLLOW

1. Identify the leads of UJT with the help of bottom view, given in Fig.6.1.
2. To measure the inter-base resistance R_{BB}, connect an Ohmmeter (DMM) between two bases leads B_1 and B_2. Now measure the resistance R_{BB}. (It may probably of the order of few KΩ)
3. To estimate the value of η (Intrinsic stand off ratio), connect the given UJT in the circuit with all the necessary components as shown in the Fig.6.4.
4. Switch on the $DCRPS_2$ (V_{BB}) and maintain a potential difference of 6V between base-2 and base-1.
5. Switch on the $DCRPS_1$ (V_{EE}) and maintain a potential difference of 0V at the emitter E.
6. Change the emitter voltage V_E to other values with the help of $DCRPS_1$ and note the corresponding Emitter currents (I_E).
7. Continue the variation of emitter voltage slowly in step of 1V, approximately equal to the peak point voltage and then vary the voltage in step of 0.1V till UJT fires (UJT shows sudden increase in I_E from its previous value (0mA) and falls to valley voltage).
8. Now onwards, vary the voltage in step of very small increment (approximately 0.02 or 0.05V) because UJT is in saturation and note the emitter currents. Tabulate the readings in Table 6.1.

9. Repeat the above procedure by maintaining V_{BB} at some other value (say 12V) and tabulate the readings in Table 6.2.
10. Draw a graph by taking the variable 'I_E' along the X-axis and variable 'V_E' along Y-axis as shown in Fig.6.5.
11. Find bout the peak point voltage (V_P) from the curve drawn on the graph paper.
12. Estimate the value of η using the given formula.
13. Draw another curve on the same graph paper and repeat the steps 11 and 12.
14. Find the average value of η.

{✡ Note: As an example, if V_{BB} = 6V and assume that η=0.5 then approximately the value of V_P is $V_P = 0.5 \times 6 + 0.7 = 3.5V$. This means that the variation of emitter voltage should be made in step of 1V from 0V upto 3V and then onwards in step of 0.1V till the UJT fires {suddenly V_E falls to valley voltage V_V (may be around 1.1V). After this condition, vary in step of 0.05V}. In the same way, a student can decide the variation of V_E when V_{BB} = 12V or any DC other voltage}.

GRAPH

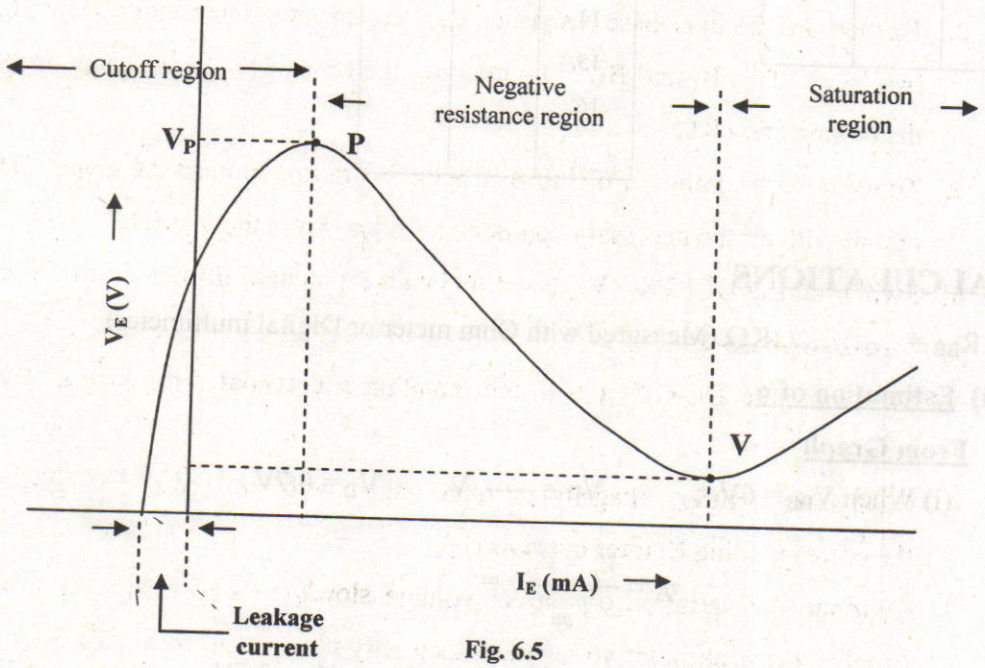


Fig. 6.5

Table 6.1
$V_{BB} = 6V$

S.No.	V_E	I_E
1.	0V	
2.	1V	
3.	2V	
4.	3V	
5.		
6.		
7.		
8.		
9.		
10.		
11.		
12.		

Table 6.2
$V_{BB} = 12V$

S.No.	V_E	I_E
1.	0V	
2.	1V	
3.	2V	
4.	3V	
5.	4V	
6.	5V	
7.	6V	
8.		
9.		
10.		
11.		
12.		
13.		
14.		
15.		
16.		

Table 6.3

S.No	V_{BB}	V_P	η
1.	6V		η_1=
2.	12V		η_2=

CALCULATIONS

(i) R_{BB} = ...KΩ (Measured with Ohm meter or Digital multimeter)

(ii) **Estimation of η**

From Graph

(i) When $V_{BB} = 6V$; Vp = ----- V, $V_D = 0.7V$

$$\eta_1 = \frac{V_P - V_D}{V_{BB}} =$$

(ii) When $V_{BB} = 12V$; Vp = ------- V, $V_D = 0.7V$

$$\eta_2 = \frac{V_P - V_D}{V_{BB}} =$$

Average value of η is given by $\eta = \frac{\eta_1 + \eta_2}{2} =$

RESULT

The V-I characteristics of given UJT were drawn and its parameters were estimated.

Inter base resistance (R_{BB}) = ------- KΩ.

Intrinsic stand off ratio (η) = --------

PRECAUTIONS

1. For UJT theR_{BB} value lies between 4 to 8K If it is >10K, take another UJT
2. While changing the emitter voltage V_E from one value to another, after approaching peak point voltage, a small amount of time has to be lapsed at each observation.
3. The peak and valley voltages are to be noted carefully.
4. The coarse and fine knobs of voltage variation of DCRPS are to be kept in minimum position before and after termination of the experiment.

VIAVA QUESTIONS

1. What is a UJT?
2. What are the uses of UJT?
3. What peculiar property is exhibited by UJT its emitter characteristics?
4. What is the intrinsic stand off ratio? Give the range of this value.
5. What is the difference between UJT and BJT?
6. Is there any use of negative resistance region? If so specify it?
7. What are the other names of UJT?

6.b UJT RELAXATION OSCILLATOR

AIM OF THE EXPERIMENT

To construct a relaxation oscillator using the given UJT and to estimate the frequency of generated waveform.

EQUIPMENT AND COMPONENTS

D.C.R.P.S(0-30V;1A)-1; Decade Capacitance Box (DCB)-1 or · Independent capacitors (0.22μF-1, 0.33μF-1, 0.47μF-1) -3 ; DMM-1; CRO-1; Bread board-1; UJT (2N2646) – 1 ; Resistors (33KΩ,1/2W-1; 100Ω,1/2W-2)-3.

FORMULA

Time period of the saw tooth waveform (T)

$$T = 2.303.R_T.C_T \log_{10}\left[\frac{V_{BB} - V_V}{V_{BB} - V_P}\right]$$

Where R_T = Resistance in ohms

C_T = Capacitance in Farads

V_{BB} = Inter-base voltage

V_P = Peak point voltage

V_V = Valley voltage

Frequency of saw tooth waveform (f) =1/T Hz

THEORY

Oscillator is an electronic circuit that generates sinusoidal or non sinusoidal waveforms on its own without any input. The circuit that generates sawtooth waveform is called a Relaxation oscillator. It is so called because the output varies linearly with time and drops suddenly (relax) to zero. On account of the negative resistance region exhibited by UJT and its particular behaviour, the UJT finds its application in a variety of circuits. They are: Relaxation oscillator, switching, sawtooth wave generator, timing circuits, amplification, voltage or current regulated supplies. Fig.6.5 shows the circuit of UJT as relaxation oscillator. In this, the discharging of a capacitor through UJT can develop a sawtooth output as shown in Fig.6.6.

When the power supply (V_{BB}) is switched on, the capacitor C_T charges through resistor R_T exponentially until the voltage across it reaches the peak point

voltage V_P. At this point, PN junction becomes forward biased and the UJT switches into negative resistance region (i.e. V_E decreases and I_E increases). The capacitor then quickly discharges through the forward biased PN-junction and R_{B1}. When the capacitor voltage decreases to the valley point voltage (V_V), the UJT turns off, the capacitor begins to charge again and the cycle is repeated as shown in Fig.6.6. The frequency of sawtooth wave can be varied by changing either the value of C_T or R_T as they control the time constant R_TC_T of the capacitor changing circuit. Time period of sawtooth waveform (if η is known) is given by

$$T = 2.303.R_T.C_T \log_{10}\left[\frac{V_{BB} - V_V}{V_{BB} - V_P}\right]$$

CIRCUIT DIAGRAM

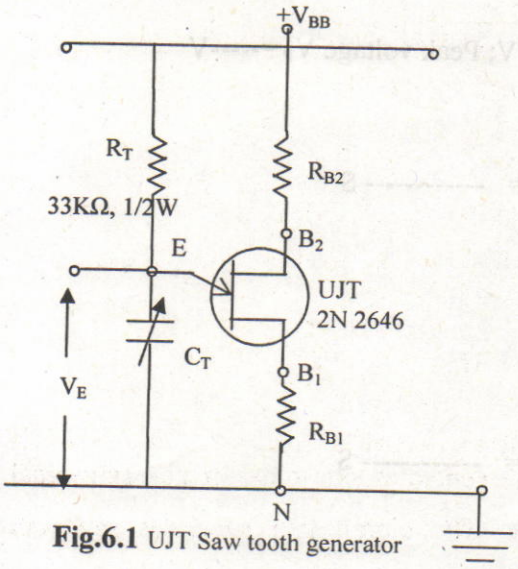


Fig.6.1 UJT Saw tooth generator

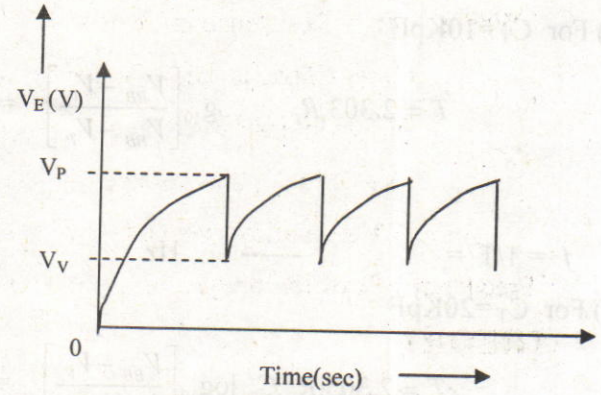


Fig 6.2 Saw tooth output across capacitor

1. Identify the leads of UJT with the help of bottom view.
2. Connect the circuit as shown in the Fig.6.1.
3. Apply a p.d of 5V to the circuit with the help of a voltage source (DCRPS).
4. Introduce some capacitance value say (0.22μF) using a capacitance box (DCB) or a 0.22μF capacitor.
5. Observe the sawtooth waveform across the capacitor on CRO screen and note the values of V_V and V_P. Simultaneously note the time period and estimate frequency.
6. Note the above values in Table.1.
7. Using the values of V_V and V_P, estimate the time period and frequency of the waveform (Theoretical).

8. Again repeat the above procedure twice by introducing or changing the capacitance value to 0.33μF and 0.47μF.
9. Compare these values with theoretical frequencies calculated earlier.

Table.1

S.No.	Capacitance (C_T)	Time period (T)		Frequency (f)	
		Theory	Practical	Theory	Practical
1	0.22μF				
2	0.33μF				
3	0.47μF				

CALUCULATIONS

From the obtained sawtooth waveform,

Valley voltage V_V = -----V; Peak voltage V_P =-----V

1) For C_T=10KpF

$$T = 2.303.R_T. \log_{10}\left[\frac{V_{BB}-V_V}{V_{BB}-V_P}\right] = \text{---------- S}$$

f = 1/T = ------ Hz

2) For C_T=20KpF

$$T = 2.303.R_T.C_T \log_{10}\left[\frac{V_{BB}-V_V}{V_{BB}-V_P}\right] = \text{---------- S}$$

f = 1/T = ------ Hz

3) For C_T=30KpF

$$T = 2.303.R_T.C_T \log_{10}\left[\frac{V_{BB}-V_V}{V_{BB}-V_P}\right] = \text{---------- S}$$

f = 1/T = ------ Hz

RESULT

A relaxation oscillator using the given UJT was constructed and the frequency of generated sawtooth waveform was estimated.

PRECAUTONS

1. The AC/DC coupling slide switch of the channel on which the waveform is observed is to be kept at DC.
2. The time period is to be measured accurately by choosing suitable ranges of the time base switch.

VIVA QUESTIONS

1. What is a UJT?
2. What is an oscillator?
3. What is negative resistance region? What is its use?
4. What other devices exhibit negative resistance region?
5. What are the uses of UJT?
6. The coarse and fine knobs of voltage variation of DCRPS are to be kept in minimum position before and after termination of the experiment.

Suggestions:

1. Keeping R_TC_T product as constant repeat experiment with different values of C_T Observe the changes in the waveform for each setting. Record them on a tracing paper.
2. Double the value of R_TC_T and observe the changes in the shape of Saw tooth wave.

7. RC-COUPLED AMPLIFIER

AIM OF THE EXPERIMENT

a) To study the frequency response of single stage CE amplifier b) To study the effect of negative feedback in the circuit.

EQUIPMENT AND COMPONENTS

DCRPS – 1; CRO -1; Function generator (Signal generator)-1; Bread board- 1; Electrolytic capacitors – 3 (10μF/25V-2; 50μF/25V-1); Transistor – 1(BC 107, BC109, BC147, BC547); Resistors -4 (1KΩ,1/2W →1; 4.7KΩ,1/2W →1; 8.2KΩ,1/2W →1; 33KΩ,1/2W →1).

THEORY

Amplifier is an electronic circuit that raises the strength of a weak signal that appears at its input. Amplification is the phenomenon that is accomplished by an amplifier. A transistor can act as an amplifier when it is working in the active region.

A single-stage BJT (one transistor with other components) circuit may be employed as a small-signal amplifier, but two cascaded stages (cascading means combining the output of one amplifier to the input of other amplifier) give much greater amplification. Amplifiers can be classified according to

(1) Use : Voltage, current, trans conductance and trans resistance

(2) Method of analysis : Small signal, large signal

(3) Frequency range : Audio frequency (A.F.)
Intermediate frequency (I.F)
Radio frequency (R.F)
Video frequency (V.F)

(4) Conduction angle (or) operating point: Class A, Class B, Class AB, Class C

(5) Coupling scheme : Direct, RC, Inductance, Transformer

For high input impedance, a FET may be used as an input stage with a BJT as the second stage. When the input signal is so weak as to produce small fluctuations in the collector current compared to its quiescent value, the amplifier is called Small signal amplifier or voltage amplifier. Such an amplifier is used as the first stage of the amplifier system used in radio and TV receivers, tape recorders, stereos and measuring instruments. As the voltage gain of a single stage (one transistor) amplifier is not sufficient for practical purposes, we use more than one stage. Such an amplifier is called a Multistage Amplifier or a Cascaded Amplifier. Much higher gains can be

obtained from multi-stage amplifiers. The gain of an n-stage amplifier with individual gains as $A_1, A_2, A_3, \ldots\ldots, A_n$ is $A_1 \times A_2 \times A_3 \times A_4 \times \ldots\ldots \times A_n$. If $A_1, A_2, A_3, \ldots\ldots, A_n$ are expressed in decibels then the overall gain is $A = A_1 + A_2 + A_3 + A_4 + \ldots\ldots + A_n$. The reason for use of decibel gain is (i) It permits gains to be directly added when a number of stages are cascaded (ii) It permits us to denote, both very small as well as very large, quantities of linear scale by conveniently small figures RC-couple amplifier is most convenient and least expensive. It has a wide frequency response; has less frequency distortion.

$$\text{Voltage gain} = A_V = V_O / V_{IN}$$

CIRCUIT

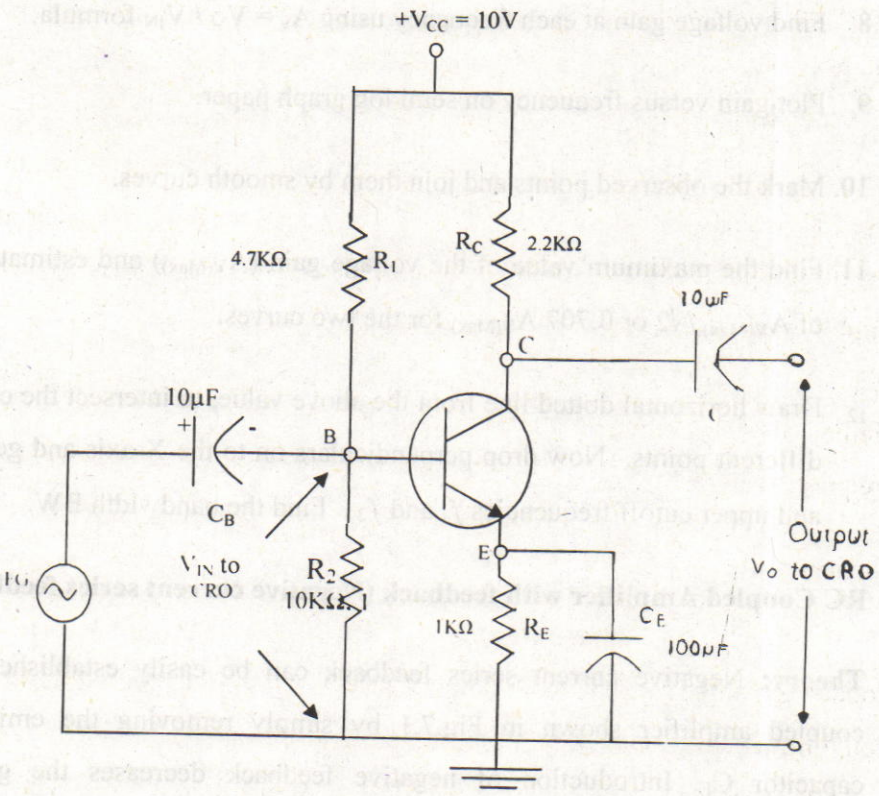


Fig.7.1 RC-coupled amplifier

STEPS TO FOLLOW

RC Coupled Amplifier without feedback

1. Identify the given components (resistor, capacitor, transistor)
2. Check the given transistor for its correctness using a multimeter possessing β measurement facility.
3. Connect the circuit as shown in Fig.7.1.

4. Switch on the DC RPS and apply a potential of 10V to the circuit.
5. Switch on the function generator and fix suitable input V_{IN} to set undistorted output waveform at 1 KHz frequency with the help of a CRO.
6. Note the input voltage Vin by giving function generator output directly to B channel of CRO. Its value will be below 50mV. Throughout the experiment, the input value has to be kept at this value before measuring output voltage Vo.
7. Vary the frequency from 10Hz to 1MHz in convenient steps and note V_o in the Table.7.1. Take as many observations as possible around the corners of response curve
8. Find voltage gain at each frequency using $A_v = Vo / V_{IN}$ formula.
9. Plot gain versus frequency on semi log graph paper.
10. Mark the observed points and join them by smooth curves.
11. Find the maximum value of the voltage gain ($A_{V(Max)}$) and estimate the value of $A_{V(Max)}/\sqrt{2}$ or 0.707 $A_{V(Max)}$ for the two curves.
12. Draw horizontal dotted line from the above value, to intersect the curve at two different points. Now drop perpendiculars on to the X-axis and get the lower and upper cutoff frequencies f_1 and f_2. Find the bandwidth BW.

RC Coupled Amplifier with feedback (Negative current series feedback)

Theory: Negative current series feedback can be easily established in a RC coupled amplifier shown in Fig.7.1 by simply removing the emitter bypass capacitor C_E. Introduction of negative feedback decreases the gain of the amplifier, decreases the lower cut-off frequency and increases the upper cut-off frequency If A^1 and A are gains with and without feedback, f_1^1 and $f_1$are the lower cut-off frequencies with and without feedback, f_2^1 and f_2 are the upper cut-off frequencies, with and without feedback, if feedback ratio is β, these are connected by the relations

$$A' = \frac{A}{1+A\beta}; \qquad f_1' = \frac{f_1}{1+A\beta}; \qquad f_2' = f_2(1+A\beta)$$

The bandwidth BW^1 with feedback is given by f_2^1-f_1^1. The bandwidth without feedback BW is given by f_2 - f_1. As f_1 and f_1^1 are in Hertz and f_2 and f_2^1 are in Kilo Hertz, the bandwidth $BW^1 \approx f_2^1$ and $BW \approx f_2$.

1. Follow steps mentioned in without feedback case assemble the circuit and plot the frequency response curve. Now remove the emitter bypass capacitor C_E from the circuit. The circuit becomes the amplifier with current series feedback.

2. Repeat the experiment as in the case of without feedback case.

3. You will notice that gain has decreased, lower corner frequency shifted to a value less than that of without feedback case, the upper corner frequency extended to a value greater than the without feedback case. So you choose the frequencies such that the graph is covered evenly with the points and fill the table. Plot the graph preferably on the graph plotted for without feedback case .Determine the upper and lower cutoff frequencies f_2^1 and f_1^1 for the second curve and then estimate the new bandwidth BW^1 (with feedback).

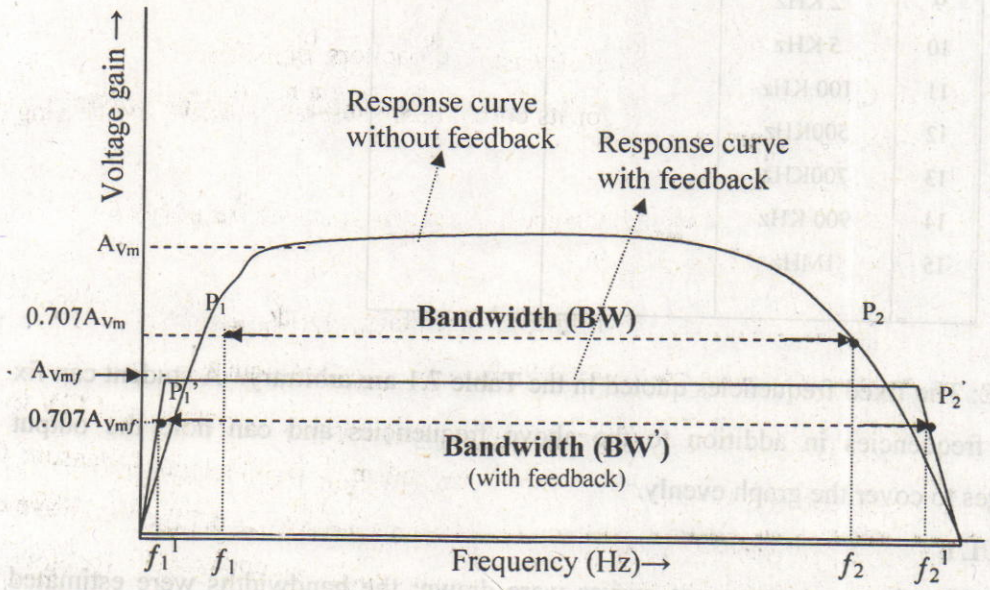


Fig.7.2

4. Compare the above bandwidths obtained for the two curves as shown in Fig.7.2.

5. Using the above mentioned formulae, verify calculate A^1. f_2^1 and f_1^1 and check how far the calculated values are in agreement with observed values.

Table 7.1

V_{IN} = ...V

S.No.	Frequency f	Output voltage Vo	Voltage gain A_V
1	10 Hz		
2	20 Hz		
3	100 Hz		
4	200 Hz		
5	500 Hz		
6	700 Hz		
7	1 KHz		
8	1.5 KHz		
9	2 KHz		
10	5 KHz		
11	100 KHz		
12	500KHz		
13	700KHz		
14	900 KHz		
15	1MHz		

NOTE: The fixed frequencies quoted in the Table 7.1 are arbitrary. A student can fix other frequencies in addition to the above frequencies and can note the output voltages to cover the graph evenly.

RESULT

The frequency response curves were drawn; the bandwidths were estimated (with and without feedback) and were compared.

Observed:

BW (without feedback) = ----------; BW (with feedback) = ----------;

Calculated

Gain with feedback = ----------; BW (with feedback) = ----------;

f_1^1 = ; f_2^1 =

VIVA QUESTIONS

1. What is an amplifier?
2. Which device can act as an amplifier?
3. Under what conditions, transistor can act as an amplifier?
4. What is bandwidth?
5. What is feedback? Mention the types?
6. What is the effect of negative feedback on bandwidth?
7. What are the advantages of RC-coupling?
8. Why the gain of RC-coupled amplifier remains constant in mid frequency region?
9. What is a frequency response curve?
10. What is a cutoff frequency?
11. What is the purpose of electrolytic capacitors used in RC-coupled amplifier?
12. What are the names of other coupled amplifiers?
13. What is the use of coupling two stages of an amplifier with coupling elements?
14. Mention some coupling elements?

Suggestions:

1. It is very important to come prepared with the relevant theory behind the practical and to know what parameters have to be measured and to know how each component behaves in the circuit. Taking observations with the circuit that was assembled by others is almost equal to copying the observations. You must be proud of and confident about your observations. These come only if you do the practical with knowledge. You can select your own transistor (it need not be BC107) Also you may select your C_B, C_E and C_C values. The collector and biasing resistors can also be changed. No harm will be done if you replace a 2.2KΩ resistor with a 2KΩ or 2.5KΩ resistor available in the store. Don't try to reproduce the results of others. You compare them

with the calculated values and see whether you are committing any errors if there is no agreement. Lab supervisors are requested to encourage this approach.

2. Change C_B and C_C from 1μF to 250 μF with available standard values and study the low frequency response curve for each value and observe changes in the frequency response curve.
3. Change the emitter bypass capacitor C_E in steps of 10μF from 1μF onwards and observe changes in the response curve.
4. Interchange R_1 and R_2 and repeat the experiment. Note your observations.
5. Double the collector resistance and repeat the experiment.
6. Connect 1000pF capacitor across the output and determine the frequency response curve. Compare with the earlier response curve.
7. Usually function generators give output more than 100mV. But we are supposed to give an input of 30mV only. Instructors are advised to order those function generators that provides variable output in the range 10 to 100mV.
8. Use a CRO to measure the amplitude of 30mV signal. Multimeters have poor frequency response and are not suitable to measure amplitudes of signals of frequency above 5 KHz. So do not measure audio frequency and radio frequency voltages with DMMs or analog multimeters. You may use FET VTVMs with R.F probe for this purpose.
9. Measure the frequency of the function generator at different frequencies in the frequency range of response curve with a CRO and check whether the face readings are agreeing with measured values or not.
10. Replace the BC107 transistor with BC147 transistor and plot the response curve. What changes did you observe? Repeat the experiment.
11. Change V_{cc} from 12 to 5V DC and repeat the experiment. Change V_{cc} to 15V and repeat the experiment.

8. LIGHT DEPENDANT RESISTOR (LDR)

AIM OF THE EXPERIMENT

To draw the Light Intensity -Resistance characteristic of a given LDR.

EQUIPMENT AND COMPONENTS

Auto transformer (variable AC source)-1; Lamp arrangement-1; Bread board-1; Ohmmeter (DMM)-1; Digital Luxmeter-1; LDR-1.

CIRCUIT DIAGRAM

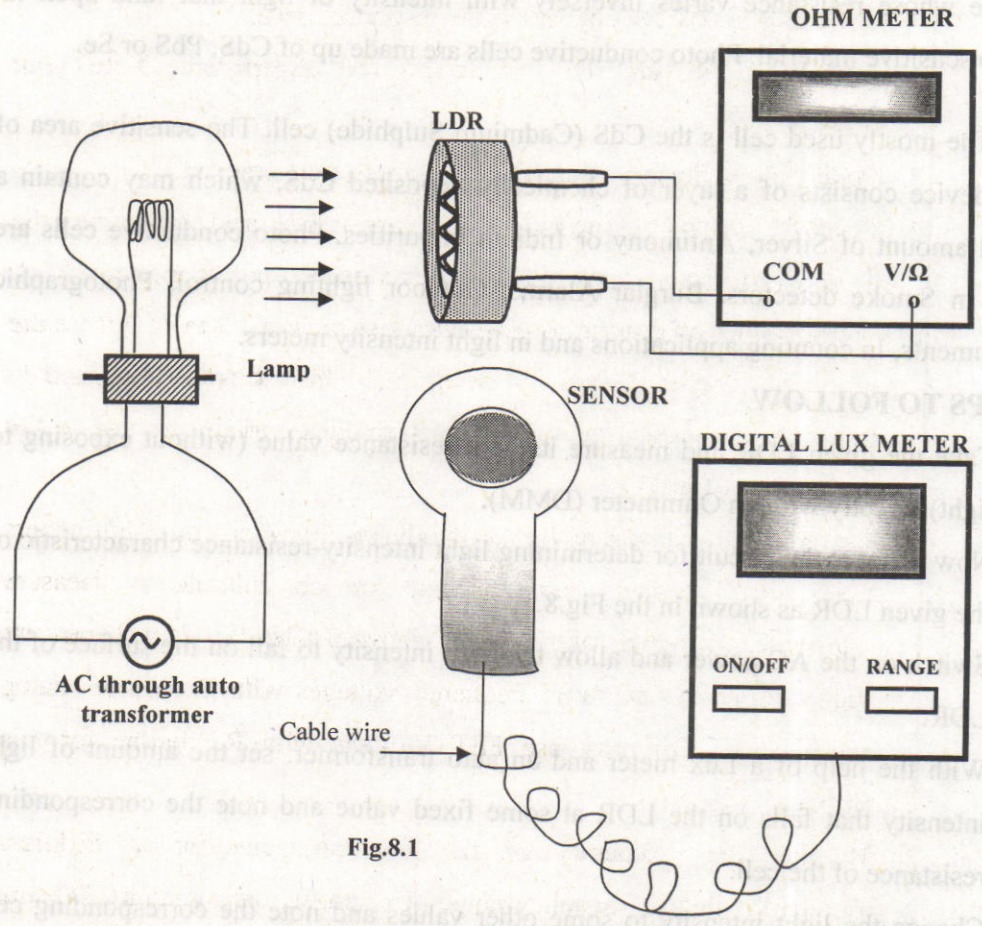


Fig.8.1

THEORY

LDR is also known as a Photoconductive cell. The phenomenon of increase in conductivity of a semiconductor when exposed to radiation is known as **Photo Conductivity**. If radiation falls upon a semiconductor, its conductivity increases. The conductivity σ of a semiconductor increases with the increase of concentration of charge carriers according to the relation $\sigma = (n\mu_n + p\mu_p)e$ where n is the magnitude

of free electron concentration; p is the magnitude of hole concentration, μ_p, μ_n are the hole and electron mobilities; e is the electron charge. If the radiation, possessing energy hν (greater than E_g), falls on a semiconductor, this radiation will be utilized to break the covalent bonds. As a result, new electron-hole pairs are created in excess of those generated thermally. These increased current carries decrease the resistance of the material and hence such a devise is called a ***Photo Resistor*** or a ***Photo Conductor*** or a ***Light Dependent Resistor*** (*LDR*). Photo conductive cell is a semiconductor device whose resistance varies inversely with intensity of light that falls upon its photo sensitive material. Photo conductive cells are made up of CdS, PbS or Se.

The mostly used cell is the CdS (Cadmium Sulphide) cell. The sensitive area of this device consists of a layer of chemically deposited CdS, which may contain a small amount of Silver, Antimony or Indium impurities. Photo conductive cells are used in Smoke detectors, Burglar Alarms, Outdoor lighting control, Photographic instruments, In counting applications and in light intensity meters.

STEPS TO FOLLOW

1. Take the given LDR and measure its dark resistance value (without exposing to light) directly with an Ohmmeter (DMM).
2. Now connect the circuit for determining light intensity-resistance characteristic of the given LDR as shown in the Fig.8.1.
3. Switch on the AC power and allow the light intensity to fall on the surface of the LDR.
4. With the help of a Lux meter and an auto transformer, set the amount of light intensity that falls on the LDR at some fixed value and note the corresponding resistance of the cell.
5. Change the light intensity to some other values and note the corresponding cell resistance readings.
6. Finally draw a graph by taking the variable '**light intensity**' along X-axis and the variable '**cell resistance**' along Y-axis.
7. Mark the observed points and join them by a smooth curve as shown in Fig.8.2.

MODEL GRAPH

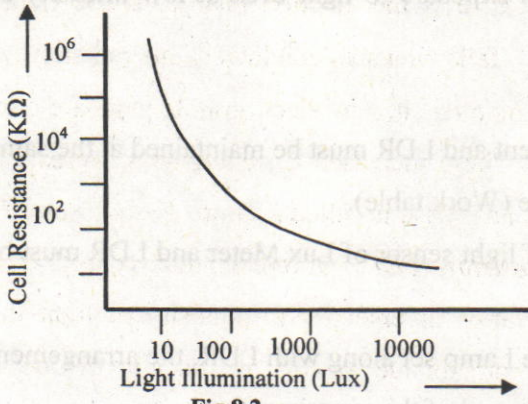


Fig.8.2

OBSERVATION TABLE

Dark resistance of LDR > ------ MΩ

S.No.	Applied Voltage	Light Intensity (Lux)	Cell Resistance (KΩ)
1.	230V		
2.	220V		
3.	210V		
4.	200V		
5.	190V		
6.	180V		
7.	170V		
8.	160V		
9.	150V		

RESULT

The Light intensity-Resistance characteristic of the given LDR was drawn.

The variation of resistance with light intensity is non linear. The resistance falls very sharply with exposure to light even at low intensity and levels of at high intensity.

PRECAUTIONS

1. The bulb filament and LDR must be maintained at the same height from the reference plane (Work table).
2. The surfaces of light sensor of Lux Meter and LDR must be in the same vertical plane.
3. After fixing the Lamp set along with LDR, the arrangement should not be disturbed till the end of the experiment.

VIVA QUESTIONS

1. What is the other name of LDR?
2. What are the uses of LDR?
3. Explain the phenomenon of photoconductivity.
4. What are the materials used to manufacture the LDR?
5. What is spectral response?
6. What is an auto transformer? What is its use?
7. What is the use of lux meter?
8. What do you mean by dark resistance?
9. How do you explain the non-linearity of the observed characteristic?
10. What is the principle involved in the working of Lux Meter?
11. What precautions do you take in using LUX meter?

Suggestions:

You have now at your disposal a very useful device. Using an R.C coupled amplifier and a Photo resistor you can develop very useful projects like Burglar's alarm by incorporating a relay and electrical alarm. By interfacing a digital counter to the amplifier output, you can count the number of visitors that attended a function. By interfacing a digital camera, you can even take snap shots of the visitors as they enter. The system can be placed at important places in a concealed manner to avoid theft or to identify the thieves. **Electronics For You** magazine old issues contain good number of projects. Try to develop them in the lab. Developing such projects enhances interest in the subject.

9. RC – PHASE SHIFT OSCILLATOR

AIM OF THE EXPERIMENT

To design an RC – Phase shift Oscillator and to estimate the frequency of generated output.

EQUIPMENT AND COMPONENTS

DCRPS -1, CRO – 1, Transistor -1 (any general purpose transistor like BC 107); Electrolytic capacitor – 1 (50 μF/63V); Polyester/Ceramic disc capacitors – 3 (taken after design); potentiometer (10KΩ) – 1; Resistors – 3 (10KΩ, 1KΩ, 33KΩ)

THEORY

Oscillator is an electronic circuit that produces sinusoidal or non-sinusoidal wave forms on its own without any input signal. Oscillator can be either RC or LC type. RC Phase shift oscillator is an RC oscillator. This utilizes RC network.

The gain of an amplifier with feedback is given by

$A_f = \frac{A}{1 - A\beta}$ where A is the gain without feedback and β is the feedback factor. If $A\beta = 1 \angle 0^0$, the gain with feedback is infinity. Under such conditions the amplifier provides its own inputs, i.e., it works as an oscillator. The conditions for production and maintenance of oscillations may be achieved in a variety of ways. The method adopted mainly depends on the frequency range. In general a single stage amplifier provides 180^0 phase shift (in CE mode) and an additional phase shift of 180 is provided by appropriate feedback networks. At audio frequencies, RC networks are used while at radio frequencies LC networks are used. The circuit diagram of phase shift oscillator is shown in Fig.9.1. Here the conventional BJT shifts the phase by 180^0. The amplifier is followed by three cascaded RC circuits, the output of the last RC combination being fed back to the base. The R value used in the RC sections must be same. Likewise the Capacitors also must have same value. So that at a particular frequency each section contributes a phase shift of 60 degrees and the total phase shift introduced by 3 segments will be will be 180 degrees. At this frequency, the total phase shift is 360^0 or 0^0 leading between input and feedback signal and the system oscillates, provided the amplifier gain makes up for the attenuation due to the RC network. In the circuit you see only two Resistances and three capacitors. The input resistance $R_i \approx h_{ie}$ acts as the resistor for third segment. However the value of R_i may

not be equal to R used in the circuit. In such a case 180 total phase shift cannot be achieved. To overcome this problem a resistance in series with R_i is added so that $R = R_i + R^1$.

The frequency of oscillation of this circuit is given by

$$f_0 = \frac{1}{2\pi RC}\cdot\frac{1}{(6+4K)^{1/2}} \qquad \text{(E7.1)}$$

where $K = R_c/R$.

Conditions for sustained oscillations is

$$h_{fe} \geq 4K + 23 + \frac{29}{K} \qquad \text{(E7.2)}$$

CIRCUIT

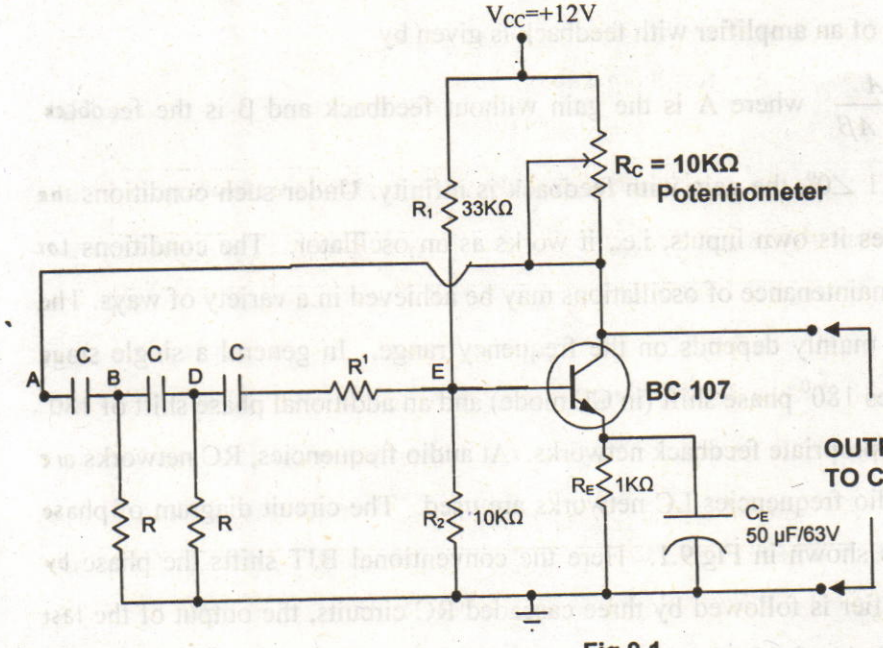


Fig.9.1

DESIGN PROCEDURE

1. Eq.(2) shows that h_{fe} is minimum for K = 2.7. So the minimum value of h_{fe} = 44.5. Hence choose a transistor with h_{fe} value (current gain or β) > 50.
2. Determine or find the input impedance (h_{ie}) of the transistor from data sheets.
3. Estimate R^1 value using $R^1 = R - h_{ie}$ at a selected value of R. For example : If h_{ie}=2KΩ; and let R = 2.2KΩ then $R^1 = R - h_{ie}$=2.2KΩ-2KΩ = 200Ω.

4. Evaluate R_C for optimum value of K=2.7 i.e., $R_C = KR = 2.7 \times 2.2K\Omega \approx 6K\Omega$ As this value may not be in lab use a 10KΩ potentiometer and use it as variable resistance . Set it to 6K for R_C.
5. Calculate the value of C by using R,K and f_0 values in Eq.(1).

STEPS TO FOLLOW

1. Identify the leads of the given transistor and measure its h_{fe} value.
2. Connect the circuit as shown in Fig.9.1 with the components evaluated as per the design procedure.
3. Adjust the potentiometer R_C such that the oscillations are just sustained. Observe the output waveform on CRO screen and measure its amplitude.
4. Measure the output frequency and compare with the theoretical values given by Eq.(1).
5. Enter the readings and results in Table.9.1.

Table.9.1.

Output voltage	Theoretical value	Practical values	
	Frequency	Time period	Frequency

CALCULATIONS

Ex: (i) Let $h_{fe} = 100$ (measured with multimeterr having h_{fe} or β measurement facility);

$h_{ie} = 2.0K\Omega$ (from data sheets);

Let $R = 2.2K\Omega$; Hence $R^1 = 200\ \Omega$

$K=2.7$; $R_C=KR = 2.7 \times 2.2K\Omega = 6K\Omega$

Let $f_0 = 800Hz$. Hence $C = \frac{1}{2\pi f_0 R} \cdot \frac{1}{(6+4K)^{1/2}} = 0.022\ \mu F.$

(ii) Let $R = 2.2K\Omega$; Hence $R^1 = 200\ \Omega$

$K=2.7$; $R_C=KR = 2.7 \times 2.2K\Omega = 6K\Omega$

Let $f_0 = 1000$Hz. Hence $C = \frac{1}{2\pi f_0 R}.\frac{1}{(6+4K)^{1/2}} = 0.0178\ \mu F \approx 0.02\ \mu F$

RESULT

A phase shift oscillator is designed and the frequency of generated output is estimated and compared with the theoretical frequency. The agreement between observed and calculated values is satisfactory.

VIVA QUESTIONS

1. What is the difference between LC and RC oscillators?
2. What do you mean by positive feedback and where it is used?
3. State the Barkhausen criterion for oscillations.
4. How a transistor produces a phase shift of 180^0 between input and output?
5. How the RC-phase shift network produces a phase shift of 180^0?
6. How a single RC combination produces a phase shift of 60^0?

Suggestions:

Resistors come with 10% tolerance. That is a resistor labeled 1000 Ω may have any value between 900 to 1100Ω. As the experiment demands identical values for R and C, measure the resistors and capacitors with DMM and see that all the resistors in R-C phase shift network have same value and all capacitances have the same prescribed or calculated value.

2. The circuit gives output immediately on switching on the power supply. If it doesn't work, check whether V_{BE} is about 0.6V DC and V_{CE} is about $V_{CC}/2$(between 4 to 8V DC). If these two checks are O.K., the problem may be in feedback path. Detach feedback path by removing wire that comes from collector to point A, shown in Fig.9.1. The resulting circuit is an R-C Coupled amplifier. Inject a signal at A using a Sine wave generator at the expected oscillator frequency with amplitude of about 30mV. You will find amplified Sine wave as output. The output signal amplitude increases as you change injector position from A to B and D. If the output is as expected, the circuit is working as R-C coupled amplifier. (Otherwise follow the suggestions given for R-C coupled amplifier and see that it works). Restore the connection between A and the Collector. Now the oscillator normally works. If not, remove the feedback path again and see whether the input waveform and output waveform commence at the same point when they are superposed. If

you observe a phase shift between the two, adjust the variable resistance R^1 until the phase shift is zero. Remove signal injector and restore feedback path. The circuit works. If the circuit doesn't work, replace the transistor with higher h_{fe} value. The circuit works. Sometimes as you change different C or R values in Phase shift network, this problem comes. In such cases, changing the R_C value or changing the V_{CC} around the set value will solve the problem.

3. An R.C. Phase shift oscillator gives pure Sine wave output at a single frequency, you can assemble your own test signal generator at a fixed audio frequency. This will be useful in servicing audio sections of Transistor radio receivers and T.V. sets. You can use this as a signal source for clipper and clamper experiment. You have already noted the need for signal generator in testing the circuit. A good R-C Phase shift oscillator suitably mounted in a cabinet can be used as a good signal injector.

10. COLPITT'S OSCILLATOR

AIM OF THE EXPERIMENT

To design a Colpitt's oscillator and to estimate the frequency of generated sine wave output.

EQUIPMENT AND COMPONENTS

DCRPS – 1; CRO -1; Bread board- 1; Electrolytic capacitors – 3 (10μF/63V-2; 50μF/63V-1); Transistor – 1(BF 194); Resistors - 4 (1KΩ,1/2W →1; 2.5KΩ,1/2W →1; 8.2KΩ,1/2W →1; 33KΩ,1/2W →1), Non-electrolytic capacitors -2 (To be selected after design); Inductor (Decade Inductance Box or DIB)-1.

THEORY

Oscillator may be defined as an electronic circuit that converts energy from a DC source into a periodically varying electrical output. It is usually an amplifier with excessive regenerative feedback. Amplifiers with excessive regenerative feedback produce oscillations at a frequency that satisfies Barkhausen's criterion. The operating frequency is decided by the frequency for which the feedback signal is in phase with input signal. Oscillators do not need external input signal. The oscillating frequency is selected by the frequency selective network from the noise present in the circuit. If the amplifier (that result when feedback path is removed) produces 180^0 phase shift , the frequency selective network between output and input is designed to produce an additional phase shift of 180^0 to makeup the total phase shift between input and output to 360^0. For amplifiers that produce in phase output, the frequency selective network produces zero or 360^0 phase shift.

Oscillators can produce either sinusoidal or non-sinusoidal waveforms. Oscillators which produce sine waves are called *Sinusoidal Oscillators* Ex: Wien bridge, Phase shift, Colpitt's and Hartley oscillators. The two types of LC oscillators are Colpitt's and Hartley oscillators. These belong to LC oscillator's family because their frequency determining circuit consists of inductor and capacitor as the elements.

An oscillator generally consists of an active device like transistor, feedback circuit, biasing circuit and an energy source (voltage source). Colpitt's oscillator is a high frequency oscillator which utilizes an LC-parallel circuit as the feedback circuit or frequency determining circuit. The transistor when used in CE configuration

produces a phase shift of 180^0 and an additional phase shift of 180^0 is provided by the LC-parallel circuit (Tank circuit). So a total phase shift of 360^0 is achieved around the loop. This is the condition for sustained oscillations. The frequency of oscillations is given by

$$f = \frac{1}{2\Pi\sqrt{LC_{eq}}} \quad \text{where } C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

DESIGN EQUATIONS

Feedback factor $\beta = \frac{C_2}{C_1}$; Voltage gain $A_{V(MIN)} = \frac{1}{\beta} = \frac{C_1}{C_2}$

Frequency of output waveform $= f = \frac{1}{2\Pi\sqrt{LC_{eq}}}$; $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$

Let $C_1 = 0.22\mu F$; $C_2 = 0.022\mu F$. Frequency generated to be nearly 50 KHz. To estimate the value of L, use the following equation

$$C_{eq} = \frac{0.22 \times 0.022}{0.242} = 0.02\mu F$$

$$L = \frac{1}{4\Pi^2 f^2 C_{eq}} = \frac{1}{4 \times 3.142^2 \times 25 \times 10^8 \times 4 \times 10^{-8}} = 3.949mH$$

Commercially available 4mH choke can be selected.

$$A_{V(\min)} = \frac{0.22}{0.022} = 10$$

As A_{Vmin} is related to the parameter h_{fe} of the transistor we have to select a transistor whose h_{fe} is greater than by 10 times the A_{Vmin}. A transistor whose h_{fe} greater than 100 can be used. In DMMs h_{fe} is referred to as β. Some text books also use this notation. One should not get confused with feedback ratio, as this is also referred to as β.

Input resistance of transistor circuit is assumed to be much larger than the reactance of C_1 at the oscillator frequency. So C_1 is the capacitance that lies in the input side and its value will be $A_{v(min)}$ times C_2. At high frequencies, stray and wiring capacitance have to be taken into account. So amplifier voltage gain must be much larger than $A_{V(min)}$.

CIRCUIT DIAGRAM

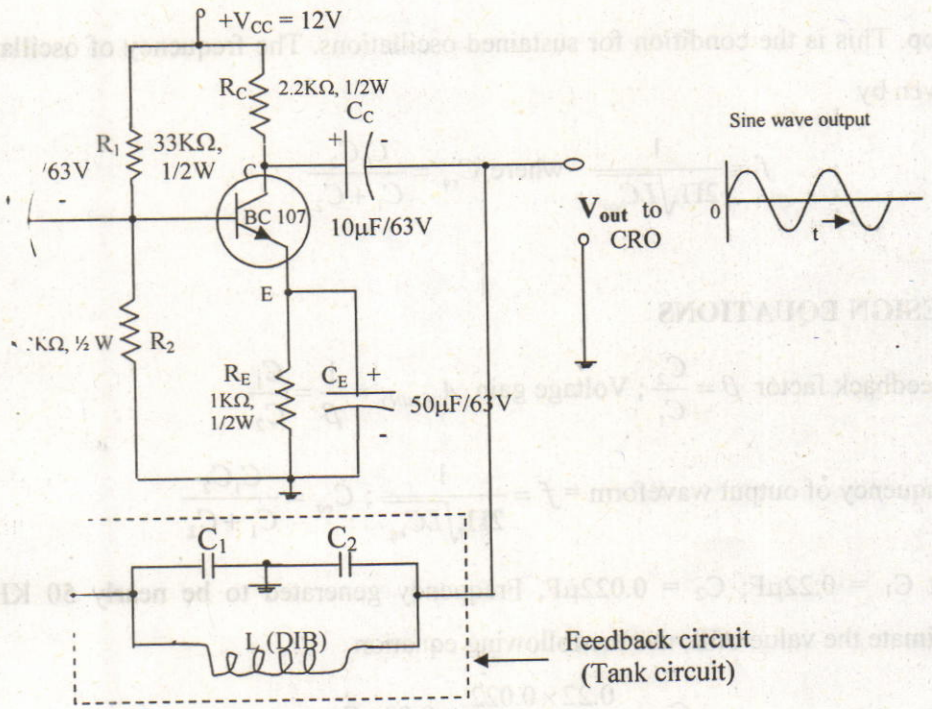


Fig.10.8

STEPS TO FOLLOW

1. Identify the given components (resistors, capacitors, transistor)
2. Check the given transistor for its correctness using a multimeter possessing β measurement facility.
3. Calculate the value of inductance for a given value of frequency at a fixed capacitor pair of C_1 and C_2.
4. Connect the circuit as shown in Fig.10.1 along with designed components to generate a sine wave of specified frequency.
5. Switch on the DCRPS and apply a d.c potential of 12V to the circuit.
6. Connect a CRO at the output terminals and measure the wavelength. Also estimate the time period and frequency of the sine wave output.
7. Similarly introduce other sets of components (inductors, capacitors) and repeat the above step (step 6).
8. Enter the readings into the table 10.1 and compare the theoretical and experimental values of frequency.

Table 10.1

S.No.	C_1	C_2	L	Time period	Frequency	
					Theoretical	Experimental
1						
2						
3						

RESULT

A Colpitt's oscillator was designed and the frequency of generated output was estimated and compared with measured value. The agreement between observed and calculated values is satisfactory.

VIVA QUESTIONS

1. What is an oscillator?
2. What are the various functioning blocks in an oscillator?
3. State Barkhausen criterion for oscillation.
4. How total phase shift of 360^0 is obtained in the Colpitt's oscillator?
5. Why is it necessary to take two capacitances in the tank circuit? What happens if C_2 is replaced by an inductance?
6. What happens if C_1 is less than C_2.
7. If C_1 and C_2 are equal, is it possible to get oscillations. ?

Suggestions:

1. When a decade inductance box or resistance box are given, measure the values for each setting. Resistors and inductances might have been burnt by earlier experimenters. Don't take face readings of the boxes, measure the parameter of interest with an LCR meter.
2. Designing Colpitt's oscillator for low frequencies (below 50 KHz) is not advisable. When high inductance chokes are used, the iron core due to hysterisis effect distorts shape of the signal. The coils have significant resistance also. Air core or high quality ferrite chokes are preferable. Instead of general purpose transistor, you may use radio frequency transistors like BF194

3. Ugly connections with unnecessarily long wires introduce unwanted feedback. Use wires as short as possible to make connections avoiding output leads falling on input side. At high frequencies, physical connection is not necessary for unwanted feedback.
4. Capacitances in tank circuit may carry very high voltage than supply voltage. If you are asked to dismantle the circuit immediately after switching off, first discharge the capacitors and then touch them.
5. If you are not getting a pure sine wave, adjust the supply voltage V_{CC} by 2 or 3V on either side.
6. If you use a power transistor like SL100 and if the oscillator frequency is more than 500 KHz you can use a wave meter to measure the frequency of oscillator. If a wave meter is available in your lab, learn how to use it to measure frequency.
7. Repeat the experiment with C_1 and C_2 positions interchanged. See if you can make the circuit oscillate with changes in circuit components.
8. Repeat the experiment with $C_1 = C_2$.
9. A Colpitt's oscillator with an air gang capacitor (Two capacitors whose capacitance can be varied simultaneously) used for C_1 and C_2 will help to change the frequency in a given range, decided by the LC circuit. To change frequency range, you can use another coil. Observe the frequency changing mechanism, provided in a 3 band radio receiver set. A variable frequency Colpitt's oscillator mounted in a shielded cabinet can be used to test the working of I.F. and R.F stages in Radio receiver and T.V. Receiver sets.

11. ASTABLE MULTIVIBRATOR

AIM OF THE EXPERIMENT

To design a free running multivibrator and to determine the frequency of generated square wave output.

EQUIPMENT AND COMPONENTS

DCRPS -1, CRO – 1, Transistors-2 (BC 107); Polyester/Ceramic disc capacitors – 2 (0.01μF); Resistors – 4 (taken after design).

THEORY

The oscillator which generate waveforms, other than sine wave forms are called Non-sinusoidal or Relaxation oscillators. Non-sinusoidal waveforms may be square wave, rectangular wave, sawtooth wave, pulse etc. It is defined as a circuit in which voltage or current change abruptly from one value to another and which continues to oscillate between these two values as long as dc power is supplied to it. These can be classified as Astable, Monostable, and Bistable Multivibrators. The term *multivibrator* is derived from the fact that a square wave actually consists of large number of sinusoidal waves of each of different frequency.

Multivibrator is an electronic circuit which can generates non – sinusoidal waveforms. It is basically a two-stage resistance coupled amplifiers with positive feedback from the output of one amplifier to the input of the other. The feedback is supplied in such a manner that one transistor is driven to saturation and the other to cut-off. It is followed by new set of conditions in which the saturated transistor is driven to cut-off and the cut-off transistor is to driven to saturation. Thus multivibrators are based on switching characteristics of the transistor and the time required to switch from one state to the other. Depending upon the type of coupling and the stability of operating states, the multivibrators are classified as : (i) Astable or free running (ii) Monostable or one-shot and (iii) Bi-stable or Flip-flop multivibrator.

Astable Multivibrator: *A multivibrator which generates square waves on its own is known as an Astable or Free Running Multivibrator.*

The astable multivibrator has no stable state. It switches automatically between the two states (ON and OFF) and remains in each for a time dependent upon the circuit constants. It is an oscillator since it requires no external pulse for its operation.

Monostable Multivibrator: A multivibrator in which one transistor is always conducting (i.e. is in ON state) and the other is non-conducting (i.e. in the OFF state) is called Monostable multivibrator. A Monostable multivibrator has only one state stable. This means that if one transistor is conducting and the other is non conducting, the circuit will remain in this position. With the application of external pulse, the circuit will interchange the states. However, after a certain time, the circuit will automatically switch back to the original state and remains there until another pulse is applied. Thus a mono stable multivibrator can not generate square waves on its own.

Bistable Multivibrator: A multivibrator which has both states stable is called a Bistable Multivibrator. It can stay in one of its two states indefinitely; (as long as power is supplied) changing to other state only when it receives a trigger pulse from outside. When it receives another triggering pulse, then it goes back to its original state. The Bistable Multivibrator is also known as *Flip-Flop* circuit. Multivibrators are used : as a frequency divider ; as sawtooth generator; as square wave and pulse generators; as memory elements in computers ; as standard frequency sources and for use in TV and RADAR circuits.

CIRCUIT DIAGRAM OF ASTABLE MULTIVIBRATOR

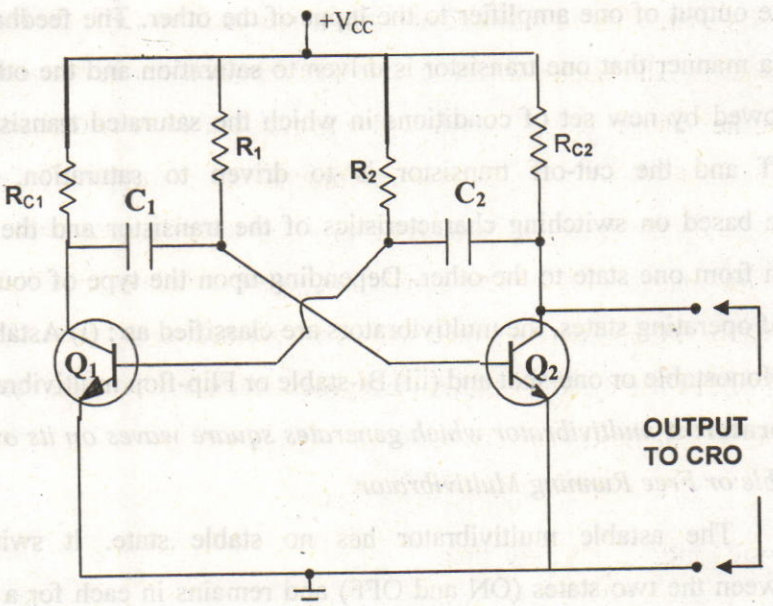


Fig.11.1

OUTPUT WAVEFORM

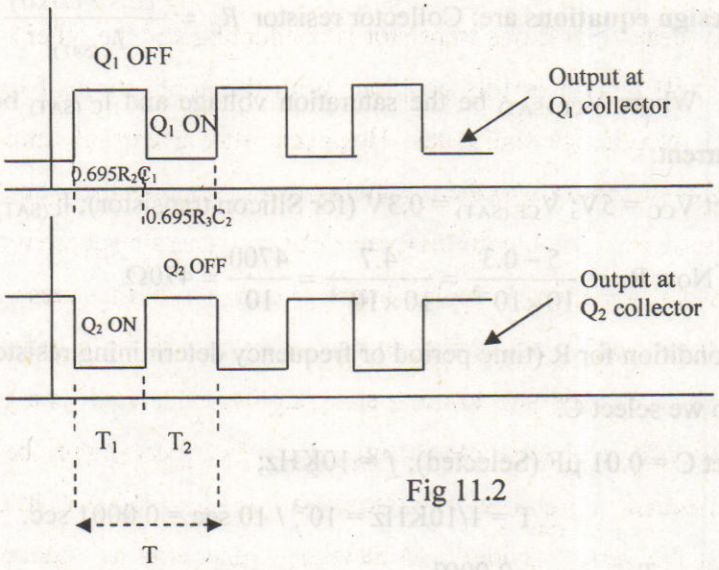


Fig 11.2

Working:

This circuit will generate square wave output provided $h_{FE} > \frac{R_1}{R_{C1}}$ or $\frac{R_2}{R_{C2}}$

Suppose at time t, Q_1 has just switched from OFF to ON.; the voltage V_{C1} falls from V_{CC} to (V_{CE}) sat. This voltage change gets transmitted through C_1 to the base of Q_2 and cuts-off Q_2. The capacitor C_1 has one of its terminals connected at the collector of Q_1 where the voltage is $(V_{CE})_{sat}$. The other terminal of C_1 is connected to the base of Q_2 which is at $-V_{CC}$. As C_1 charges through R_1 towards $+V_{CC}$ (total charging potential $2V_{CC}$) the base of Q_2 rises from $-V_{CC}$ to $+V_{CC}$. As soon as it becomes positive and reaches $(V_{BE})_{sat}$, the transistor Q_2 gets switched ON. The potential V_{C2} then drops to $(VCE)_{sat}$ and negative step is transmitted to the base of Q_1 through C_2 turning Q_1 OFF. The cycle continues fiving oscillations as shown in Fig.11.2.

Total time period of the square wave is

$$T = T_1 + T_2 = 0.695(R_1 C_1 + R_2 C_2)$$

If $R_1 = R_2 = R$; $C_1 = C_2 = C$ then

$$T = 0.695\ (RC+RC) = 1.388\ RC \text{ seconds.}$$

Frequency of the square wave $= f = \frac{1}{T} = \frac{0.7}{RC}$ Hz.

DESIGNING

Let $R_{C1} = R_{C2} = R_C$ be the collector resistor; I_C be the collector current; V_{CE} be the collector-to-emitter voltage and V_{CC} be the supply voltage.

Design equations are: Collector resistor $R_C = \dfrac{V_{CC} - V_{CE(SAT)}}{I_{C(SAT)}}$

Where $V_{CE\,(SAT)}$ be the saturation voltage and $I_{C\,(SAT)}$ be the saturation collector current.

Let $V_{CC} = 5V$; $V_{CE\,(SAT)} = 0.3V$ (for Silicon transistor); $I_{C(SAT)} = 10mA$ (given).

$$\text{Now } R_C = \frac{5-0.3}{10\times10^{-3}} = \frac{4.7}{10\times10^{-3}} = \frac{4700}{10} = 470\Omega$$

Condition for R (time period or frequency determining resistor) is $R < h_{fe}R_C$.

So we select C.

Let C = 0.01 μF (Selected); f = 10KHz;

$$\therefore T = 1/10KHz = 10^{-3} / 10 \text{ sec} = 0.0001 \text{ sec.}$$

$$R = \frac{T}{1.38C} = \frac{0.0001}{1.38\times0.01\times10^{-6}} = 7.246K\Omega$$

Finally for $V_{CC} = 5V$; $I_C = 5mA$; C= 0.01 μF; f = 10 KHz;

$R_1 = R_2 = 7.246K\Omega$; $C_1 = C_2 = 0.01$ μF; $R_{C1} = R_{C2} = 470\Omega$;

(As 7.246KΩ resistor is not available, a combination of 6.8KΩ and 470Ω resistors can be taken to achieve this value. A 10KΩ potentiometer (or trimpot) can be used to introduce the above resistance value.). A combination of capacitances connected in parallel to obtain suitable values.

In this way, one can design the components of the circuit for generating any other selected frequencies.

STEPS TO FOLLOW

1. Identify the leads of the given transistors and check them for their correctness using a multimeter possessing h_{fe} measurement facility.
2. Choose the fixed frequencies and estimate the corresponding resistance and capacitance values using the suitable formulae.
3. Connect the circuit as shown in Fig.11.1 with suitable components on a bread board.
4. Switch on the DCRPS and introduce a suitable dc voltage (say 5V) into the circuit.

5. Connect a CRO at one of the collectors of the circuit and measure the time period and hence estimate the frequency of the square wave output.
6. Replace the components (R_1 and R_2) with different sets of resistors (keeping capacitances unchanged) for generating new frequencies.
7. Replace the components (C_1 and C_2) with different sets of capacitors (keeping resistances unchanged) for generating new frequencies.
8. Enter the observations in the Table 11.1.

Table 11.1

S.No.	Frequency		Time period		Resistors	
	Theory	Practical	Theory	Practical	$R_1=R_2=R$	$C_1=C_2=C$ (in μF)
1.	1 KHz					
2.	2 KHz					
3.	4 KHz					
4.	8 KHz					
5.	10 KHz					0.01
6.	1 KHz					
7.	2 KHz					
8.	4 KHz					
9.	8 KHz					
10.	10 KHz				7.246KΩ	

RESULT

An astable multivibrator was designed and the frequency of generated output was measured using a CRO. The observed values are compared with estimated value and the agreement between observed and calculated values is satisfactory.

PRECAUTIONS

1. Apply accurately the dc voltage with the help of digital multimeter.
2. While measuring time periods/ wavelengths, display only one or two cycles of the waveform.
3. Attend all the precautions of CRO.
4. Keep the coarse and fine voltage variation knobs of the DCRPS in minimum position before and completion of the experiment.

VIVA QUESTIONS

1. What is a multivibrator? What are the uses of multivibrators?
2. What are ON and OFF states of transistor?
3. Which type of feedback is used in multivibrator?
4. What is the name of the output of multivibrator?
5. Differentiate between monostabe and bistable multivibrators.
6. If C_1 is not equal to C_2 what changes do you observe in the waveform?
7. Keeping RC product value same, if low capacitances are used what changes do you observe in the waveform?
8. Keeping RC product value same, if low resistances are used what changes do you observe in the waveform?
9. What changes do you observe in the waveform, if collector resistances used are slightly different?
10. What changes do you observe, if you increase the Vcc value by 25% over the starting value?
11. What changes do you observe, if you increase the Vcc value by 25% less than the starting value?
12. What changes do you observe, if the two transistors have different h_{fe} values?

Suggestions:

1. Design a circuit that works for 6VDC for V_{CC}. Assemble and test it with 4 pen cells. Now you have a portable multivibrator.
2. Put a Zener diode of 4.8V across each output. You have a TTL compatible Astable multi vibrator.
3. Design a circuit that works for 3VDC for V_{CC}. Assemble and test it with 2 pen cells. Now you have a portable multivibrator with cost reduced.
4. Calculate R and C values for T = 2 sec. Put one LED in series with each collector resistor with the anode at positive end. Now you have a visual display of 1sec ON and 1sec OFF periods of the transistors.
5. Design an astable multivibrator with higher V_{CC} (>12V) and use more LEDs in series with R_C instead of 1. You can arrange LEDs to represent an alphabet like "W". You have a character display. Explore how to display multiple characters like "WELCOME"?

12.ENERGY BAND GAP

AIM OF THE EXPERIMENT

To determine the forbidden energy band gap of semiconductor diode.

EQUIPMENT AND COMPONENTS

DCRPS (0–30V, 2A)-2; Heating arrangement – 1; 120^0C mercury thermometer or a PT100 probe digital thermometer -1; Micro ammeter (0-200 μA or Higher range or a digital panel meter 0-500 μA)-1; Digital multimeter -1; Test tube-1; Semiconductor diode (Germanium diode OA 79)-1.

THEORY

Materials are classified according to band theory of solids as conductors, semiconductors, and insulators. Conductors possess no forbidden energy gap (i.e., E_g = 0 eV); Semiconductors possess relatively small forbidden energy gap (i.e., $E_g \approx 1$ eV). Insulators possess large forbidden energy gap (i.e., $E_g \approx 5$ eV).

Forbidden energy gap is the difference in energy between the lower edge of the conduction band E_C and upper edge of the valence band E_V on energy level diagram. It is measured in Electron Volt (eV) unit. An electron volt is the amount of energy that would be imparted to an electron on being accelerated through a potential difference of 1V. Thus 1 eV = 1.6×10^{-19} J, Silicon possess a forbidden energy gap of 1.2 eV whereas Germanium material possess a gap of 0.7 eV. This means that an electron in valence band can become a conduction electron if an energy equal to or greater than forbidden energy gap is to be supplied. When a junction is formed between two semiconducting materials (P, N) in a diode, it allows different magnitude of currents in different directions. The current that flows in reverse direction is known as Reverse saturation current. This current is a function of temperature.

$$I(T) = KT^m e^{\frac{-V_G}{\eta V_T}}$$

where K is constant,

T is absolute temperature; qV_{Go} is forbidden energy gap in Joules.

For Ge, $m = 2$; $\eta = 1$; $V_{G0} = 0.785$V

$V_T = KT/q$ is the volt equivalent of temperature. From experimental data, it is found that the reverse saturation current approximately doubles for every 10^0C rise in temperature.

This feature or behaviour can be utilized for the estimation of forbidden energy gap using the relation

$$E_G = \frac{2000 \times K \times 2.303 \times (\log_{10} I_2 - \log_{10} I_1)}{\left(\frac{1000}{T_1} - \frac{1000}{T_2}\right)} eV$$

Where K is the Boltzman constant = 8.6 x 10^{-5} eV/ ^{0}K; I_1 and I_2 are the reverse saturation currents at temperatures T_1 and T_2 respectively (in ^{0}K).

CIRCUIT DIAGRAM

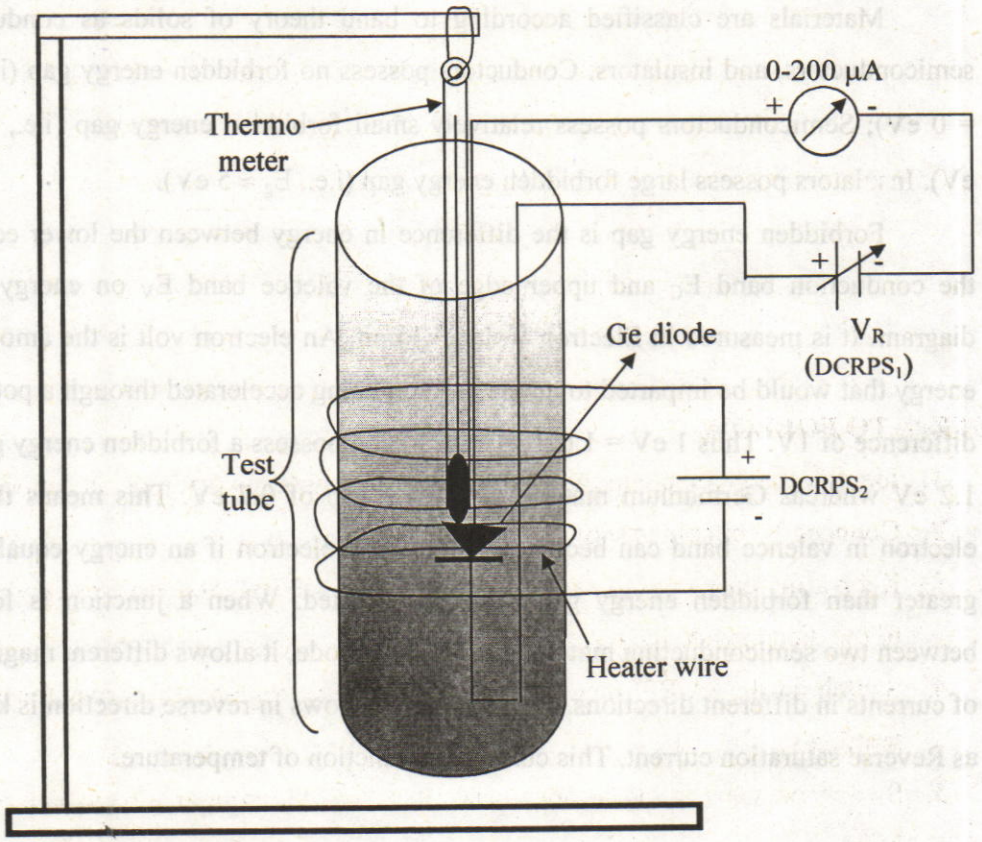


Fig.12.1

Description of the setup:

Take a 20 mm diameter test tube. Place a diode inside the test tube at the middle of its length. Wind a canthal wire of 10Ω resistance on the outside of the test tube such that the turns cover evenly on either side of the diode. The two ends of the canthal wire are connected to a 12V, 2A supply or battery. Place a digital thermometer probe or a mercury thermometer inside the test tube touching the diode.

The two ends of the diode are connected to a DC power supply such that the diode is reverse biased.

GRAPH

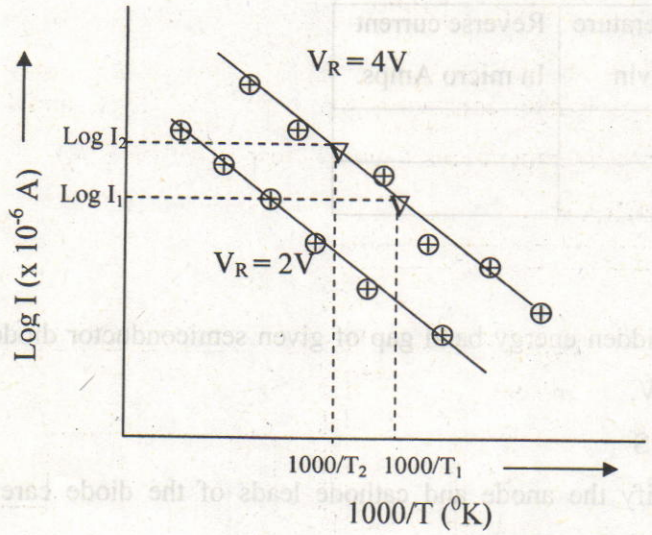


Fig.12.2

STEPS TO FOLLOW

1. Identify the given component (diode) and find its leads (cathode and anode).
2. Connect the circuit as shown in Fig.12.1.
3. Keep a mercury thermo meter or PT100 probe digital thermometer very close to the diode inside the test tube.
4. Switch on the DCRPS and maintain a reverse voltage of 2V across the diode terminals.
5. Switch on the heating arrangement and allow the temperature to rise up to 75^0C.
6. Note the reverse current when the temperature on falling reaches 75^0C.
7. Similarly note other readings at other temperatures, with a decrement of 5^0C, up to room temperature.
8. Repeat the experiment by changing the reverse voltage to 4V.
9. Enter the readings in the table 12.1.
10. Draw a graph by taking the variable 1000/T values along X-axis and the variable log I values along Y-axis.
11. Mark the observed points and join them by straight lines as shown in Fig.12.2.

12. Estimate the value of E_G from the graph by using the formula given above.

Model Table

Reverse bias Voltage : -------

Sl.No.	Temperature In Kelvin	Reverse current In micro Amps.

RESULT

The forbidden energy band gap of given semiconductor diode was estimated as E_G = ... eV.

PRECAUTIONS

1. Identify the anode and cathode leads of the diode carefully and apply reverse bias properly.
2. Do not ex e working temperature of the Germanium diode (i.e., 80^0C) while heating it.
3. Choose an appropriate range in the micro Ammeter, preferably a digital panel meter.
4. The canthal wire has to be kept in position by using insulation tape.

VIVA QUESTIONS

1. What is forbidden energy gap?
2. What are the units of forbidden energy gap?
3. What are conduction band and valence band?
4. Define electron volt.
5. What is reverse saturation current?
6. What are the values of E_G for Si and Ge?

13.VOLTAGE DOUBLER

AIM OF THE EXPERIMENT

To construct a full wave voltage doubler circuit and to study its operation.

EQUIPMENT AND COMPONENTS

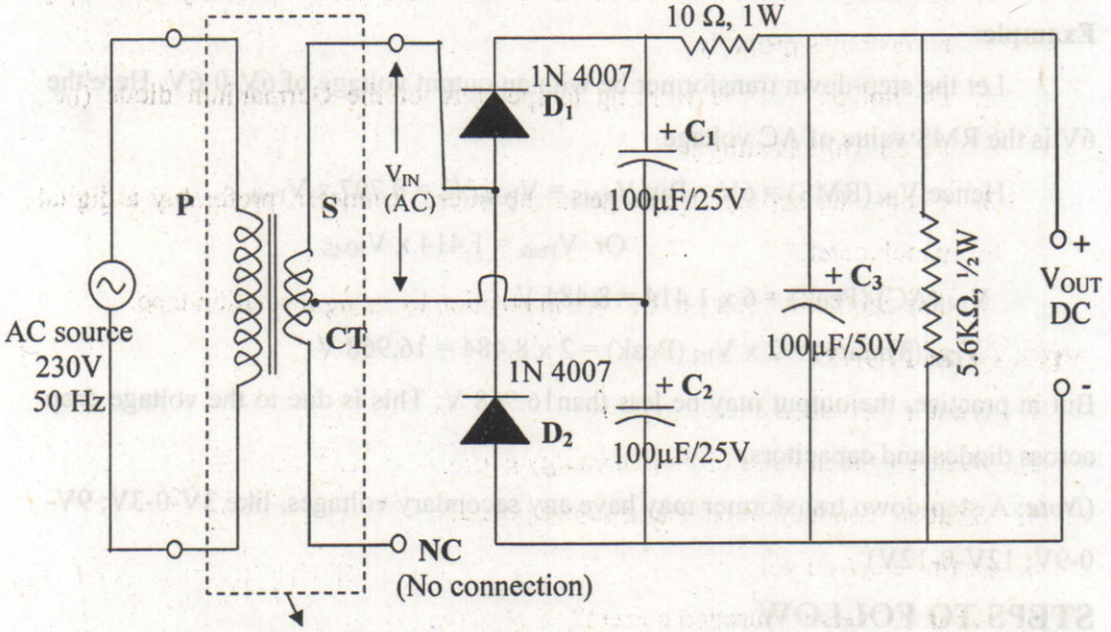
CRO-1; Ohm meter (DMM)-1; DC volt meter (0-200V)-1; AC volt meter (0-200V)-1; Step-down transformer (220V\ __V- 0-__V)-1; Bread board-1; Diodes (1N 4007) - 2; Electrolytic capacitors-3 (100μF/25V-2; 100μF/40V-1); Resistors-2 (10Ω, 1W-1; 5.6KΩ, 1/2W-1)

FORMULAE

V_{IN} (peak) = $\sqrt{2}$ x V_{IN} (RMS)

V_{OUT} (DC) 2 x V_{IN} (Peak)

CIRCUIT DIAGRAM



Step-down transformer (230V/__ V-0V-__V)

Fig.13.1

THEORY

A voltage doubling circuit (Voltage doubler) produces an output voltage which is almost equal to double the peak voltage of the input waveform. In the same way, one can imagine tripler and quadruplar. The action can be understood as follows.

The voltage doubler can utilize either one half cycle or both half cycles (+ve and –ve) of its input voltage waveform. Hence, we can have either a half wave voltage doubler or a full wave doubler. In the full wave voltage doubler circuit, shown in Fig.13.1, a centre tapped transformer is fed with an AC power to its primary coil (P). The AC output from the secondary coil (S) is applied to the diodes and capacitors as shown. During the positive half cycle of AC input, diode D_1 gets forward biased and charges the capacitor C_1. Then a DC voltage, equal to the peak value of the AC input voltage, will be developed across the capacitor C_1. Similarly, during the negative half cycle of the AC input, diode D_2 gets forward biased and charges the capacitor C_2. Then a DC voltage, equal to the peak value of the AC input voltage, will be developed across the capacitor C_2. These two peak voltages are added together giving rise to double the peak value of AC input voltage. Any ripples (AC component) that are left in the output across C_1 and C_2 combination are smoothed out or filtered by the third capacitor C_3. Thus the circuit acts as a voltage doubler.

Example:

Let the step-down transformer be with an output voltage of 6V-0-6V. Here the 6V is the RMS value of AC voltage.

Hence V_{IN} (RMS) = 6V But $V_{RMS} = V_{Peak}/\sqrt{2} = 0.707 \times V_{Peak}$

Or $V_{Peak} = 1.414 \times V_{RMS}$

V_{IN} (AC) (Peak) = $6 \times 1.414 = 8.484$ V

V_{Out} (Theory) = $2 \times V_{IN}$ (Peak) = $2 \times 8.484 = 16.968$ V

But in practice, the output may be less than16.968 V. This is due to the voltage drop across diodes and capacitors.

(***Note***: A step-down transformer may have any secondary voltages, like 3V-0-3V; 9V-0-9V; 12V-0-12V)

STEPS TO FOLLOW

1. Identify the given components like resistors, capacitors and diodes.
2. Identify the leads (anode and cathode) of the given diodes.
3. Take the given step-down transformer and connect its primary coil (P) to AC mains.
4. Using an AC voltmeter, measure the magnitude of AC voltage at the output terminals (secondary) of the same transformer and note it in the observation

table.1. Convert this value (RMS value) into its equivalent peak value and note this value as V_{IN} (Theory).

5. Now calculate the output voltage by using suitable formula and note this value as V_{OUT} (theory) .
6. Observe the AC input voltage waveform with a CRO; measure its amplitude (peak value) and note it.
7. Connect the circuit as shown in Fig.13.1 on a bread board for observing the behaviour of voltage doubler.
8. Now observe the output voltage waveform with the CRO and measure its value.
9. Repeat the above step with DC voltmeter.
10. Now disconnect the load temporarily at the output terminals of the circuit and measure the output voltage with the DC voltmeter and CRO.
11. Note the observed values in the table in the row against DC voltage (without load).

Table.13.1

S.No.	Item	With DMM	With CRO	Theory
1.	V_{IN} (AC)	[RMS value]	[peak value]	
2.	V_{OUT} (DC) (with load)			
3.	V_{OUT}(DC) (without load)			

CACULATIONS

Theoretical

V_{IN}(RMS) = ----------V (with an AC volt meter).

V_{IN}(peak)= Vin(RMS) x 1.414 = ----------V

V_{OUT} = 2 x V_{IN}(peak) = = ----------V

RESULT

A voltage doubler circuit was constructed and its operation was studied

PRECAUTIONS

1. The anode and cathode leads of given diode are to be identified properly.
2. The polarities of electrolytic capacitors are to be observed carefully before introducing into the circuit. Capacitors with working voltage rating less than that of the voltage to be doubled should not be used as they may explode. As the present circuit is not designed for commercial purpose, it is advisable to use to select capacitors with double the doubler output.
3. The connections on the primary side of the transformer are not to be touched while the power is on.
4. While observing the input waveform on one channel (A-channel) of CRO, the AC/DC coupling slide switch must be put at AC mode, while for observing the output; the AC/DC slide switch must be put at DC mode.

VIVA QUESTIONS

1. What is a voltage doubler?
2. What is a filter? Which components can act as a filter?
3. Explain about Π and L-section filters.
4. How capacitor acts as a filter?
5. How an inductor acts as a filter?
6. What is ripple? How to eliminate it?
7. What is the purpose of a step-down transformer in a voltage doubler?
8. Explain the action of voltage doubler.
9. What type of filter is used in voltage doubler circuit?
10. Why the third capacitor C_3 possess more/double DC voltage specification?
11. Why the output voltage is less than the theoretically predicted value?
12. In the voltage doubler circuit, how a diode acts?

Suggestions:

1. A voltage doubler has application in flash lights. Flash lights discharge large power for few milliseconds. The batteries used in the circuits cannot provide such

power instantaneously. So they are used to charge capacitors to higher voltages. Doubler circuits are usually designed to give large power instantaneously.

2. Doublers provide high potential difference than is available from the source. If you need a p.d of around 1400V, you can use a step-up transformer of 500-0-500V and develop a doubler circuit with capacitors of suitable working voltage. We have to keep in mind, the reverse breakdown voltage of diodes also and select such diodes that have larger reverse breakdown voltage than is generated in the doubler. One has to be careful in dealing with doubler circuit as they may give electrical shock.

14 Simulation experiments

Aim: To learn how to study the performance of a designed circuit through simulation on a computer using software based on SPICE

Apparatus: A PC with Windows XP operating system, Any of the software packages like Multisim (Suppliers :Electronic work bench) or circuit maker which uses version of SPICE or PSPICE (Popular Simulation Program with Integrated Circuit Emphasis.). Recent books on Electronics are giving details of using the software and to test the working of circuit through simulation. In the software provided by them along with provision to develop a circuit of his/her choice by the user, some standard circuits developed and ready for analysis are given. A CD is usually enclosed along with the book which contains student version of the software. We learn how to use circuit maker software package. Those who conduct practical have to procure official version of the full package.

MultiSim and Circuit maker are the two packages which are almost alike even at the command level. MultiSim package is available in CD form for those who purchase "Electronic devices and Circuits Eighth Edition by Robert L.Boylestand & Louis Nashelsky" published by M/s Prentice Hall of India. The authors gave detailed description of the software and details of how to analyze electronic circuits using computer simulation at the end of each lesson. As the syllabus of the course is covered by the book to a great extent, students are advised to go through the relevant part of the subject before conducting simulation experiments.

Circuit maker/MultiSim can model independent voltage and current sources, resistors, capacitors, inductors, transformers, transmission lines, dependent sources, BJTs, MOSFETS, JFETS and diodes.

Circuit maker/MultiSim can analyze the transient, small signal, or steady state frequency response, of a circuit. The program circuit maker includes a graphical output interface called probe and a library of devices with predetermined characteristics called parts.

Before using software, first draw the circuit you want to simulate , on a paper and note the component values, active device selected, polarities and values of voltage sources and electrolytic capacitors and signal sources. Identify and number the nodes.

Now the circuit can be drawn on computer monitor using Circuit Maker/MultiSim by following the steps given here.

Install Circuit Maker/MultiSim on to a PC. If you have installed it on your hard disk, you're ready to run the program.

1 Open the Start menu.

2 Choose Programs > Circuit Maker 6 or Circuit Maker PRO or MultiSim.

3 Choose the Circuit Maker/MultiSim program by double-clicking on the icon.

By going through the step by step procedure given in the help menu, one can very easily assemble a circuit and test it. The individual value of various components can be changed and the resulting changes in the response of the assembled circuit can be studied.

In MultiSim a PDF file "Getting started" is given with almost every detail in using the Package. Following installation procedure the software has to be installed. Then you can go through other details. Clear illustrations for each step are provided for self study. After installation open MultiSim . You will get a circuit window.

Select circuit maker/MultiSim by a double click of the mouse on the icon of circuit maker. The authors used circuit Maker software. So here after you will find reference to **circuit maker** A device selection dialog box opens.

Using the Device Selection Dialog Box

On the top row of the device selection dialog box you see various functions the software can perform.. As in M. S. Office software you see **File, Edit, Options, view, simulation, window, devices, and help** in a row.

Selecting the **File** option shows various sub options available. open a **new** file, **open** an existing file option to **reopen** a file, **save** a file, **save as** another file , **revert, import, export, print set up, print circuit, print wave forms.**. For Window O.S. Users most of the operations mentioned are well known. You can open a new untitled file by clicking the mouse on **New** file button.

In the second row of the main screen a tool bar appears with various icons. By clicking on any one of the items you can do specified functions. The various functions you can do are

1) New : Open a new file

2) Open : Open an existing file

3) Save : Save the created file.

4) Print : Print the current file

5) Arrow : Tool to select, move and edit devices, wires and text.

6) Wire : Tool to connect circuit,

7) Text : Tool to add text to the circuit,

8) Delete : Tool to delete devices, wires and text.

9) Zoom : Tool to reduce and magnify circuit.

10) Rotate : To rotate 90^0 the components or object.

11) Mirror: To produce a component which is a mirror image of the given component.

12) Digital analog simulation mode: To select one of the modes: analog or digital; If digital is selected, logic gate symbol is displayed. If analog mode is selected, a transistor symbol is displayed.

13) Reset

14) Step (single step)

15) Run/Stop

16) Probe: Tool to indicate digital states of gates and plot analog data

17) Trace : Used in digital simulation to indicate the logic states of all nodes

18) Wave form: To show digital wave form and analog plot windows

19) Parts : To display and select devices

20) Search : To search a device by name, number and description.

21) Macro : To create a macro

22) ? (Help) : To display information on devices and wires,

23) PCB: To run traxmaker.

When one of the above buttons is selected, meaning and use are displayed on the top of the screen. One can easily follow them.

Drawing a schematic is as easy as pointing and clicking with the mouse. Let's walk through a simple example by constructing the circuit shown in Figure .1.

STEPS TO USE THE SOFTWARE

Suppose we want assemble the circuit given in Fig 1.

We assume Circuit maker is opened and various icons mentioned above are displayed.

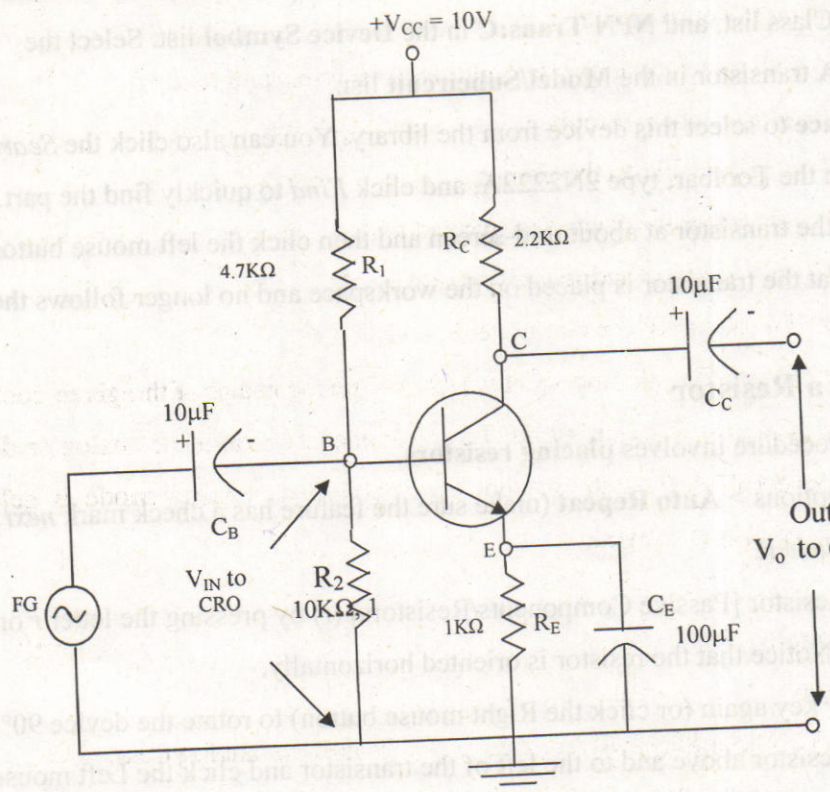


Fig.1.1 RC-coupled amplifier

1 Begin by clicking the **New** button on the Toolbar.

A blank workspace appears with device selection dialog box .Twenty three icons appear on the top row. Each icon stands for an option and various sub options.

2 Choose **Devices > Browse** or click the **Parts** button on the Toolbar to display the various devices available in the library. The location of a device in the library is indicated by its major and minor class and its default Hot Key (if applicable) using this format:

[major device class/minor device class] (default Hot Key)

For example, a battery is found at [Analog/Power] (b). You can also find devices through hot keys in the **Devices > Hot Keys1** and **Hot Keys2** menus. By simply pressing a Hot Key (for example, the letter "b" for battery), you can quickly select and insert a device into the workspace.

Selecting a Transistor

Begin the circuit by selecting the 2N2222A transistor **[Active Components/BJTs].**

1.Select **Active Components** in the **Major Device** Class list, **BJTs** in the **Minor Device** Class list, and **NPN Trans:C** in the **Device Symbol** list. Select the **2N2222A** transistor in the **Model/Subcircuit** list.

2.Click **Place** to select this device from the library. You can also click the *Search* button on the Toolbar, type 2N2222A, and click *Find* to quickly find the part.

3.Position the transistor at about mid-screen and then click the left mouse button once. Notice that the transistor is placed on the workspace and no longer follows the mouse

Selecting a Resistor

The next procedure involves **placing resistors.**

1 Choose Options > **Auto Repeat** (make sure the feature has a check mark *next* to it) or press *Ctrl+R.*

2 Select a Resistor [Passive Components/Resistors] (r) by pressing the letter *r* on the keyboard. Notice that the resistor is oriented horizontally.

3 Press the *r* key again (or click the Right mouse button) to rotate the device 90°.

4 Drag the resistor above and to the left of the transistor and click the Left mouse button once.This will be resistor R1. Don't worry about the value yet. Since you enabled the *Repeat On* feature, another resistor will appear with the same orientation as the previous one.

5. Place the next resistor directly above the transistor. This will be resistor RC.

6.Another resistor appears. Fix it as shown in circuit 1 for RE. Likewise fix R2. When fixing the resistors is over, press any key on the keyboard (except R or M) to delete it.

7.Choose Options > **Auto Repeat** and uncheck the Auto Repeat feature or press Ctrl + R.

Selecting a Capacitor

The procedure is just like selecting resistors.. Fix the capacitors following polarity.

Selecting +V and Ground Devices

Now you'll ***place a voltage source*** and change its settings.

1.Select a **+V [Analog/Power] (1)** by pressing the 1 (number one) key. Place it above resistor RC.

2.Select a **Ground [Analog/Power]** (0) by pressing the 0 (zero) key. Place it below the

transistor.

3.Double-click **the +V device** using the Left mouse button to open **the Edit Device Data** dialog box, pictured in Figure 3.3 in the user manual.

4.Change the **Label-Value field** to read +10V.

5 Click once on the *Visible* check box next to the Label-Value field to change the black check mark to a grayed-out check mark. This causes +10V to replace the +V on the schematic.

6 Enter Vcc in the Designation field and click once in the Visible check box next to it so that there is a black check mark in it. Click OK.

Selecting sinusoidal ac source:

Sinusoidal voltage source is listed in the **source.slb** library as **VSIN.** Once placed on the diagram, double-clicking the symbol will result in the Part Name: **VSIN** dialog box with a list of options. Each choice can be made by double-clicking the desired quantity, which will then appear in the Name and value rectangles at the top of the box. The cursor appears in the value box, and the desired value can be entered. After each entry, be sure to save **Attr** to save the entered attribute. If done properly, the assigned value will appear in the listing. For our analysis the following choices will be made.

VAMPL = 1mV (the peak value of sinusoidal signal).

FREQ = 10kHz (the frequency of interest).

PHASE = 0 (no initial phase angle for the sinusoidal signal)

VOFF = 0(no dc offset voltage for the sinusoidal signal)

AC = 1mV

Changing Resistor/Transistor Label-Values

Now try the same editing procedure on the transistor and resistors.

1 Double-click resistor R1.

2 Change the Label-Value field to read 4.7k, enter R1 in the Designation field, make it visible and click OK.

3. Following step2 change the value and labels of other resistors.

4. Change the values and labels of capacitors also

5.Double-click the transistor to display the Model Selection dialog box. Since you have already selected the model that you want to display (2N2222A), just click on

the *Netlist* button to open the Edit Device Data dialog box.

6 Enter Q1 in the Designation field and make it visible. Click OK, and then click ***Exit*** to return to the schematic.

7 If necessary, drag the devices and labels around with the mouse to place them in convenient locations.

Wiring the Circuit Together

Now it's time to hook up these devices into a working circuit by wiring them together.

1 Select the **Wire** Tool from the Toolbar (or use the Arrow Tool if the **Arrow/Wire** option is enabled).

2 Place the cursor on the emitter pin (the pin with the arrow) of the transistor. When the cursor gets close to the pin, a small rectangle appears.

3 Click and hold the left mouse button, then drag the wire to the pin of the Ground symbol.

4 Release the mouse button to make the connection.

If **Options > Show Pin Dots** is enabled, a small dot will be placed at each connection point to verify the connection (see circuit example on the following page).

5 Place the cursor on the bottom pin of R_C, and then click and hold the mouse button to start a new wire.

6 Drag the end of the wire to the collector pin of the transistor and release the mouse button.

7 Connect a wire from the top pin of R_C to Vcc.

8 Connect another wire from the bottom pin of R_1 to the base of the transistor.

9 Following the method suggested in above steps wire other components also.

You can move device and wire positions by dragging them with the mouse.

After wiring the circuit, view points may be inserted to display voltages of interest. Choosing the **Setup Analysis** icon will result in the **Analysis Setup dialog box,** in which the **ac sweep** will result in an **AC sweep and noise analysis dialog box, in** which **linear** is chosen along with **total pts:1, Start Freq; 10kHz, and end Freq:10kHz.** The result will be an analysis at only one frequency. Our initial interest will be in the magnitude of the of the quantities and not their shape or appearance.. Therefore, we should turn to analysis-Probe Set-up and choose **DO not auto-run Probe** to save time getting to the desired results. Clicking the **Analysis** icon will show

dialog box that will indicate **AC Analysis** is finished. With in this box if we choose **File** followed **Examine Output,** we will obtain a lengthy listing of input output data on the analyzed network.

A plot of the output waveform can be obtained using the **probe** option.. The sequence **Analysis-Probe-Setup** automatically run **Probe** after **simulation-OK** will result in a MicroSim Probe screen when the analysis icon is chosen. The horizontal scale is set by the sequence **Analysis-Setup-Transient** with the **ac sweep disabled-Transient** with the ac sweep. Clicking the transient option will result in a **Transient** dialog box, in which a number of choices have to be made based on the waveform to be viewed. The period of the applied signal is of 10kHz is 0.1ms =100μs. The **Print setup** option refers to the time interval between printing or plotting of the results of transient analysis. For our example we will choose 1μs to provide 100 plot points per cycle. The **Final time** is the last instant the network's response will be determined. Our choice is 500μs or 0.5ms to provide 5 full cycles of the waveform.

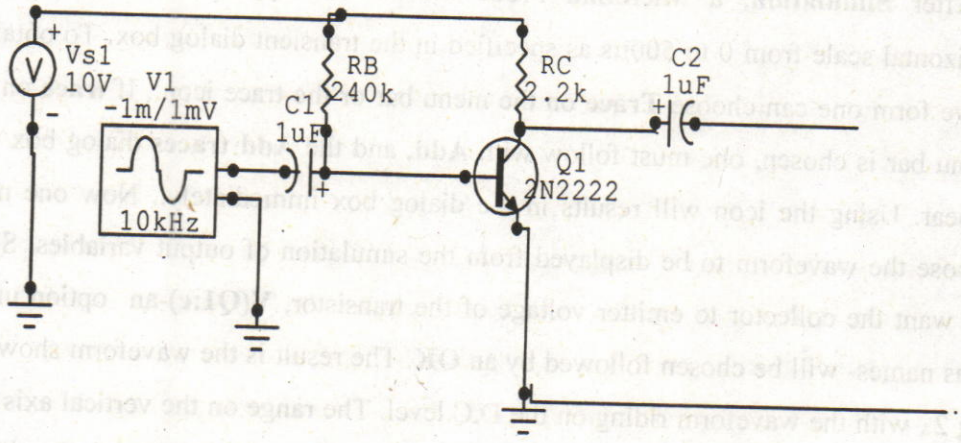
The **No-Print Delay** was taken as 0 since all the capacitors are are essentially short circuits at 10kHz.. The last choice of **Step Ceiling** sets a maximum time period between response calculations for the system, which we will set at 1μs.

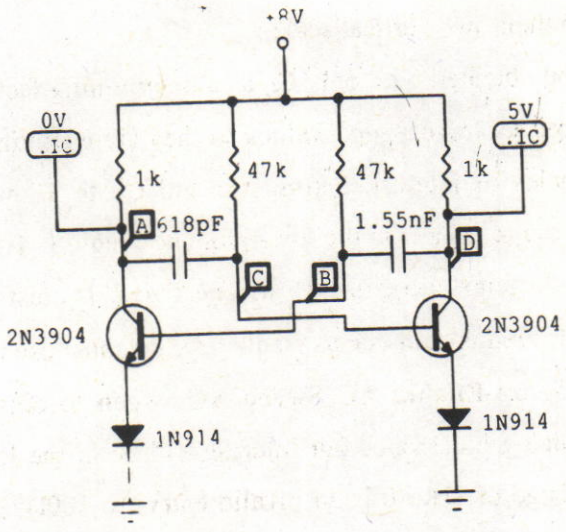
After **Simulation**, a MicroSim Probe screen will appear showing only the horizontal scale from 0 to 500μs as specified in the transient dialog box. To obtain a wave form one can choose **Trace** on the menu bar or the trace icon.. If **trace** on the menu bar is chosen, one must follow with **Add,** and the **Add traces** dialog box will appear. Using the icon will results in the dialog box immediately.. Now one must choose the waveform to be displayed from the simulation of output variables. Since we want the collector to emitter voltage of the transistor, **V(Q1:c)**-an option under alias names- will be chosen followed by an **OK**. The result is the waveform shown in Fig 2., with the waveform riding on the D.C.level. The range on the vertical axis will be chosen automatically by the computer. Five full cycles of the data will be displayed with 100 data points for each cycle. If you would like to see the data points, simply turn to **Tools-Options-Probe Options** and choose, **Mark data points. Click OK** , and the data points will appear.

If a comparison is to be made between the input and output voltages on the same graph, the Add Y axis option under plot can be chosen.. After it is triggered, choose

the Add trace icon and select V(Vs:+). The result is that both the wave forms will appear on the same screen, each with their own vertical scale.

A gain versus frequency ploy\t can be obtained with only C_B as a determining factor. The other capacitors C_E and C_C will be set to very high values so they are essentially short circuits at any of the frequencies of interest. Setting Cc and Ce to 1F will remove any effect they will have on the response on the low-frequency region.. Here one must be careful as the program does not recognize 1F as one Farad. It must be entered as 1E6μF. Since the pattern desired is gain versus frequency, we must use the sequence **Analysis-Setup-Analysis Setup-Enable AC Sweep-AC sweep** to obtain the **AC Sweep and noise analysis** dialog box. Since our interest will be in the low frequency range,, we will choose a range of 1Hz (0 is an invalid entry) to 100Hz. If you want a frequency range starting close to 0Hz, you have to select a frequency such as 0.001Hz. The **total pts:** will be set at 1000 for a good continuous plot. the **Start Freq.**: at 1Hz and the **End Freq.**: at 100Hz. The AC sweep will be left on linear. A simulation followed by **Trace-Add**-v(RL:1) will r4esult in the desired plot. Two model circuits are provided below for student's guidance. They may assemble these circuits for practice and proceed further.




+8V
0V
.IC
5V
.IC
1k
47k
47k
1k
A
618pF
1.55nF
D
C
B
2N3904
2N3904
1N914
1N914

(కత్తిరించి పంపవలెను)

అధ్యాపకుల, విద్యార్థుల సలహాలు, సూచనలు :

అధ్యాపకులు, విద్యార్థులు ఈ స్టడీ మెటీరియల్‌కు సంబంధించిన సలహాలు, సూచనలు, ముద్రణ దోషాలు తెలియపరచినచో, పునర్ముద్రణలో తగు చర్యలు తీసుకొనగలము. తెలియపరచవలసిన చిరునామా : **డిప్యూటీ డైరెక్టర్, దూరవిద్యా కేంద్రం, ఆచార్య నాగార్జున విశ్వవిద్యాలయం, నాగార్జున నగర్ - 522 510.**

Course	Year	Paper No. &Title
B.Sc., Electronics	2nd Year	Paper - II : Electronic Devices & Circuits

(కత్తిరించి పంపవలెను)

(కత్తిరించి పంపవలెను)

(కత్తిరించి పంపవలెను)