SOLID STATE ELECTRONIC CIRCUITS AND DIGITAL ELECTRONICS

B.Sc., Electronics III year - Paper - III

Lesson writers

Prof. M. Rangacharyulu
Professor in Physics (Retired)
Acharya Nagarjuna University
Nagarjuna Nagar – 522510

Dr.A.Radha Krishna Murthy
M.Sc., M.Phil, Ph.D.
Lecturer in Physics
Chalapathi Institute of Engineering & Technology
Chalapathi Nagar, LAM-522 034

Dr.J.Sivarama Krishna, M.Sc., Ph.D.
Assistant Professor in Physics
Acharya Nagarjuna University PG Centre
NUZVID, Krishna Dt.

Sri. V. Radha Krishna, M.Sc., M.Phil.,
Lecturer, Department of Physics
SKBR Collge
Amalapuram, E.G. District

Sri. S.V.Kumara Sastry, M.Sc., M.Phil
Lecturer, Department of Physics
SKBR Collge, Amalapuram - E.G. District

Associate Editor
Dr.A.Radha Krishna Murthy, M.Sc., M.Phil, Ph.D.
Lecturer in Physics
Chalapathi Institute of Engineering & Technology
Chalapathi Nagar, LAM-522 034

Editor
Prof. M. Rangacharyulu, M.Sc., Ph.D.
Professor in Physics (Retired)
Acharya Nagarjuna University

Academic Coordinator
Prof. S. Srechari Sastry, M.Sc., M.Phil, Ph.D.
Professor in Physics
Acharya Nagarjuna University

Director
Dr. Nagaraju Battu
MBA, MHRM, LLM, M.Sc. (Psy), MA(Soc.)., M.Ed., M.Phil., Ph.D.
Dept. of HRM

CENTRE FOR DISTANCE EDUCATION
Acharya Nagarjuna University
Nagarjuna Nagar – 522510
Ph: 0863 - 2293299. (08645) 211023. 211024 Cell: 9848285518
e-mail: anucde@yahoo.com
Web site: www.nagarjunauniversity.ac.in

B.sc., 3rd Year : Electronics, Paper - III

First Edition : 2009

New Impressions : 2021

No. of Copies : 318

Published by :
Dr. Nagaraju Battu,
Director,
Centre for Distance Education,
Acharya Nagarjuna University

Printed at :
M/s Sri Sainadh Printers,
Vijayawada

FOREWORD

Since its establishment in 1976, Acharya Nagarjuna University has been forging ahead in the path of progress and dynamism, offering a variety of courses and research contributions. I am extremely happy that by gaining a B++ (80-85) grade from the NAAC in the year 2003, the Acharya Nagarjuna University is offering educational opportunities at the UG, PG levels apart from research degrees to students from over 285 affiliated colleges spread over the three districts of Guntur, Krishna and Prakasam.

The University has also started the Centre for Distance Education with the aim to bring higher education within reach of all. The centre will be a great help to those who cannot join in colleges, those who cannot afford the exorbitant fees as regular students, and even housewives desirous of pursuing higher studies. With the goal of brining education to the doorstep of all such people, Acharya Nagarjuna University has started offering B.A., and B.Com courses at the Degree level and M.A., M.Com., M.Sc., M.B.A., and L.L.M., courses at the PG level from the academic year 2003-2004 onwards.

To facilitate easier understanding by students studying through the distance mode, these self-instruction materials have been prepared by eminent and experienced teachers. The lessons have been drafted with great care and expertise in the stipulated time by these teachers. Constructive ideas and scholarly suggestions are welcome from students and teachers involved respectively. Such ideas will be incorporated for the greater efficacy of this distance mode of education. For clarification of doubts and feedback, weekly classes and contact classes will be arranged at the UG and PG levels respectively.

It is my aim that students getting higher education through the centre for Distance Education should improve their qualification, have better employment opportunities and in turn facilitate the country's progress. It is my fond desire that in the years to come, the Centre for Distance Education will go from strength to strength in the form of new courses and by catering to larger number of people. My congratulations to all the Directors, Academic Coordinators, Editors and Lesson-writers of the Centre who have helped in these endeavours.

Prof. P. Rajasekhar
Vice-Chancellor
Acharya Nagarjuna University

B.SC III YEAR ELECTRONICS PAPER – III
SOLID STATE ELECTRONICS CIRCUITS AND DIGITAL ELECTRONICS

UNIT I

Rectifier and Power Supplies: (a) Rectifier: Half wave, Full wave and Bridge Rectifiers and their efficiency . Ripple factor, regulation, harmonic components in rectifier output. (b) Types of filters: Choke input filter (inductor), Shunt capacitor filter, L - section and P section filters. (c)Regulated power supplies: Series regulated power supply.

Power amplifier: Expression for power , harmonic distortion and efficiency . Push-pull amplifiers , Class A, Class B and Class AB. Advantages and disadvantages

UNIT II

Operational Amplifier :Basic (emitter controlled) difference amplifier and its parameters operational amplifier characteristics of 'n ideal Op Amp. Block diagram of an ideal Op Amp Feedback arrangement Open loop gain, common mode voltage gain, common mode rejection ratio (CMRR), slew rate, offset voltage and bias currents.

Op Amp analysis: Concept of virtual ground . Analysis of inverting amplifier summing amplifier, current and voltage followers Application: Op Amp as comparator, voltage regulator, free running multivibrator and to solve a simple second order differential equation.

UNIT III

Modulation and detection (Qualitative) : Need for modulation. Amplitude modulation and detection : Analysis of amplitude modulated wave, side bands. Simple amplitude modulator circuit and its working. Detection of AM wave (diode detector).

Frequency modulation and detection: Advantages of frequency modulation, side bands (frequency components) Working of a simple frequency modulator. Detection of FM waves.

Electromagnetic spectrum: Identification of areas where radio waves and microwaves are applied. Radio broadcasting and reception , explanation of working of super hetrodyne receiver (block diagram). Microwaves, their properties and applications.

UNIT IV

Digital Electronics: (a) Number system Binary number system, converting binary to decimal and vice versa, Binary addition and subtraction (1's and 2's compliment methods). hexadecimal number system. Converting binary to hexadecimal and vice versa, converting hexadecimal to decimal and vice versa. Binary coded decimal(8421) and gray code, conversion between binary and gray codes ,The ASCII code (American Standard Code for Information Interchange).

(b) Logic gates: OR, AND, NOT gates: Truth tables, realization of these gates using diodes, resistors and transistor circuits. Positive and negative logic. Laws of Boolean algebra, Universal building blocks NAND and NOR gates, transistor - transistor logic (TTL), complimentary metal oxide semiconductor (CMOS) logic.

(c) Combinational logic circuits: Half, full and parallel adders, sequential logic circuits flip-flops (RS, T, D, JK and Master slave JK) their working and truth tables, Binary and decade counters and shift registers.

TEXT BOOKS

1. Integrated Electronics by Millman and Halkias
2. Electronic Communications by Kennedy
3. Principles of Digital Electronics by Malvino and Leach
4. Basic Electronics and Linear Circuits - Bhargava etc

REFERENCE BOOKS

1. A text lab manual in Electronics by ZBAR.(Tata Mc graw Hill)
2. Electronics fundamentals by JD Ryder
3. Modern Electronics Communications by Gray and Miller
4. Digital Electronics by William H.Gothman
5. Op.Amp and linear integrated Circuits by Ramakant Gayakwad
6. Electronic Devices and Circuits by Samuel Seely

B.SC III YEAR (ELECTRONICS)

(For the students admitted in 2004-05 & onwards)

Practical Paper III

1. DC power supply and filters
   a) Full wave rectifier with various filters
   b) Transistor DC regulated power supply and filters
2a. Astable multivibrator (using OP AMP 741)
2b Astable Multivibrator using Transistors/opamps
3. Schmitt Trigger using OP AMP 741
4. Bistable Multivibrator using Transistors
5. Emitter follower
6. Verification of truth tables OR, AND, NOT, NAND, NOR, EX-OR gates and verification of De Morgan's theorems
   6a) IC logic gates 6b) Logic gates with Discrete components
   6c) De Morgan's Theorems
7. Construction of other gates using NAND and NOR gates & construction of half-adders and full adders, verifying their truth tables.
   7a) Universal Logic gates
   7b) Half-Adder & Full Adder
8. Testing and verifying Flip-Flops (RS,D and JK)
9. Testing and verifying counters – Binary (7493), BCD (7490)
   Division module N (1 to 9) & shift registers using JK flip-Flops.
10. OP Amp characteristics –off set null voltage, bias currents, CMRR and slew rate
11. OP amp 741 as
    (a) DC inverting Amplifier (b) Non-inverting Amplifier (DC and AC) © Summer
    (d) Differential Amplifier Tr
12. OP amp 741 as .
    a) Integrator b) Differentiator
13. Op Amp Wein Bridge oscillator
14. Voltage regulator using IC 7805
15. Construction of Astable multivibrator using IC 555.

Any twelve experiments

B.Sc. DEGREE EXAMINATION.

(Examination at the end of Third Year)

Part II - Electronics

Paper III- SOLID STATE ELECTRONIC CIRCUITS AND DIGIGITAL ELECTRONICS

Time: There hours **Maximum: 100 marks**

PART A - (4 x 14 =56marks)

Answer ALL questions.

Each question carries 14 marks.

1. (a) Draw the circuit diagram of a Class – B Push – pull. Amplifier and Discuss its working. Derive expressions for collector efficiency and Output Power. Give the reasons for cross – over Distortion in Push – Pull Amplifiers.

Or

(b) Draw a neat circuit diagram of Bridge Rectifier and describe its operation. What are the advantages and disadvantages?

2. (a) What is an OP-AMP? Mention the characteristics of an ideal OP-AMP. Explain the concept of Virtual – Ground in OP-AMP. Draw the circuit of an OP-AMP Inverting- Amplifier and explain its action.

Or

(b) Draw the pin diagram of Timer IC 555. Draw the circuit of an Astable Multivibrator using OP-AMP and describe its working.

3. (a) Explain how the FM waves are detected. Describe the principle and working of a discriminator.

Or

(b) What are important properties of Microwaves and Mention their applications in detail.

4. (a) What are sequential logic circuits? Describe the working of Master Slave JK Flip Flop.

Or

(b) Draw the block diagram of a Decade Counter and Explain its Operation. Sketch the timing diagram.

PART B - (4 x 5 = 20 marks)

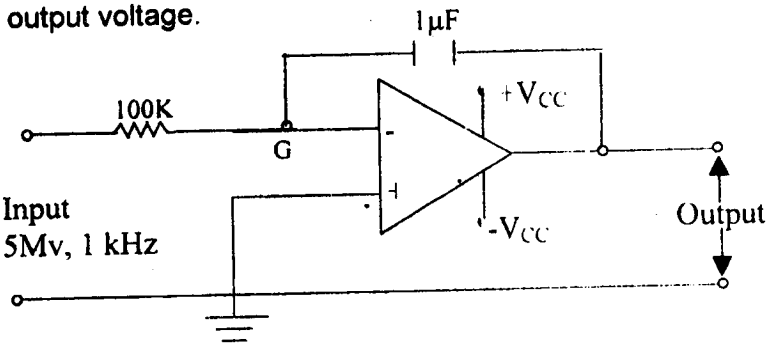
Answer any FOUR questions.

5. What are the advantages of Bridge Rectifier and Full Wave Rectifier?
6. Explain Cross-Over distortion? Explain how it can be eliminated.
7. Explain the working of OP-AMP summing Amplifiers.
8. Draw the circuit diagram of a OP-AMP to solve a Second Order Differential equation.
9. Briefly explain how AM wave is detected.
10. Draw the full adder circuit, and explain its operation.
11. State and explain the basic laws of Boolean Algebra.

PART C - (4 x 6 = 24 marks)

Answer any FOUR questions.

12. Define the terms:
    (a) Ripple factor and
    (b) Regulation
    (c) Rectifier Efficiency as related to Full Wave Rectifier.
13. When a sinusoidal signal is fed to an Amplifier, the Output current is given by. $i_c = 15\sin 400t + 1.5\sin 800t + 1.2\sin 1200t + 0.5\sin 1600t$. Calculate
    (a) Second, Third and Fourth percentage Harmonic Distortions.
    (b) Percentage increase in power due to distortion.
14. 5mV, 1 kHz sine wave is applied at the input of the OP-AMP as shown in fig. Find the output voltage.



15. Calculate the modulation index of an FM wave which has carrier swing of 160 kHz and has been modulated by a signal 10 kHz.

16. Prove the following Boolean identity

$$ABC + A\bar{B}C + AB\bar{C} = A(B + C).$$

17. Multiply :

    (a) 1100 x 101

    (b) 1110 x 111

18. Explain the working of Super Heterodyne Receiver.

B.Sc III YEAR ELECTRONICS PAPER - III

Solid State Electronic Circuits and Digital Electronics

CONTENTS **PAGES**

HALF-WAVE AND FULL - WAVE RECTIFIERS

OBJECTIVES OF THE LESSON

To know the working of half-wave and full-wave rectifiers

STRUCTURE OF THE LESSON

1.1 INTRODUCTION

Most of the electronic circuits need D.C. voltage supply. Even though we plug a computer or T.V. to A.C mains, in side it, there will be a circuit which converts the Mains A.C voltage to D.C. voltage. This D.C. voltage is used to power the electronic circuit with transistors and ICs. So, it is very essential to know how to build a D.C voltage source from A.C mains supply. Alternately Batteries can be used to provide required D.C. voltage, but they are very

HALF-WAVE AND FULL - WAVE RECTIFIERS

OBJECTIVES OF THE LESSON

To know the working of half-wave and full-wave rectifiers

STRUCTURE OF THE LESSON

1.1 INTRODUCTION

Most of the electronic circuits need D.C. voltage supply. Even though we plug a computer or T.V. to A.C mains, in side it, there will be a circuit which converts the Mains A.C voltage to D.C. voltage. This D.C. voltage is used to power the electronic circuit with transistors and ICs. So, it is very essential to know how to build a D.C voltage source from A.C mains supply. Alternately Batteries can be used to provide required D.C. voltage, but they are very

expensive and need regular charging, maintenance and increase the weight and size of the gadget. In this lesson we learn how to assemble a D.C voltage source from A.C mains using rectifier circuits.

A. D.C. power supply provides a certain amount of constant current at a given constant D.C. voltage here, *constant* means, there will be no variation in their values with time. Transistor based circuits need a constant operating voltage in the range between 0 to ±30VD.C. Linear IC based circuits need about ±15V D.C. Digital I.C based circuits need +5V D.C. The current rating for the transistor and Linear I.C circuits and simple digital circuits is usually between 10 to 500mA D.C. For Microprocessor and other high power circuits it will be up to 5 Amps. So, we confine our discussion to Power circuits of this category.

To construct a D.C. power supply, we usually draw power from mains supply, which is provided as Single phase 220V A.C. with 5A A.C. current at a frequency of 50Hz. We can have a D.C. power supply constructed in three ways.

1. Simple unregulated power supply with filter circuit.
2. Transistor or IC based Regulated power supply
3. Switching Mode Power Supply

We consider the first two types in detail as per the syllabus.

1.2 Unregulated D.C. Power supply

An unregulated power supply is one that simply converts the A.C. voltage taken from the A.C supply into required D.C. voltage supply at the required current. It consists of the following parts:

1. Step down transformer
2. Rectifier
3. Filter circuit

1.2.1 Transformer

A transformer consists of two sets of inductance coils wound on a common core. In a power transformer, the first coil called Primary coil or simply Primary is so designed to draw the needed power from A.C mains supply. The other coil even though wound on the same former, is electrically insulated from primary but is magnetically coupled. Whenever there is a change in primary current, a voltage is induced in the secondary coil.

Whatever is the current and voltage requirement, to construct a D.C. power supply, we have to select a power transformer that takes A.C electrical power in its primary coil from electrical mains and provides the required A.C voltage in its secondary coil. A transformer enables us to step up or step down the A.C. voltage to the required level and also provides electrical isolation from A.C. mains. As you

studied in detail about transformers, coils, capacitors, chokes, in your 1st year course, that knowledge is assumed here.

Transformers that provide A.C output voltage less than that of primary voltage are called ***Step-down*** transformers. The secondary to primary voltage ratio depends upon the turns ratio of the transformer. A transformer designed to handle low power will be small in size when compared to a transformer that delivers larger current at the same voltage as it is provided with thicker wires and good quality core.

1.2.2 Rectifier

A Rectifier is device that converts alternating current into unidirectional current. The process of converting A.C to D C is called ***Rectification***. A diode acts as a rectifier. The unidirectional conducting property of diode is used to remove either positive or negative half of the sinusoidal signal applied to it. Time average of a sine wave over a cycle is zero. By removing either the positive or negative half cycle from it, we can mathematically show that the output of a rectifier consists of certain amount of D.C voltage, and superposed on it, various sine waves, whose frequencies are multiples of the frequency of applied A.C voltage. This alternating A.C. component is called ***Ripple***. Ripple component is filtered out using a filter circuit to obtain pure D.C.

For high voltage rectification vacuum tube diodes are preferred. For voltages needed in transistor and I.C circuits, semiconductor diodes are preferred. For low voltage high current applications, Selenium bridge rectifiers are used. A diode has two electrodes called **Anode** and **Cathode**. Current flows through the diode when anode is more positive than cathode. In a semiconductor p-n junction diode, the p-terminal is identical to anode and n-region is the equivalent of cathode.

1.2.3 Filter circuit

Most rectifier circuits use a reservoir capacitor at the output terminal to smooth the rectified voltage in to D.C. voltage. It is important to note that the presence of the reservoir capacitor substantially changes the rectified voltage waveform and often affects the diode current and voltage requirements. A large capacitance whose reactance is negligible when compared to the R_L will serve the purpose. It has the further advantage that the capacitor stores the charge and retains the potential during the off-period of the diode, thereby improving the amplitude of D.C voltage.

If we use a single rectifier to rectify A.C. it is called a ***half-wave rectifier*** as we are using only half of the sinusoidal input wave. See Fig 1.1

1.3 HALF-WAVE RECTIFIER

Fig.1.1 shows the circuit of a half-wave rectifier. The rectified output consists of half sinusoids as shown in the Fig.1.1. This has a time average of D.C and several A.C components which have to be filtered, to get pure D.C voltage across load resistance R_L. A semiconductor diode with required current rating and reverse breakdown voltage is used for rectification. As these diodes are designed to handle larger power than ordinary diodes, these are usually called Power rectifiers. Usually a BY127 or 1N4001 serves the purpose for low power applications.

Working

A diode conducts only during positive half cycle of the input cycle when connected as shown in the Fig.1.1. So, current flows during positive half cycles of the input and produces a voltage drop across the load resistance R_L. The repetition frequency of the half sinusoids is same as the input A.C waveform. As it is, this rectifier is not suitable as D.C. source, as the output is a time varying waveform. However, it has a time averaged D.C component also. This D.C voltage is obtained by filtering out the A.C portion of the output using a suitable filter.

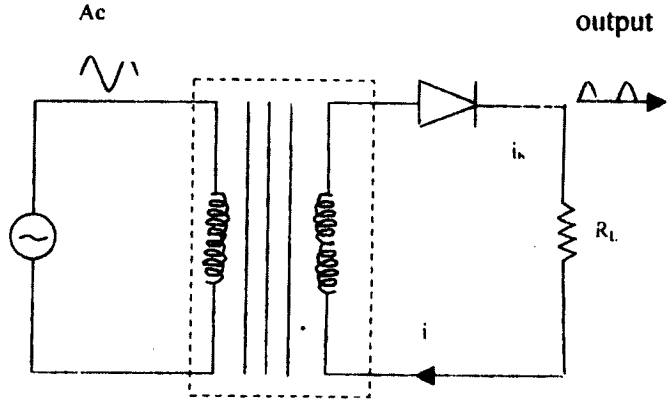


Fig.1.1 Half-wave rectifier

When a diode is forward biased, the voltage drop across it is V_F and the output voltage is

$$V_{po} = V_{pi} - V_F$$

Note that $V_p = 1.414V_i$

Where V_i is the rms level of the sinusoidal input voltage.

The diode peak forward current is

$$I_F = \frac{V_{pi}}{R_f}$$

During the negative half-cycle of the input, the reverse biased diode offers a very high resistance. So only a very small reverse current (I_R) flows giving an output voltage,

$$-V_o = -I_R \times R_L.$$

While the diode is reverse biased , the peak voltage of the negative half-cycle of the input is applied across its terminals. Thus, the peak reverse voltage of peak inverse voltage (PIV), applied to the diode is

$$V_R = PIV = V_{pi}$$

1.3.1 Average current and voltage components

For the sinusoidal input to the transformer, the output voltage across the secondary of transformer will also be sinusoidal having frequency same as that of the input. Let the voltage across the secondary of transformer be given as $v = V_0 \sin \omega t$ where V_0 is the peak voltage across the secondary and $\omega/2\pi$ is the frequency. If R_f be the dynamic forward resistance of the diode, R_s the resistance of the secondary of the transformer and R_L the load resistance the instantaneous current i_b through resistance R_L is given by

$$i_b = \frac{voltage}{total\ resistance} = \frac{v}{R_f + R_S + R_L} = \frac{V_0 \sin \omega t}{R_f + R_S + R_L} \qquad \ldots\ldots\ldots\ldots\ldots\ldots (1.3.1)$$

$$= I_0 \sin \omega t$$

Where the maximum value of current

$$I_0 = \frac{V_0}{R_f + R_S + R_L}$$

Since this current i_b flows only for half cycle, hence

$i_b = I_0 \sin \omega t$ during $0 \le \omega t \le \pi$,

and $i_b = 0$ during $\pi < \omega t \le 2\pi$, $\qquad \ldots\ldots\ldots\ldots\ldots\ldots (1.3.2)$

Average values:

The average value of current (I_{av}) through R_L can be given by

$$I_{av} = I_{dc} = \frac{\int_0^T i_b\,dt}{\int_0^T dt} = \frac{\int_0^{T/2=\pi/\omega} I_0 \sin \omega t\,dt + \int_{T/2}^{T} 0.dt}{\int_0^{2\pi/\omega} dt}$$

$$= \frac{-\frac{I_0}{\omega}[\cos\omega t]_0^{T/2=\pi/\omega} + 0}{2\pi/\omega} = \frac{I_0}{\pi}$$

$$= \frac{V_0}{\pi(R_f + R_s + R_L)} \qquad \ldots\ldots\ldots\ldots\ldots\ldots (1.3.3)$$

Hence the dc or average voltage at the load R_L will be

$$V_{dc} = I_{dc}R_L = \frac{I_0 R_L}{\pi} = \frac{V_0 R_L}{\pi(R_f + R_s + R_L)} = \frac{V_0}{\pi\left[1 + (R_f + R_s)/R_L\right]}$$

$$= \frac{V_0}{\pi}\left[1 + \frac{R_f + R_s}{R_L}\right]^{-1} = \frac{V_0}{\pi} - \frac{V_0}{\pi R_L}(R_f + R_s)$$

$$= \frac{V_0}{\pi} - I_{dc}(R_f + R_s) \qquad \ldots\ldots\ldots\ldots\ldots\ldots (1.3.4)$$

This shows that the dc output voltage depends not only upon the load current but the diode and transformer resistance also.

These two equation give the dc or or average power across the load R_L.

$$\therefore \quad P_{dc} = V_{dc}I_{dc} = I_{dc}^2 R_L = \frac{V_0^2 R_L}{\pi^2(R_f + R_s + R_L)^2} \qquad \ldots\ldots\ldots\ldots\ldots\ldots (1.3.5)$$

R.M.S value of the current:

The Root Mean Square or effective value of current in the circuit can be given as

$$I_{rms}^2 = \frac{\int_0^T i_b^2\,dt}{\int_0^T dt} = \frac{\int_0^{T/2=\frac{\pi}{\omega}} I_0^2 \sin^2\omega t\,dt + \int_{\frac{T}{2}}^{T=\frac{2\pi}{\omega}} dt}{\int_0^{T=\frac{2\pi}{\omega}} dt} = \frac{I_0^2}{4},$$

$$\text{Or} \quad I_{rms} = I_0/2 = V_0/2(R_f + R_s + R_L) \qquad \ldots\ldots\ldots\ldots\ldots\ldots (1.3.6)$$

Thus the I_{rms} is greater than the dc component I_{dc}. This also show that the R.M.S value of the half rectified current is not the same as the R.M.S value of the sinusoidal current which is $I_0/\sqrt{2}$.

1.3.2 Harmonic components of rectified output

Frequency components of rectified output: The output current of the rectifier can be assumed as consisting of several harmonics of frequency and can be written in terms of Fourier series as

$$i_b = A_0 \sum A_n \cos n\omega t + \sum B_n \sin n\omega t,$$

Where the coefficients A_0, A_n and B_n are given by

$$A_0 = \frac{1}{T}\int i_b dt, A_n = \frac{2}{T}\int i_b \cos n\omega t\, dt$$

$$and\ B_n = \frac{2}{T}\int i_b \sin n\omega t dt.$$

On solving the integrals using the limiting values of i_b from equation, we get equation as

$$i_b = I_0\left[\frac{1}{\pi} + \frac{1}{2}\sin\omega t - \frac{2}{3\pi}\cos 2\omega t - \frac{2}{15\pi}\cos 4\omega t.....\right] \cdots\cdots\cdots\cdots\cdots\cdots (1.3.7)$$

The first term of the series gives the directs or average component and is equal to the Eq.(1.3.7).The second term has its frequency same as that of the supply with peak value $I_0/2$. The rms value of this fundamental frequency component will be

$$= \frac{peak\ value}{\sqrt{2}} = \frac{I_0/2}{\sqrt{2}} = \frac{I_0}{2\sqrt{2}}. \qquad \cdots\cdots\cdots\cdots\cdots\cdots (1.3.8)$$

The third term gives the second harmonic term. The other frequency terms are also there in the equation. So through the load resistance R_L, dc as Well as ac components will pass.

1.3.3 Other important parameters of half-wave rectifier

Rectifier efficiency: The efficiency of the rectifier, also known as ratio of rectification, is defined as

η = Direct output power / Alternating input power from transformer secondary

$$= \frac{P_{dc}}{P_{ac}}.$$

The input power from transformer secondary is the power that would be indicated by a wattmeter placed in the rectifying circuit with its terminals connected across the transformer secondary. Thus

$$P_{ac} = I_{rms}^2 R_f + I_{rms}^2 R_L = \frac{1}{4} I_0^2 (R_f + R_L)$$

$$\therefore \eta = \frac{I_0^2 R_L}{\pi^2} \times \frac{4}{I_0^2 (R_f + R_L)} = \frac{4R_L}{\pi^2 (R_f + R_L)}$$

or

$$\%\ of\ \eta = \frac{4}{\pi^2 [1 + R_f / R_L]} \times 100 = \frac{40.6}{[1 + R_f / R_L]} \cdots\cdots\cdots\cdots\cdots\cdots (1.3.9)$$

The given the theoretical efficiency of a half wave rectifier which increase as $R_f / R_L \to 0$. Thus the maximum efficiency will be 40.6%. But the rectifier delivers maximum output power when the load resistance is equal to R_f. So, the efficiency is now reduced to 20.3 percent only.

Transformer Utilization Factor (TUF): The transformer utilization factor TUF is defined as

TUF = dc power delivered to the load /ac rating of the transformer secondary

$$= \frac{P_{dc}}{P_{ac}(rated)}.$$

The rating of the transformer secondary is different from the actual power delivered by the secondary. It is the product of the rated R.M.S. voltage of the secondary $V_0 / \sqrt{2}$ .and the actual R.M.S.current flowing through the secondary $I_0 / 2$. Hence

$$TUF = \frac{(I_0 / \pi)^2 R_L}{(V_0 / \sqrt{2})(I_0 / 2)}.$$

$$since \quad V_0 = I_0(R_f + R_s + R_L),$$

Therefore

$$TUF = 0.286/[1 + (R_s + R_f)/R_L] = \eta \times 0.707 \qquad \text{.....(1.3.10)}$$

Thus the TUF is different from the rectifier efficiency.

Ripple factor: This represents the fluctuating, pulsating or alternating part in the output of rectifier. As obtained from Fourier analysis the output wave consists of altering components called as ripples. So ripple factor is a measure of the fluctuating or pulsating components i.e. purity of output. It is defined as the ratio of the effective value of the ac components of the current or voltage to the direct or average value of the current or voltage i.e.

$$Ripple\ factor(r) = \frac{effective\ value\ of\ ac\ components}{dc\ value\ of\ the\ components}$$

The output current of a rectifier (I_{rms}) consists of the direct component (I_{dc}) and effective value of all ac components (I'_{rms}).

$$I^2_{rms} = I^2_{dc} + I'^2_{rms} \quad or \quad I'_{rms} = (I^2_{rms} - I^2_{dc})^{1/2}$$

$$\therefore r = \frac{I'_{rms}}{I_{dc}} = \left(\frac{I^2_{rms}}{I^2_{dc}} - 1\right)^{1/2}$$

So for a half wave rectifier

$$r=\left[\left(\frac{I_0/2}{I_0/\pi}\right)^2-1\right]^{1/2}=\left[\frac{\pi^2}{4}-1\right]=1.21. \qquad \text{.....(1.3.11)}$$

$$\therefore I'_{rms}=1.21I_{dc}.$$

Similarly $V'_{rms}=1.21V_{dc}$.

This shows that the effective values of the ac components of the output exceeds the dc value of the output. Thus we see that the half-wave rectifier is not a suitable device for obtaining dc.

Peak Inverse Voltage: Peak inverse voltage (PIV) is defined as the maximum voltage present across the diode ends when the diode is reverse biased and thus does not conduct. For half-wave rectifier the non-conducting periods is during the negative part of applied alternating wave and its peak valve is equal to V_0. Thus for a half-wave rectifier PIV = V_0. To avoid breakdown, PIV must be less than the PIV rating of the diode.

Voltage regulation: It is a measure of the ability of a rectifier to maintain a specified output voltage with the variation of load resistance and is defined as

$$\text{Voltage regulation(V.R.)}=\frac{\textit{output at no load}-\textit{output at full load}}{\textit{output at full load}}$$

In a perfect voltage regulator the output voltage does not charge with the load resistance. For a half-wave rectifier we have.

$$V_{dc}=I_{dc}R_L=\frac{I_0R_L}{\pi}=\frac{V_0R_L}{\pi(R_f+R_s+R_L)}=\frac{V_0}{\pi\left[1+(R_f+R_s)/R_L\right]}$$

$$=\frac{V_0}{\pi}\left[1+\frac{R_f+R_s}{R_L}\right]^{-1}=\frac{V_0}{\pi}-\frac{V_0}{\pi R_L}(R_f+R_s)$$

$$=\frac{V_0}{\pi}-I_{dc}(R_f+R_s). \qquad \text{.....(1.3.12)}$$

Assuming here (R_f+R_S) << R_L, the higher powers of (R_f + R_S) /R_L are neglected for load (open circuit, $R_l = \infty$), I_{dc}= 0 and $V_{dc} = V_0/\Pi$.

At full load, we have

$$(V_{dc})_{full\ load}=(V_{dc})_{no\ load}-(I_{dc})_{full\ load}.(R_f+R_S)$$

$$\therefore\ \textit{Voltage regulation}=\frac{(V_0/\pi)-(V_0/\pi)-\left[\left((I_{dc})_{full\ load}\right)(R_f+R_S)\right]}{V_0/\pi-\left((I_{dc})_{full\ load}\right)(R_f+R_S)}$$

$$= \frac{\left((I_{dc})_{full\ load}\right)(R_f + R_S)}{V_0 / \pi - \left((I_{dc})_{full\ load}\right)(R_f + R_S)}$$

Thus the voltage regulation is very poor in half –wave rectifiers.

Current rating of diode: In a half wave rectifier, the dc diode current is equal to the dc load current. On the sheets, I_{dc} is usually listed as I_0, known as current rating of the diode; this tells us how much direct current the diode can handle. The diode must have current rating greater than the average rectified current.

The simple half-wave rectifier filters combination although gives D.C. voltage, it has got several disadvantages. The three major disadvantages are

a. Its output changes with input A.C. supply voltage.
b. Its output voltage changes with the amount of load current drawn.
c. Ripple increases at higher load currents.

1.4 Full-wave rectifier

. To utilize the total power content, and to reduce the ripple, we have to rectify the full-wave. This can be done in two ways;

1) A transformer with centre-tapped secondary and two diodes
2) four diodes arranged in a bridge form and a transformer

1.4.1 Full-wave rectifier using a transformer with centre-tapped secondary and two diodes:

The circuit is shown in Fig 1.2

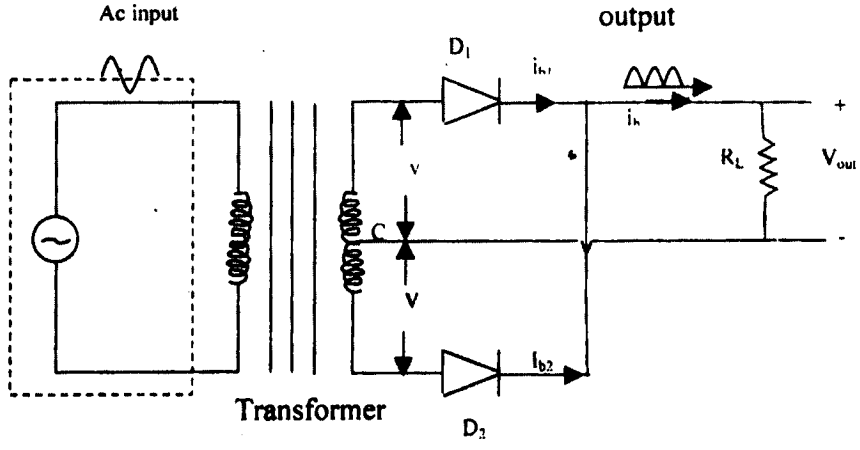


Fig.1.2 Full-wave rectifier with two diodes

The circuit is essentially a combination of two half–wave rectifier circuits, each supplied from half of the transformer secondary. When the transformer output voltage is positive at the top, as illustrated in Fig.1.2., the anode of D_1 is positive and the center-tap of the transformer is connected to the cathode of D_1 via R_L.

Consequently, D_1 is forward biased, and load current (I_L) flows from the top of the transformer secondary though D_1 through R_L from top to bottom and back to the transformer center-tap. During this time, the polarity of the voltage from the bottom half of the transformer secondary causes diode D_2 to be reverse- biased.

For the duration of the negative half-cycle of the transformer output, the polarity of the transformer secondary voltage causes D_1 to be reversed biased and D_2 to be forward biased I_L flows from the bottom terminal of the transformer secondary through diode D_2, through R_L from top to bottom, and back to the transformer center-tap. The output waveform is the combination of the two half-cycles; that is, a continuous series of positive half-cycles of sinusoidal waveform. This is full wave rectification and the circuit is called a full-wave rectifier.

1.4.2 Average current and voltage components of a full-wave rectifier:

As both the diodes are considered to be identical, also considering that the dynamic characteristic is linear for each diode, the mathematical analysis of full wave rectifier can be given as follows:

Let $v = V_0 \sin\omega t$ be the applied alternating potential also considering that the dynamic forward resistance of each diode and R_s the resistance of the secondary of transformer. The instantaneous value of current through the load will be equal to the sum of the currents due to diodes D_1 and D_2 at that instant. These currents are given by the relations.

$$i_{b1} = \frac{V_0}{(R_f + R_S + R_L)} \sin\omega t = I_0 \sin\omega t \quad \Bigg\} \quad \text{during } 0 \le \omega t \le \pi,$$

$I_{b2} = 0$

Also

$I_{b1} = 0$ $\Bigg\}$ during $\pi \le \omega t \le 2\pi$,

$$i_{b2} = \frac{V_0}{(R_f + R_S + R_L)} \sin(\omega t + \pi) = -I_0 \sin\omega t \quad \Bigg\}$$

.....(1.4.1)

Average values:

The average value of current (I_{dc}) through R_L can be given by

$$I_{av} = I_{dc} = \frac{\int_0^T i_b dt}{\int_0^T dt} = \frac{\int_0^{\frac{T}{2}} I_0 \sin \omega t \, dt + \int_{\frac{T}{2}}^{T} (-I_0 \sin \omega t).dt}{\int_0^{T=\frac{2\pi}{\omega}} dt}$$

$$= \frac{2I_0}{\pi} = \frac{2V_0}{\pi(R_f + R_s + R_L)} \qquad \text{.....(1.4.2)}$$

So, the dc or average voltage at the load R_L will be

$$V_{dc} = I_{dc} R_L = \frac{2I_0 R_L}{\pi} = \frac{2V_0 R_L}{\pi(R_f + R_s + R_L)} = \frac{2V_0}{\pi\left[1 + (R_f + R_s)/R_L\right]}$$

and $P_{dc} = V_{dc} I_{dc} = I_{dc}^2 R_L = \frac{4V_0^2 R_L}{\pi^2\left[(R_f + R_s + R_L\right\}^2]}$

rms value of current: The rms (or effective) value of current in the circuit can be given as

$$I_{rms}^2 = \frac{1}{T}\left[\int_0^{T/2} (i_{b1})^2 dt + \int_{T/2}^{T} \{i_{b2}\}^2 dt\right]$$

$$I_{rms}^2 = \frac{\int_0^{T} i_b^2 dt}{\int_0^{T} dt} = \frac{\int_0^{\frac{T}{2}=\frac{\pi}{\omega}} I_0^2 \sin^2 \omega t dt + \int_{\frac{T}{2}}^{T} dt}{\int_0^{T=\frac{2\pi}{\omega}} dt} = \frac{I_0^2}{2},$$

Or $I_{rms} = I_0/\sqrt{2}$ $\frac{V_0}{\sqrt{2}(R_f + R_s + R_L)}$ .....(1.4.3)

1.4.3 Harmonic components of rectified output

Frequency components of rectified output: Fourier analysis of the output waveform of the Full-wave rectifier will be having frequency components depending upon the resultant due to the waveform of each diode output

$$i_{b1} = I_0\left[\frac{1}{\pi} + \frac{1}{2}\sin \omega t - \frac{2}{3\pi}\cos 2\omega t - \frac{2}{15\pi}\cos 4\omega t.....\right]$$

Since i_{b2} is 180^0 out of phase with i_{b1} and hence

$$i_{b1} = I_0\left[\frac{1}{\pi} - \frac{1}{2}\sin \omega t - \frac{2}{3\pi}\cos 2\omega t - \frac{2}{15\pi}\cos 4\omega t.....\right]$$

Therefore the total current

$$i_b = I_0\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t.....\right] \qquad .....(1.4.4)$$

This equation shows that a lowest frequency term has a frequency twice the frequency of the input source and the odd harmonics are not present.

1.4.4 Other important parameters

Rectifier efficiency: The percentage of efficiency is defined as

$$\%\ of\ \eta = \frac{P_{dc}}{P_{ac}} \times 100 = \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_f + R_s + R_L)} \times 100$$

$$= \frac{(2I_0/\pi)^2 R_L \times 100}{(I_0/\sqrt{2})^2 (R_f + R_s + R_L)} = \frac{81.2\, R_L}{(R_f + R_s) + R_L} = \frac{81.2}{1 + (R_f + R_s)/R_L}$$

Ripple factor. The ripple factor is given by

$$r = \left[\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1\right]^{1/2} = \left[\left(\frac{I_0/\sqrt{2}}{2I_0/\pi}\right)^2 - 1\right]^{1/2}$$

$$= \left[(1.117)^2 - 1\right]^{1/2} = 0.48 \qquad .....(1.4.5)$$

PEAK INVERSE VOLTAGE: In the case of full-wave rectifier when one diode (say D_1) is conducting, the other diode (D_2) will be non- conducting. The kerchief's laws can be applied to fig, the equation obtained will be

$$v_{b1} - v_{b2} + 2V_0 \sin \omega t = 0$$

Where v_{b1} and v_{b2} are the potential drops across D_1 and D_2 respectively. If the diode D_1 is conducting we can consider the potential drops across it as zero, hence the potential drops across non- conducting diode (D_2) will be

$$v_{b2} = 2V_0 \sin \omega t \quad or \quad (v_{b2})_{max} = 2V_0$$

Similarly for the diode (D_2) as conducting and (D_1) non- conducting

$$v_{b1} = -2V_0 \sin \omega t \quad or \quad (v_{b1})_{max} \quad 2V_0$$

So the peak inverse voltage (PIV) for the diode used for full wave rectifier circuit is $2V_0$, each diode must have sufficient insulation to with stand this voltage, or PIV rating greater than $2V_0$.

Voltage regulation: The Voltage regulation is given by

$$V.R. = \frac{(V_{dc})_{no\ load} - (V_{dc})_{full\ load}}{(V_{dc})_{full\ load}}$$

Here $$(V_{dc}) = \frac{2V_0 R_L}{\pi(R_f + R_s + R_L)} = \frac{2V_0}{\pi}\left[1 + \frac{R_f + R_s}{R_L}\right]$$

$$= \frac{2V_0}{\pi} - \frac{2V_0}{\pi} \cdot \frac{R_f + R_s}{R_L} = \frac{2V_0}{\pi} - I_{dc}(R_f + R_s) \qquad \text{.....(1.4.6)}$$

Here we have assumed $(R_f + R_S) < R_L$

At no load (open circuit $R_L=\infty$), $I_{dc}= 0$, and $V_{dc}=2V_0/\pi$.

At full load we have,

$$(V_{dc})_{full\ load} = (V_{dc})_{no\ load} - (I_{dc})_{full\ load}(R_f + R_S)$$

$$\therefore \text{Voltage regulation} = \frac{(I_{dc})_{full\ load}(R_f + R_S)}{[(2V_0/\pi) - (I_{dc})_{full\ load}(R_f + R_S)]}$$

.....(1.4.7)

Current rating of diodes: The current rating of each diode I_0 must be greater than half the dc load current.

1.5 Full-wave rectifier using diode bridge:

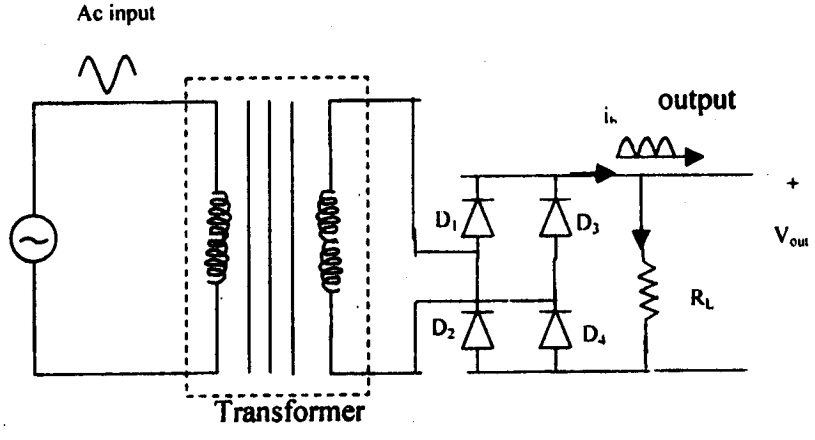


Fig.3 Full-wave bridge rectifier

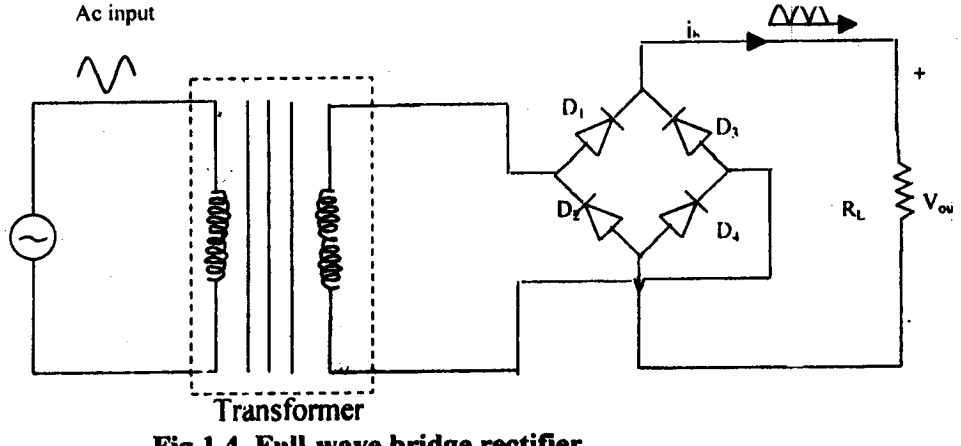


Fig.1.4 Full-wave bridge rectifier

The center-tapped transformer used in the circuit of Figs.1 and 2 is usually more expensive and requires more space than additional diodes. So, a bridge rectifier is the mot most frequently used for full-wave rectification. The bridge rectifier circuit shown in Fig.1.3 consists of four diodes connected with their arrowhead all pointing toward the positive output terminal of the circuit. Diodes D_1 and D_2 are series-connected, as are D_3 and D_4. The ac input terminals are the junction of D_1 and D_2 and the junction of D_3 and D_4. The positive output terminal is at the cathodes of D_1 and D_3, and the negative output is at the anodes of D_2 and D_4

During the positive half-cycle of input voltage, diodes D_1 and D_4 are in series with R_L. Thus load current (I_L) flows from the positive input terminal through D_1 to R_L , and then through R_L and D_4 back to the negative input terminal. Note that the direction of the load current through R_L is from top to bottom. During this time, the positive input terminal is applied to the cathode of D_2, and the negative output is at D_2 anode. So, D_2 is reverse biased during the positive half-cycle of the input. Similarly, D_3 has the negative input at its anode and the positive output at its cathode during the positive input half-cycle, causing D_3 to be reverse biased. The diodes D_2 and D_3 are forward biased during the negative half-cycle of the input waveform, while D_1 and D_4 are reverse biased. Although the circuit input terminal polarity is reversed, I_L again flows through R_L from top to bottom, via D_3 and D_2 .

In Fig 1.4, the bridge circuit is drawn in the conventional form which is seen in various text books. The working is same. It will be easy to remember the diode bridge arrangement, if we follow the Fig1.3.

It is seen that during both half-cycles of the input, the output terminal polarity is always positive at the top of R_L , negative at the bottom. Both positive and negative half-cycles of the input are passed to the output. The negative half–cycles are inverted, so that the output is a continuous series of positive half-cycles of sinusoidal voltage.

The bridge rectifier has two forward-biased diodes in series with the supply voltage and the load. Because each diode has a forward drop (V_F), the peak output voltage is,

$$V_{po} = V_{pi} - 2V_F$$

As in the case of the half-wave rectifier. A reservoir capacitor substantially changes the full-wave rectified output voltage waveform and affects the diode current and voltage requirements.

1.5.1 Average current and voltage components of a full-wave bridge rectifier

Instantaneous currents through the load R_L will be given as

$$i_{b1} = \frac{V_0}{(2R_f + R_S + R_L)} \sin \omega t = I_0 \sin \omega t \quad \left.\right\} \text{ during } 0 \le \omega t \le \pi,$$

$I_{b2} = 0$

and Also

$I_{b1}=0$

$$i_{b2} = \frac{V_0}{(2R_f + R_S + R_L)} \sin(\omega t + \pi) = -I_0 \sin \omega t \quad \left.\right\} \text{ during } \pi < \omega t \le 2\pi,$$

Thus the maximum current through the load is

$$\frac{V_0}{(2R_f + R_S + R_L)} \sin(\omega t) = I_0$$

The expressions for the average dc, r.m.s value of current, rectifier efficiency and ripple factor may be obtained as for the full-wave rectifier.

$$I_{dc} = \frac{2I_0}{\pi} = \frac{2V_0}{\pi(2R_f + R_S + R_L)},$$

$$V_{dc} = \frac{2V_0}{\pi\left[1 + (2R_f + R_s)/R_L\right]},$$

$$I_{rms} = V_0 \Big/ \sqrt{2}(2R_f + R_s + R_L),$$

$$\% \text{ of } \eta = \frac{81.2}{[1 + (2R_f + R_S)/R_L]}$$

And r = 0.48

The peak inverse voltage across each diode is the peak voltage (V_0) across the secondary of transformer instead of $2V_0$, the PIV value for full-wave rectifier.

1.5.2 Advantages and disadvantages of bridge rectifier

1. Small transformer can be used.
2. Central tap on the secondary of the transformer is not required.
3. PIV per diode is V_0 instead of $2V_0$ in a full-wave rectifier.

The main **disadvantages** of this type of rectifier are

1. The circuit requires two extra diodes. and
2. It has a poor voltage regulation.

1.5.3 Peak loss

An aspect of most rectification is a loss from peak input voltage to the peak output voltage, caused by the built-in voltage of the diodes (around 0.7 V for ordinary silicon p-n-junction diodes and 0.3 V for Schottky diodes). Half-wave rectification and full-wave rectification using two separate secondary windings will have a peak voltage loss of one diode drop. Bridge rectification will have a loss of two diode drops. This may represent significant power loss in very low voltage supplies. In addition, the diodes will not conduct below this voltage, so the circuit is only passing current through for a portion of each half-cycle, causing short segments of zero voltage to appear between each "hump".

1.5.4 Comparison of half-wave and full-wave rectifiers

1. In half -wave rectifier, the current flows through the secondary of the transformer always in the same direction, the dc saturation of the transformer core takes place. This produces hysteresis loss and harmonics in the secondary output and reduces the efficiency of transformer. In a full-wave rectifier equal currents flows through the two halves of the center tapped secondary of the transformer in opposite directions and hence no core saturation exists.
2. The average or dc values of currents and voltages are double in case of full-wave in comparison of half -wave rectifier.
3. Effective or r.m.s value of output current in full-wave rectifier is $\wp$ times the value for half -wave rectifier.
4. The dc power delivered to the load by a full-wave rectifier is 4 times the power delivered by a half-wave rectifier.
5. The fundamental angular frequency term is eliminated in full-wave rectifier secondary harmonics component (2ω) in the output of full-wave rectifier is easier to filter out.
6. Efficiency of full-wave rectifier is twice that of half -wave rectifier.
7. The ripple factor of full-wave rectifier is quite low (0.48) than of a half -wave rectifier (1.21). The full-wave rectifier converts higher percentage of power

into desired dc power with smaller portions as undesired ac. So for a half-wave rectifier a comparatively expensive smoothing filter is required.

8. The full-wave rectifier diode must be chosen such that is insulation strength is sufficient to withstand the peak inverse voltage of $2V_0$. PIV is V_0 only for a diode of half-wave rectifier.
9. The half-wave rectifier has poor voltage regulation in comparison to a full-wave, i.e. the change in the output of a full-wave is smaller than that or a half-wave rectifier. The half-wave rectifier has the chief advantage of simplicity and low design cost and PIV value compared to a full-wave rectifier. But the above points clearly indicate that a full-wave rectifier has higher efficiency, higher dc output values, less core saturation, less ripple factor and higher voltage regulation. So for a better rectification full-wave rectifier is always preferred than a half-wave rectifier.

1.6 SUMMARY

Most of the present day electronic units work on D.C. Power supply. Transistor based circuits need operating voltage in the range between 0 to ±30V. Linear IC based circuits need ±15VD.C. Digital I.C based circuits need +5V. So, it is very essential to know how to build a D.C voltage source from A.C mains supply.

A D.C. Power supply can be constructed in three ways.

1. Simple unregulated power supply with filter circuit.
2. Transistor or I.C based Regulated power supply
3. Switching Mode power supply

Simple unregulated power supply is used in low-cost commercial electronic items Transistor or I.C based Regulated power supply are used in laboratory and scientific electronic equipment.

An unregulated power supply is one that simply converts the A.C. voltage taken from the A.C. Supply into required D.C. voltage supply at the required current. It consists of the following parts:

1. Step down Transformer
2. Rectifier
3. Filter circuit

The maximum efficiency of a half-wave rectifier will be 40.6%. But the rectifier delivers maximum output power when the load resistance is equal to R_f , the efficiency is now reduced to 20.3 percent only. The effective values of the ac components of the output exceed the dc value of the output. So, the half-wave rectifier is not a suitable device for obtaining dc.

Voltage regulation is a measure of the ability of a rectifier to maintain a specified output voltage with the variation of load resistance and is defined as

$$\text{Voltage regulation}(\text{V.R.}) = \frac{\textit{output at no load} - \textit{output at full load}}{\textit{output at full load}}$$

voltage regulation is very poor in half–wave rectifiers.

Ripple factor is defined as the ratio of the effective value of the ac components of the current or voltage to the direct or average value of the current or voltage i.e.

$$\textit{Ripple factor}(r) = \frac{\textit{effective value of ac components}}{\textit{dc value of the components}}$$

A full-wave rectifier can be formed by

1. A step-down transformer with centre-tapped secondary and two diodes.
2 Four diodes arranged in a bridge form and a step-down transformer.

The output waveform of a full-wave rectifier is a continuous series of positive half-cycles of sinusoidal waveform.

The bridge rectifier has two forward-biased diodes in series with the supply voltage and the load. Because each diode has a forward drop (V_F), the peak output voltage is,

$$V_{po} = V_{pi} - 2V_F$$

For a given tolerable ripple the required capacitor size is proportional to the load current and inversely proportional to the supply frequency and the number of output peaks of the rectifier per input cycle. The load current and the supply frequency are generally outside the control of the designer of the rectifier system but the number of peaks per input cycle can be affected by the choice of rectifier design.

A half-wave rectifier will only give one peak per cycle and for this and other reasons is only used in very small power supplies. A full wave rectifier achieves two peaks per cycle and this is the best that can be done with single-phase input.

1.7 KEY TERMINOLOGY

Regulation: Keeping a parameter to be in set limits irrespective of the other parameters that otherwise cause changes in the first parameter

Unregulated D.C. power supply: A D.C. supply that has no mechanism to keep its output voltage at a constant value when changes in load current or input supply value changes.

Rectifier: A rectifier is a diode. There are two types of rectifiers. 1) Signal rectifier 2) Power supply rectifier. Even though basically both the types perform the same task, a signal diode is used to rectify modulated r.f waves to recover the modulated signal or for demodulation .A diode meant for use as a rectifier in power supply will have large current carrying capacity and large reverse break down voltage.

1.8 Self assessment Questions:

Long answer Questions

1. What is a rectifier?. Explain the working of a full-wave rectifier. Obtain expression for average and RMS values of current and efficiency.
2. Describe the working of a full-wave rectifier with centre tapped transformer.
3. Describe the working of a full-wave rectifier and obtain expression for efficiency.
4. Explain the circuit diagram of a bridge rectifier and explain its operation with waveforms. Derive expressions for its efficiency and ripple factor.

A half-wave rectifier uses silicon diode with a forward resistance of 0.05 ohms and a threshold voltage of 0.7 Volt.It has a secondary emf of 14.4 Volts(r.m.s) with a resistance of 0.2 ohms. For a load resistance of 15 ohms calculate
i) dc load current, ii) dc load voltage, III) voltage regulation and IV) efficiency.

Short answer questions

1. The dc output voltage is 40 Volts at full load and 41 Volts with out any load current. calculate the load regulation factor in percent
2. If the output voltage of a centre tap full-wave rectifier is 100V. Determine the peak inverse voltage.
3. Explain about π - section filter.
4. Compare half and full-wave rectifiers
5. A full-wave rectifier delivers 50W to a load of 200ohms. If the ripple factor is 2%, calculate the a.c. ripple voltage across the load.
6. A half wave rectifier uses a transformer of turns ratio 8:1 . If the primary voltage is 230V (r.m.s), find (i) dc output voltage,(ii) peak inverse voltage.
7. A full-wave rectifier uses a centre-tapped transformer. The ac voltage from its centre tap to either end is 10 sin 314t. The load resistance of the circuit is 40Ω and diode resistance 10Ω . Find I_{dc}, I_{rms}, ripple factor and efficiency.

8. An ac supply of 230V, 50Hz is applied to bridge type full-wave rectifier circuit through a transformer of turns ratio 4:1. Assuming the diodes to be ideal and resistance R_L= 200 Ω, find i) dc output voltage, peak inverse voltage, output efficiency.

1.9 Text and Reference Books:

1. Integrated Electronics by Millman and Halkias

2. Basic Electronics and Linear Circuits - Bhargava etc

REFERENCE BOOKS

1. A text lab manual in Electronics by ZBAR (Tata Mc graw Hill)
2. Electronics fundamentals by JD Ryder
3. Electronic Devices and Circuits by Samuel Seely.

UNIT I LESSON 2

D.C.POWER SUPPLY WITH VARIOUS FILTERS

OBJECTIVES OF THE LESSON

To learn about the effect of filters on the performance of power supplies.

STRUCTURE OF THE LESSON

2.1 INTRODUCTION

While half-wave and full-wave rectification suffice to deliver a form of DC output, neither produces constant-voltage DC. The ripple is 121% in the output of the half - wave rectifier, and 48% , in the full-wave rectifier. This large amount of ripple can not be tolerated especially in power supplies. The unwanted ac-components of the output can be filtered using filter circuits discussed in our first year course.

To smooth the output voltage of rectifiers, filter circuits (also know as smoothing circuits) are used. There are the various combinations of the capacitors and inductors. These are low pass filters.

The most common arrangements of filter used are: (a) shunt capacitor b) series inductor (c) L-section and (d) Π-section filters.

2.2 Half-wave rectifier with shunt capacitor filter:

A capacitor connected in parallel with the load resistance serves, effectively as a filter for ac components. The simple circuit for capacitor filter half-wave rectifier is shown in Fig.2.1. The reactance offered by capacitor $X_c = 1/\omega C$, so for dc ($\omega = 0$),

it offers an infinite resistance, while for any frequency (ac), its value decreases with increase in frequency. So, if the resistance due to capacitor is very small in comparison of load resistance (i.e., $1/\omega C << R_L$), then most of the ac or harmonic components will bypass through capacitor and will not appear through R_L. This will improve the D.C. output.

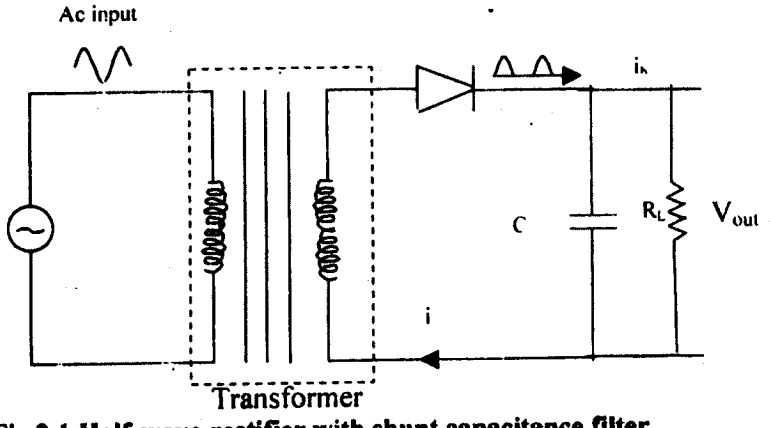


Fig 2.1 Half-wave rectifier with shunt capacitance filter

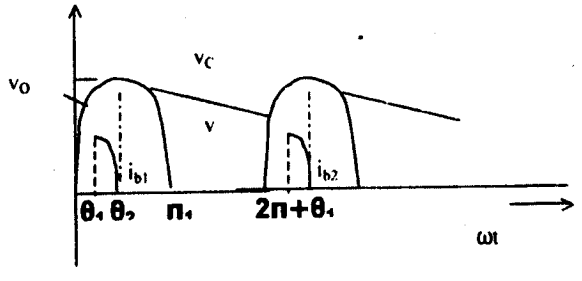


Fig: 2.1a Output wave form of a half-wave rectifier with shunt capacitance

During the first quarter cycle of ac source voltage, the diode is forward-biased, it charges the capacitor to the peak voltage V_0. Just past the peak the diode gets reverse biased and stops conducting. It is because the source is slightly less than V_0 the voltage across the capacitor. Now the voltage across the capacitor decreases exponentially due to its discharging through the load resistance R_L. The C and R_L are so chosen that the time constant ($\tau = CR_L$) is much greater than the period T of the input signal. Thus the capacitor will lose only a small part of charge, during the time diode remains reversed biased or in the off position. Therefore the fall in potential at the load will be small.

During the next positive half cycle, the diode will conduct again when the input voltage exceeds the capacitor voltage. Thus the capacitor will be recharged to the peak voltage.

The diode conduction (current flow) will be only for a short period ($\theta_1 + \theta_2$) and that too in the form of pulse and from θ_2 to ($2\pi + \theta_1$) the discharge of capacitor will take place. During this discharge the source is disconnected; so, the diode acts as an automatic switch. Thus we see that the charge lost by the capacitor during each cycle is replenished periodically by the current pulses.

During the charging interval $i_b = i_c + i_R$ and since the diode switch is closed, the supply voltage $v = V_0 \sin\omega t$, hence

$$i_b = C\frac{dv_c}{dt} + \frac{v_c}{R_L} \qquad \text{.....(2.2.1)}$$

During the conducting interval, one can assume $v_c = v = V_0 \sin\omega t$, therefore

$$i_b = \omega C V_0 \cos\omega t + (V_0 / R_L)\sin\omega t \qquad \omega t_1 < \omega t < \omega t_2$$

$$i_b = \frac{V_0}{R_L}\sqrt{(1+\omega^2 R_L^2 C^2)}\sin(\omega t + \phi) \qquad \text{where } \phi = \tan^{-1}\omega R_L C.$$

At $\omega t = \theta_2, i_b = 0$ *and we have*

$$\omega C V_0 \cos\theta_2 + (V_0 / R_L)\sin\theta_2 = 0 \quad \text{or} \quad \theta_2 = \tan^{-1}(-\omega R_L C)$$

$$\phi = \tan^{-1}(\omega R_L C) = \pi - \tan^{-1}(-\omega R_L C) = \pi - \theta_2$$

and $$i_b = \frac{V_0}{R_L}\sqrt{(1+\omega^2 R_L^2 C^2)}\sin(\omega t_2 + \omega t) \quad \omega t_1 < \omega t < \omega t_2.$$

For the period between ωt to $2\pi + \omega t_1$, the rectifier is not conducting i.e., $i_b = 0$ and solution of Eq.2.2.1 becomes

$$v_c = Ae^{-t/R_L C}$$

$\omega t = \omega t_2, v_c = V_0 \sin\omega t_2$, hence we have

$$\omega C V_0 \cos\theta_2 + (V_0 / R_L)\sin\theta_2 = 0 \quad \text{or} \quad \theta_2 = \tan^{-1}(-\omega R_L C)$$

$$\phi = \tan^{-1}(\omega R_L C) = \pi - \tan^{-1}(-\omega R_L C) = \pi - \theta_2$$

and $$i_b = \frac{V_0}{R_L}\sqrt{(1+\omega^2 R_L^2 C^2)}\sin(\omega t_2 + \omega t) \quad \omega t_1 < \omega t < \omega t_2.$$

For the period between ωt to $2\pi + \omega t_1$, the rectifier is not conducting i.e. $i_b = 0$ and solution of Eq. 2.2.1 becomes

$$v_c = Ae^{-t/R_L C}$$

At $\omega t = \omega t_2, v_c = V_0 \sin \omega t_2$, hence we have

$$v_c = V_0 \sin \omega t_2 e^{-(\omega t_1 - \omega t_2)/\omega R_L C} \qquad \omega t_2 < \omega t < (2\pi + \omega t_1)$$

At $\omega t = \omega t_1 + 2\pi, v_c = V_0 \sin \omega t_1$, hence we have

$$\sin \omega t_1 = \sin \omega t_2 e^{-(\omega t_1 + 2\pi - \omega t_2)/\omega R_L C} \qquad \text{.....(2.2.2)}$$

This relation shows that ωt_2 decreases and ωt_1 increase with $\omega R_L C$ i.e., the conduction angle is short for large values of capacitance. The dc voltage across the load can be calculated by averaging the capacitor voltage v_C over a cycle, as

$$V_{dc} = \frac{1}{2\pi}\int_{\omega t_1}^{\omega t_2} V_0 \sin \omega t \, d(\omega t) + \frac{1}{2\pi}\int_{\omega t_2}^{2\pi+\omega t_1} V_0 \sin \omega t \, e^{-(\omega t - \omega t_2)/\omega R_L C} d(\omega t)$$

After integrating and substituting the values from eqs and , we get

$$V_{dc} = \frac{V_0}{2\pi}\sqrt{(1+\omega^2 R_L^2 C^2)}\left[1 - \cos(\omega t_2 - \omega t_1)\right] \qquad \text{.....(2.2.3)}$$

This relation shows that $V_{dc} = V_0/2\pi$ for low values of capacitance and reaches to the peak value of the voltage for large values of capacitance. High value of $\omega R_L C$ is needed for a small ripple.

2.3 Full-wave rectifier with shunt capacitor filter

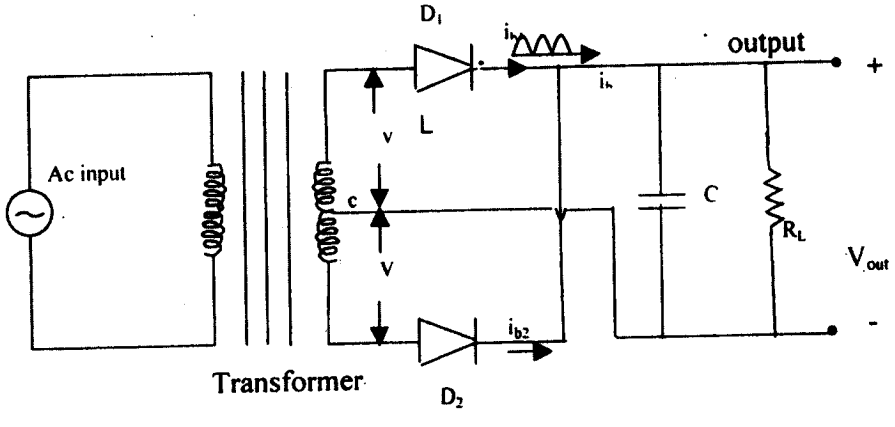


Fig.2.2 Full-wave rectifier with two diodes and with a shunt capacitance filter

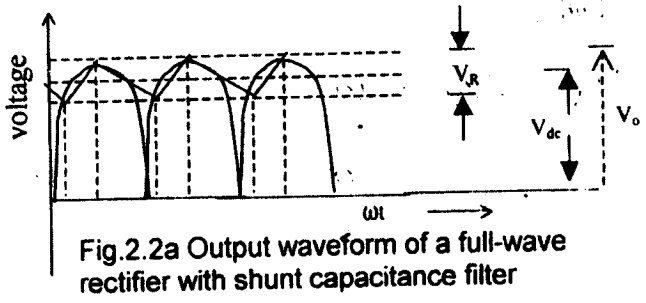


Fig.2.2a Output waveform of a full-wave rectifier with shunt capacitance filter

The operation of the full wave circuit is similar to that of the half wave circuit with the discharge time of the capacitor running only to $\pi + \omega t_1$ instead $2\pi + \omega t_1$. The cut in angle can be recalculated by the use of π in place of 2π.

$$\sin \omega t_1 = \sin \omega t_2 e^{-(\omega t_1 + 2\pi - \omega t_2)/\omega t_1 C}.$$

The dc voltage can be calculated by averaging the capacitor voltages from ωt_1 to $\pi + \omega t_1$ and noting that there are two such pulses per cycle.

$$V_{dc} = \frac{V_0}{\pi}\sqrt{(1+\omega^2 R_L^2 C^2)}\left[1 - \cos(\omega t_2 - \omega t_1)\right] \qquad (2.3.1)$$

Thus the variations in V_{dc} by the load resistance R_L are much smaller for the full-wave rectifier than for the half-wave rectifier i.e., the voltage regulation is better for the full-wave circuit.

Because of complex wave forms, the output wave is taken to be a triangular waveform for nearest approximate calculations. There are made of portions of straight lines, as shown in Fig.2.2a, peak value V_0 (maximum voltage at the capacitor). E_R is the fall in voltage across the capacitor at the load. So, the average or dc value of potential for such output is given by

$$V_{dc} = V_0 - V_R/2. \qquad (2.3.2)$$

The rms value of triangular ripple wave is given by

$$V_{rms} = V_R/2\sqrt{3}. \qquad (2.3.3)$$

i.e., the rms value of the ripple component of the triangular wave depends on the peak value (V_R) of wave and independent of slope or length of the straight lines.

I_{dc} = rate of loss of charge from capacitor = loss of charge due to a drop in potential (V_R) divided by T/2, i.e., half period

$$\therefore \quad I_{dc} = 2CV_R/T = 2C.fV_R.(as\ f\ is\ the\ frequency) \qquad (2.3.4)$$

So dc potential across the load R_L is given by

$$V_{dc} = I_{dc}R_L = 2CfV_R R_L \qquad (2.3.5)$$

The ripple factor is given as

$$r = \frac{V_{rms}}{V_{DC}} = \frac{V_R/2\sqrt{3}}{2CfV_R R_L} = \frac{1}{4\sqrt{3}fR_L C}. \qquad (2.3.6)$$

This shows that ripple factor raises inversely as time constant R_LC. Then the ripples will be smoothed when the value of C or R_L is high and shunt capacitor filter is only suitable for low output currents.

$$As \quad I_{dc} = 2CfV_R \quad or \quad V_R = I_{dc}/2Cf.$$

Therefore, the output voltage

$$V_{dc} = V_0 - I_{dc}/4Cf. \quad or \quad V_{dc} = V_0(1 + 1/4fCR_l)^{-1}$$

This relation shows that the output potential falls linearly with the increase in direct current and a simple capacitor filter will posses a poor regulation unless we have high value of the capacitor C. Thus, the regulation of series inductor is better than that of the shunt capacitor filter.

Shunt capacitor is known as a **reservoir capacitor**, **filter capacitor** or **smoothing capacitor,** is placed at the DC output of the rectifier. There will still remain an amount of AC ripple voltage and the voltage is not completely smoothed. Sizing of the capacitor represents a tradeoff. For a given load, a larger capacitor will reduce ripple but will cost more and will create higher peak currents in the transformer secondary and in the supply feeding it. In extreme cases, where many rectifiers are loaded onto a power distribution circuit, it may prove difficult for the power distribution authority to maintain a correctly shaped sinusoidal voltage curve.

2.4 Full-wave Bridge rectifier with shunt capacitance filter

For many applications, especially with single phase AC, where the full-wave bridge serves to convert an AC input into a DC output, the addition of a capacitor may be important because the bridge alone supplies an output voltage of fixed polarity but pulsating magnitude

The function of this capacitor, known as a reservoir capacitor is to lessen the variation in (or 'smooth') the rectified AC output voltage waveform from the bridge. One explanation of 'smoothing' is that the capacitor provides a low impedance path to the AC component of the output, reducing the AC voltage across, and AC current through, the resistive load. In less technical terms, any drop in the output voltage and current of the bridge tends to be cancelled by loss of charge in the capacitor. This charge flows out as additional current through the load. Thus the change of load current and voltage is reduced relative to what would occur without the capacitor. Increases of voltage correspondingly store excess charge in the capacitor, thus moderating the change in output voltage / current.

The idealized waveforms shown above are seen for both voltage and current when the load on the bridge is resistive. When the load includes a smoothing capacitor, both the voltage and the current waveforms will be greatly changed.

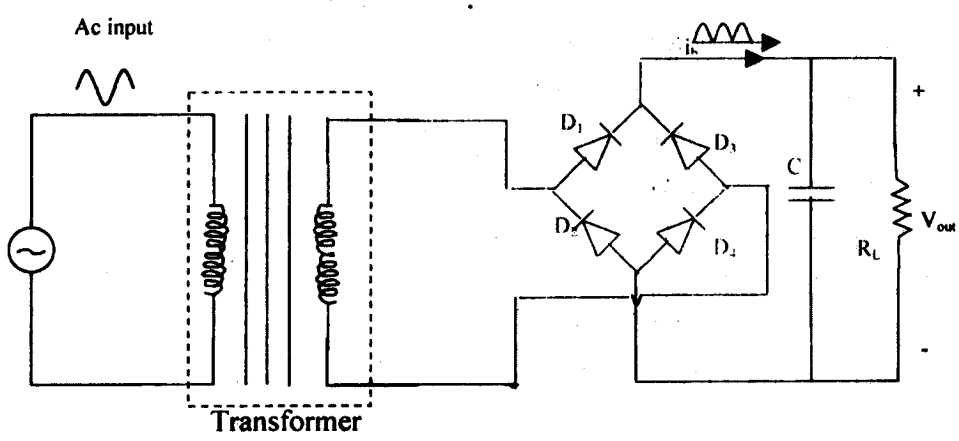


Fig.2.3 Full-wave bridge rectifier

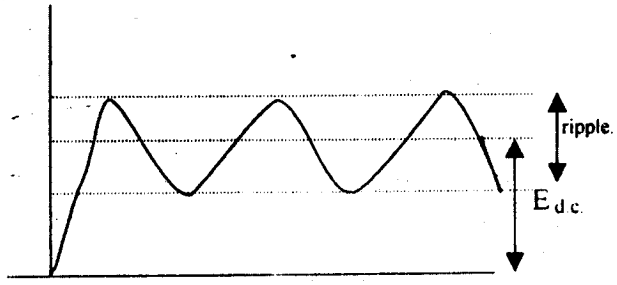


Fig.2.3(b) The effect of capacitance on full wave rectifier output

While the voltage is smoothed, as described above, current will flow through the bridge only during the time when the input voltage is greater than the capacitor voltage. For example, if the load draws an average current of n Amps, and the diodes conduct for 10% of the time, the average diode current during conduction must be 10n Amps. This non-sinusoidal current leads to harmonic distortion and a poor power factor in the AC supply.

In a practical circuit, when a capacitor is directly connected to the output of a bridge, the bridge diodes must be sized to withstand the current surge that occurs when the power is turned on at the peak of the AC voltage and the capacitor is fully discharged. Sometimes a small series resistor is included before the capacitor to limit this current, though in most applications the power supply transformer's resistance is already sufficient.

Precautions to be taken in using a D.C. Power supply with shunt capacitance filter:

The simplified circuit shown in Fig.2.3 has a well deserved reputation for being dangerous, because, in some applications, the capacitor can retain a *lethal* charge

after the AC power source is removed. If supplying a dangerous voltage, a practical circuit should include a reliable way to safely discharge the capacitor. If the normal load can not be guaranteed to perform this function, perhaps because it can be disconnected, the circuit should include a bleeder resistor connected as close as practical across the capacitor. This resistor should consume a current large enough to discharge the capacitor in a reasonable time, but small enough to minimize unnecessary power waste.

Because a bleeder sets a minimum current drain, the regulation of the circuit, defined as percentage voltage change from minimum to maximum load, is improved. However in many cases the improvement is of insignificant magnitude.

The capacitor and the load resistance have a typical time constant T = *RC* where *C* and *R* are the capacitance and load resistance respectively. As long as the load resistor is large enough so that this time constant is much longer than the time of one ripple cycle, the above configuration will produce a smoothed DC voltage across the load.

In some designs, a series resistor at the load side of the capacitor is added. The smoothing can then be improved by adding additional stages of capacitor–resistor pairs, often done only for sub-supplies to critical high-gain circuits that tend to be sensitive to supply voltage noise.

In a practical circuit, when a capacitor is directly connected to the output of a bridge, the bridge diodes must be sized to withstand the current surge that occurs when the power is turned on at the peak of the AC voltage and the capacitor is fully discharged. Sometimes a small series resistor is included before the capacitor to limit this current, though in most applications the power supply transformer's resistance is already sufficient.

2.5 Half-wave rectifier with Series inductance filter

A filter circuit can also be formed by connecting a choke (inductor) in series with the load R_L. The inductance (L) of choke is quite high than its resistance (r_L). In order to maintain a high value of L for a wide variation in current flow, some chokes use an iron core with a small air gap to prevent saturation. The inductor offers a high series impedance $Z = r_L^2 + \omega^2 L^2$ in path of ac or harmonic components and opposes any change of current passing through it. Actually an inductor stores the energy in the form of magnetic filed when the current raises from the average value and thus reduces the ripples from the output. The Fig.2.4a shows the circuit diagrams of a half-wave with the series inductor filter.

If $v = V_0 \sin\omega t$ is the applied input at the diode, the output without filter will be as shown by dotted curves. In the case of half-wave rectifier with series inductor, the growth of current exists from 0 to $\pi/2$ part of the output which is opposed by the inductance coil and from $\pi/2$ to 0 there is a fall in current which is not allowed by the coil

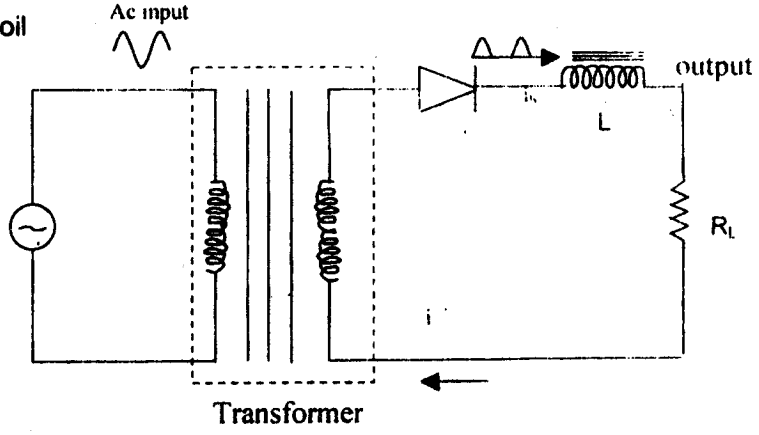


Fig 2.4a Half-wave rectifier with series inductance filter

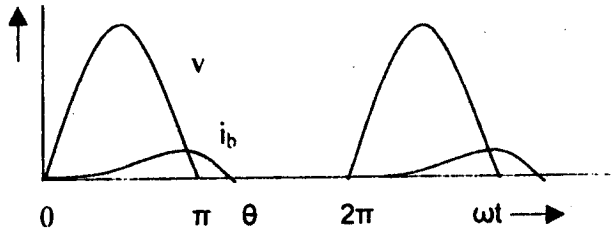


Fig.2.4b Wave shape of the output voltage and current in a half-wave rectifier with series Inductance filter

So period of the current conduction is increased from 0 to π to 0 to $(\pi+\theta_2)$. θ_2 is known as *cut-off angle* and its value increase with the increase in L. Thus the gap of π to 2π part of the cycle in the output has been filled to some extent by introducing a series inductor in the circuit due to the induced e.m.f.

2.6 Full-wave rectifier (with two diodes and) with series inductance filter

In the case of full-wave rectifier, the period of conduction in the second rectifier will start before the current in first has ceased. Thus the currents through the

inductor and load resistance never drops to zero, as shown by continuous curve in Fig.2.5(b)

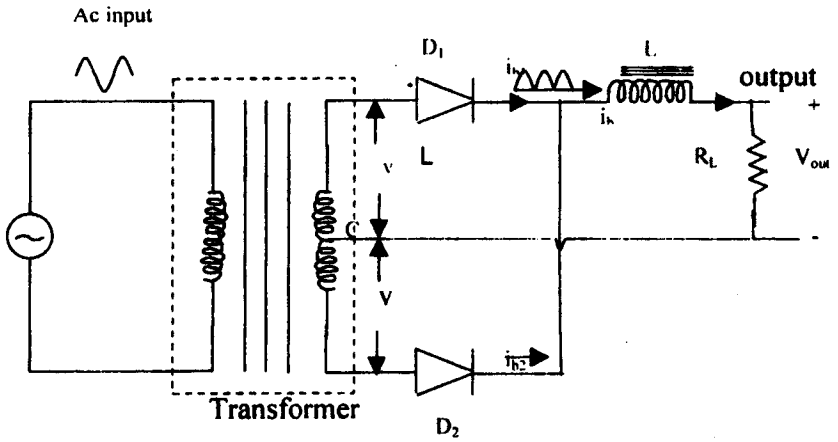


Fig.2.5a Full-wave rectifier (with two diodes) with series Inductance filter

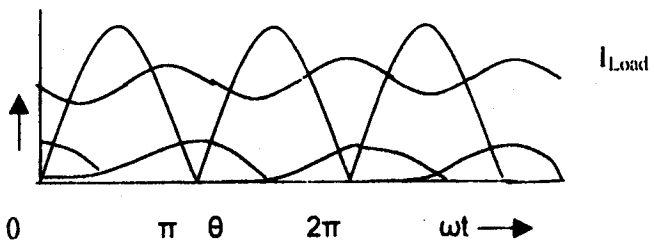


Fig.2.5b Wave shape of the output voltage and current in a full-wave rectifier with series Inductance filter

dc output. Fourier analysis of the output waveform for full-wave rectifier is given by

$$v = \frac{2V_0}{\pi}\left[1 - \frac{2}{3}\cos 2\omega t - \frac{2}{15}\cos 4\omega t \ldots\ldots\ldots\right] \qquad (2.6.1)$$

The first term is the dc component of the input filter voltage.

Assume that R_S the resistance of the secondary of transformer and R_f the dynamic forward resistance of each diode are negligible. If r_L be the resistance of inductor (or choke) and R_L is load resistance, then the (dc) current through and voltage across the load can be given as

$$I_{dc} = \frac{2V_0}{\pi(r_f + R_l)} = \frac{2V_0}{\pi(R_l)}, (\text{If } r_L << R_L) \qquad (2.6.2)$$

$$\text{and} \quad V_{dc} = I_{dc}R_L = \frac{2V_0 R_L}{\pi(r_L + R_l)} = \frac{2V_0}{\pi} = 0.637V_0, (\text{If } r_L << R_L)$$

As r_L will always be quite small than the load resistance R_L,

$$\therefore \quad V_{dc} = \frac{2V_0}{\pi}\left(1 + \frac{r_L}{R_L}\right)^{-1} = \frac{2V_0}{\pi}\left(1 - \frac{r_L}{R_L}\right) \qquad (2.6.3)$$

$$= \frac{2V_0}{\pi} - \frac{2V_0 r_L}{\pi(R_L)} = \frac{2V_0}{\pi} - I_{dc}r_L$$

Voltage regulation: when there is no load I_{dc} is zero, and $(V_{dc})_{\text{no load}} = 2V_0/\pi$, therefore the voltage regulation.

$$V.R. = \frac{(V_{dc})_{\text{no load}} - (V_{dc})_{\text{full load}}}{(V_{dc})_{\text{full load}}} = \frac{(I_{dc})r_L}{[(2V_0/\pi) - (I_{dc})r_L]} \qquad (2.6.4)$$

As the inductor (or choke) resistance is quite small, hence the regulation factor is also reduced, which means a better regulation.

Ripple factor: As the amplitudes of the higher harmonic terms are very small, hence their effects for producing ripple will also be very small, so only first ac component, i.e., $(2V_0/\pi)(\square \cos 2\omega t)$ is used for calculation of ripple factor. While neglecting higher harmonic terms, we have considered that the impedance due to inductance at high frequencies was also high and thus there was a better filtration for these terms. From the elementary circuit theory we can write the alternating current through the load resistance R_L as

$$I_{ac} = \frac{4V_0}{3\pi} \cdot \frac{\cos(2\omega t - \phi)}{[R_1^2 + (2\omega L)^2]^{1/2}} \qquad (2.6.5)$$

Where $R_1 = (r_L + R_L)$ and $\phi = \tan^{-1}(2\omega L / R_1)$. This is the angle by which the current lags behind the alternating voltage.

Thus the effective or rms value of ac at the output can be written as

$$I_{rms} = \frac{4V_0}{3\pi\sqrt{2}[R_1^2 + (2\omega L)^2]^{1/2}},$$

Hence ripple factor $r = I_{rms} / I_{dc}$

$$= \left[\frac{4V_0}{3\pi\sqrt{2}[R_1^2 + (2\omega L)^2]^{1/2}}\right]\left(\frac{2V_0}{\pi R_1}\right)^{-1}$$

$$= \frac{\sqrt{2}}{3\pi} \frac{1}{\sqrt{\left[1 + \left\{2\omega L/(r_l + R_l)\right\}^2\right]}} \qquad (2.6.6)$$

From this equation, we have

1. If $(r_L+R_L)>>2\omega L$, the ratio $2\omega L/(r_L+R_L)$ can be neglected in comparison to1, so $r = \wp/3=0.471$, it was 0.48 for without filter, so under such a condition the filtering is poor.
2. if $2\omega L >>(r_L+R_L)$, so 1 can be neglected in comparison to the ratio $(2\omega L/R_1)^2$ in the denominator, so

$$r = \frac{\sqrt{2}}{3\pi} \frac{(r_l + R_l)}{2\omega L} = 0.236 \frac{(r_l + R_l)}{\omega L} \qquad (2.6.7)$$

This shows that r can be decreased by using a choke coil with high inductance and low resistance. Being ω in the denominator, the higher frequencies will have less ripple factor. The ripple factor decreases as we decrease R_L or increase load current.

2.7 Full-wave rectifier (with two diodes and) with L-section series inductance filter:

The L-section or Inductor input Filter: This type of filter is the combination of Series Inductor and the shunt capacitor filters. It gives very low value of ripples at all loads and hence used frequently in the electronic equipments. The circuit for full wave L-section filter is shown in Fig.2.6a

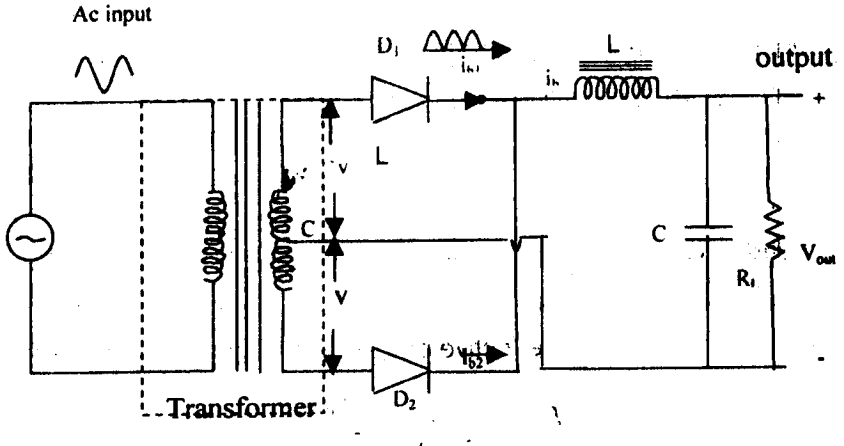


Fig 2.6a: Full-wave rectifier with two diodes with L-section filter

The Inductor L offers a high impedance to the ac or harmonic components and thus reduces there components from the output. The shunt capacitor bypasses the ac

components around the load. Thus the ripples in output are reduced considerably. The dc voltage and ripple factor may be calculated by taking the first two terms in the Fourier series representation of the output voltage of full-wave rectifier as

$$v = \left(\frac{2V_0}{\pi}\right) - \left(\frac{4V_0}{3\pi}\right)\cos 2\omega t \,. \qquad (2.7.1)$$

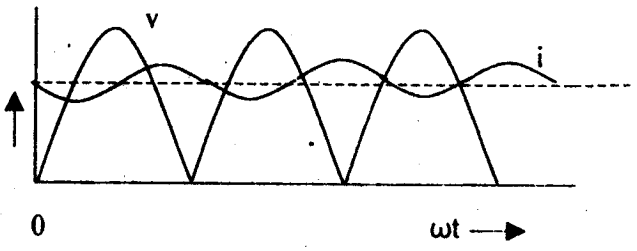


Fig.2.6b Wave shape of the output voltage and current in a full wave rectifier with series Inductance filter

It is equivalent to a **dc source** in series with an ac source having twice the power line frequency. It the sum of the resistances of diode, secondary of transformer, choke is negligible and the load resistance is R_L then

$$V_{dc} = \frac{V_0}{\pi} - I_{dc}R_L \,. \qquad (2.7.2)$$

The values of X_L and X_C at second harmonic of supply frequency (i.e., for a supply frequency ω) are 2ωL and 1/2ωC respectively. The Input impedance of the filter circuit at the second harmonic frequency 2ω is

$$Z_2 = 2j\omega L - \frac{jR_L 2\omega C}{R_L - j/2\omega C} \quad OR \quad |Z_2| = \left(4\omega^2 LC - 1\right)/2\omega C$$

The second harmonic e.m.f allows the ac current in the inductor L, given as

$$(I_L)_{rms} = \frac{4V_0}{3\sqrt{2\pi}} \cdot \frac{1}{Z_2} = \frac{8\omega C V_0}{3\pi\sqrt{2}\left(4\omega^2 LC - 1\right)} \,. \qquad (2.7.3)$$

If we assume that the entire as passes through the capacitor then $I_C \approx I_L$ where I_C and I_L are alternating currents through C and L respectively. Thus the ac potential across the load (ripple potential) is the potential across the capacitor and is given by

$$V_{rms}' = \frac{(I_C)_{rms}}{2\omega C} = \frac{(I_L)_{rms}}{2\omega C} = \frac{4V_0}{3\pi\sqrt{2}\left(4\omega^2 LC - 1\right)} \,.$$

$$\therefore \quad Ripple\ factor\ r = \frac{V_{rms}'}{V_{dc}} = \left(\frac{4V_0}{3\pi\sqrt{2}(4\omega^2 LC)}\right)/(2V_0/\pi)$$

$$= 0.47/\left(4\omega^2 LC - 1\right) \qquad (2.7.4)$$

Sine the Inductor filter has low ripple on heavy loads and the capacitor filter has low ripple on light loads, hence it is reasonable to assume that the Inductor input filter has suitable characteristics at all loads. For light loads $(R_L = \infty)$, the capacitor charges to the peak voltage with the dc output V_0. As R_L is decreased, the diode switches the supply voltage on to the filter and capacitor C is charged to the peak. The dc voltage will be lowered. The diode action is as for the shunt capacitor filter. As the load current is further increased, the discharge of the capacitor is more rapid and the effect of the inductor is appreciable. The upper part of Fig.2.62 shows the variation in V_{dc} with I_{dc}. Here current I_K indicates the point at which continuity of load current is obtained and then filter begins to act more like an inductor filter and less a shunt capacitor filter, because of good regulation at the higher load currents. The lower part of Fig.2.62 shows the output current for L-section filter.

To determine I_K, let us equate the current I_{dc} and peak-second harmonic current I_2 as

$$(2V_0/\pi)/R_L = (4V_0/3\pi)/Z_2.$$

It gives $R_L=1.5Z_2$, i.e., the current in the input inductor becomes continuous and the output voltage levels off at a load having resistance equal to 1.5 time harmonic impedance of the filter circuit. Thus the critical value of the inductor input

$$L_K = Z_2/2\omega = R_L/3\omega \quad \therefore \quad I_K = 2V_0/\pi R_L = 2V_0/3\pi\omega L_K$$

The value of ripple may be further reduced by adding more stages of L-sections. Each section reduces the ripple factor $1/(4\omega^2 LC + 1)$. The two stages L-section filter circuit is shown in fig.2.7

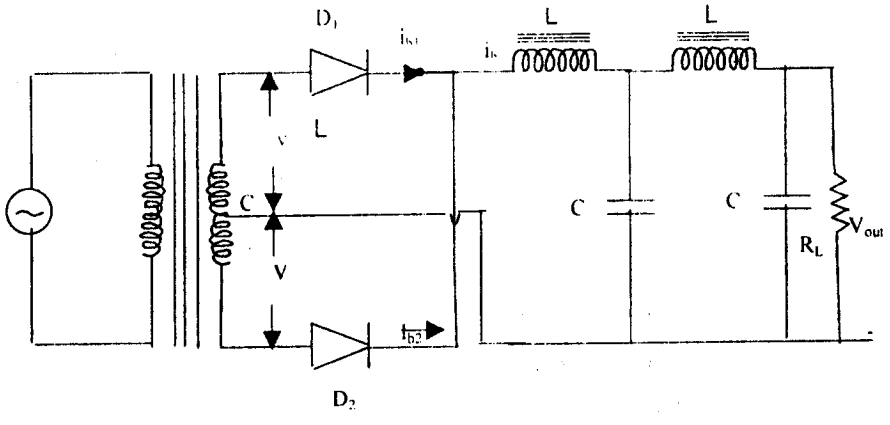


Fig.2.7 Full-wave rectifier with two L-section filters

Output can also be smoothed using a choke and second capacitor. The choke tends to keep the current (rather than the voltage) more constant. Due to the relatively high

cost of an effective choke compared to a resistor and capacitor this is not employed in modern equipment.

Some early console radios created the speaker's constant field with the current from the high voltage ("B +") power supply, which was then routed to the consuming circuits, (permanent magnets were then too weak for good performance) to create the speaker's constant magnetic field. The speaker field coil thus performed 2 jobs in one: it acted as a choke, filtering the power supply, and it produced the magnetic field to operate the speaker.

2.8 Π-section filter or capacitor input filter

For providing smooth output voltage, an input C_1 is added to L-section filter; it forms a Π -shaped filter. A full-wave rectifier with Π-section is shown in Fig.2.8 The rectifier feeds directly into the capacitor C_1. The triangular output potential wave from this capacitor is fed into the L-section filter which will further reduce the ripple component. Therefore the filter is also known as capacitor input filter.

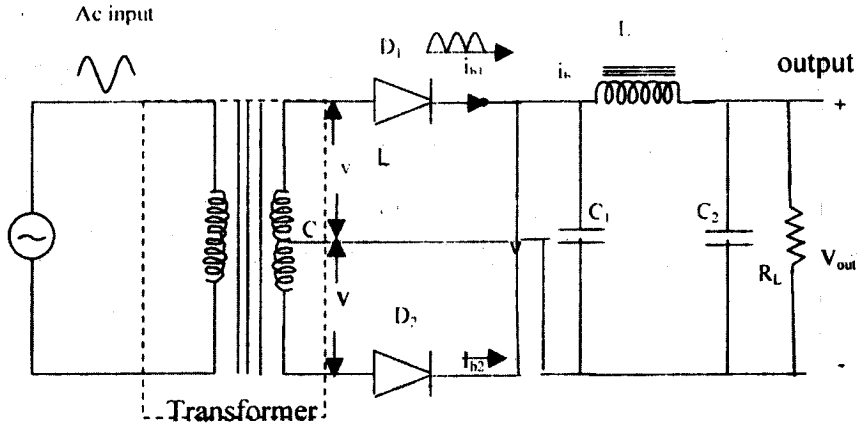


Fig.2.8 Full-wave rectifier with two diodes and with π –section capacitance input filter

Capacitor C_1 draws a charging current pulse and charged the peak value V_0 of the input voltage. It then discharges through the inductor L and load R_L and the inductor serves to maintain an almost constant discharge current. During the time in which the capacitor voltage reaches to an appropriate value, the second diode start conducting and thus the capacitor is recharged. The discharge current of C_1 is difficult to evaluate. If r_L is the resistance of the inductor and I_{dc} is the dc component of the current in it the output potential may be assumed approximately as that from the capacitor C_1 decreased by the I_{dc} r_L drop in the inductor.

$$V_{dc} = V_0 - V_R/2 - I_{dc} r_L$$

$$= V_t - I_{dc}(r_f + 1/4fC_1)$$

Using $V_{dc} = I_{dc}R_L$, we get

$$V_{dc} = \frac{V_t}{1 + (1/4fC_1R_L) + r_f/R_L} \qquad (2.8.1)$$

This relation shows that the regulation is good for higher values of C_1. We know that for the filter connected to a rectifier at the source frequency ω, the important ripple term is of second harmonic frequency. It is reasonable to neglect all harmonic except the second as their contributions are very small. This voltage is applied across L-C_2 filter. Generally the capacitive reactance $1/\omega C_2$ is made small compared with the load resistance R_L to prevent cyclic charges in output current from affecting the output voltage. $2\omega L$ is made large compared with $1/2\omega C_2$ to provide a large reduction in the ripple components of voltage. Thus

$$2\omega L >> 1/2\omega C_2 << R_L$$

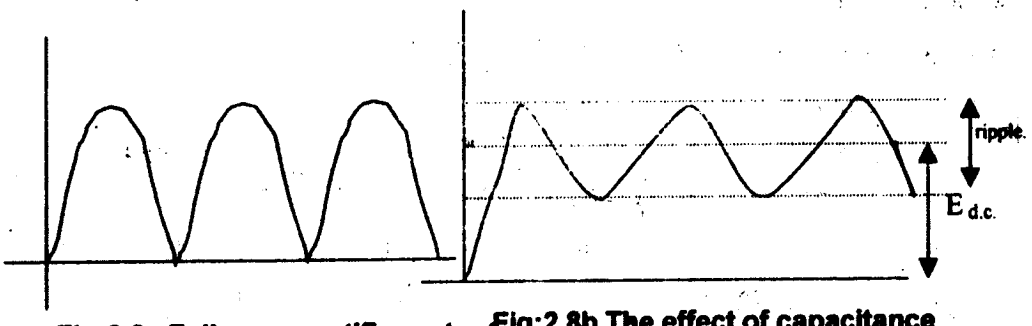


Fig:2.8a Full wave rectifier output **Fig:2.8b The effect of capacitance on full wave rectifier output**

From the theory of shunt capacitor filter, the ac-component across the capacitor C_1 is the root mean square value if the triangular ripple wave and is given by

$$V_1 = V_{rms} = V_R / 2\sqrt{3} = \pi I_{dc} / 2\sqrt{3}\omega C_1$$

The reactance of C_2 is made small with respect to load R_L. With the use of voltage division method, the ripple voltage across C_2 or across R_L is

$$V_2 = V'_{rms} = \frac{-V_R}{2\sqrt{3}} \times \frac{j/2\omega C_2}{j2\omega L - j/2\omega C_2} = \frac{V_R}{2\sqrt{3}} \frac{1}{4\omega^2 LC_2 - 1}$$

$$= \frac{I_{dc}}{4\sqrt{3}fC_1} \frac{1}{4\omega^2 LC_2 - 1} = \frac{I_{dc}\pi}{2\sqrt{3}\omega C_1(4\omega^2 LC_2 - 1)}$$

$$Ripple\ factor\ r = \frac{V'_{rms}}{V_{dc}} = \frac{\pi}{2\sqrt{3}\omega R_L C_1(4\omega^2 LC_2 - 1)}. \qquad (2.8.2)$$

With L and C_2 large, we have $4\omega^2 LC_2 >> 1$, thus the ripple factor across the load may be written as

$$r = \frac{\pi}{8\sqrt{3}\omega^3 LC_1C_2R_l} = \frac{0.216}{\omega^3 LC_1C_2R_l} = \frac{0.216}{R_l}.\frac{X_{c1}X_{c2}}{X_l}. \quad (2.8.3)$$

where the reactances are calculated at the supply frequency. Since $r\alpha 1/R_l$, the ripple increases with load current.

2.9 SUMMARY

One of the important uses of filter circuits is in Rectifier circuits. Rectifier circuits provide pure D.C. voltages and currents by rectifying the alternating voltages. However, their output contains D.C. component and A.C components. The A.C components are called *ripple* and have frequency components at the input A.C frequency (in India the power line frequency is 50Hz) and its harmonics. As such the unregulated rectifier is not fit for using it as a D.C. power supply. The unwanted ripple must be removed. A capacitance placed across the rectifier circuit comes in shunt with the input resistance of the device to which the rectifier circuit is connected to power it. The input resistance of the device and the capacitance connected across it form an RC filter. The value of capacitance is selected such that its reactance at the fundamental frequency of the input A.C. source is zero. The A.C ripple gets filtered out and only D.C. voltage appears across the load resistance. An inductance placed in series with load resistance form an LR-filter. A large value of inductance (in Henries) is used for this. The reactance of the inductor is so large such that ripple voltage drops across it and will not appear at the output. As the cost of inductor is high, sometime in low cost circuits, a resistor is used instead of an inductor. However, a resistor drops both A.C and D.C voltages. The series resistor drops some D.C. voltage and hence the D.C. voltage will be less than the required value for load. The heat generated may affect the performance of other components in the circuit. The RC and LC-filters are used to remove these A.C components. A resistance or inductance is used in series and the capacitance will be in shunt. These series inductance or resistance value is so selected such that it offers maximum resistance to A.C or ripple component. The shunt capacitance is so selected such that it offers zero resistance to A.C. components, so that the ripple component is bypassed and it will not appear at the output. The series resistance (or inductance) and *shunt capacitance filter* is called *an L-section filter* because of the appearance like English alphabet "L",

Two L-sections are connected to form a π- section filter. It can be shown that the π-section filter can more effectively remove ripple than single L-section filter. The performance of a filter to reduce ripple is measured by ripple factor, which is the ratio of the ripple output voltage to the D.C. voltage. LC filters are costlier to fabricate than RC filters, however very low D.C. resistance of inductances helps us in avoiding large D.C. voltage drops which otherwise occur if we use RC filter. Further, it can be shown that unlike RC-filter, an LC-filter ripple is independent of load resistance. When we use LR and LC-filters, the surge voltages produced during on and off of the circuit will be large and we have to use components which can withstand these voltages. The iron core inductors are not suitable for higher frequencies, as losses will be more. As load current increases, the D.C. output voltage of the filter decreases. The variation is more in capacitance input filters (Π-filters) when compared to Choke input filters (LC-filters). The steadiness of output D.C.voltage is expressed in terms of a parameter called *voltage regulation* which is defined as the ratio of the change in voltage with respect to no load voltage to the output voltage at maximum current drawn.

2.10. Key Terminology

Low-pass filter: A low –pass filter allows to pass through it frequencies below a cut-off frequency. Above this frequency, all the frequencies are heavily attenuated.

Phase angle: A sinusoidal wave changes its phase angle from 0 to 2π radians or 0 to 360^0 as it completes one cycle. In the first half cycle, the phase change will be from 0 to π.

Biasing a diode. Keeping a potential difference between anode (p-) and cathode (n-). If the anode is more positive than cathode, a diode gets forward biased. Under this bias, its resistance becomes very low and allows current to pass through. When the diode is reverse biased, i.e. if anode is negative with respect to cathode, no majority carrier current passes through it. It offers very high resistance and only minority carrier current, in micro or nano amperes, flows.

Peak value, average value, and rms values of a signal.

Peak value (positive) is the maximum positive value attained by the signal in a cycle. A sinusoidal signal reaches positive peak and a very low negative value in a cycle. The lowest value achieved in a negative part of the cycle is called a negative peak. For a sinusoidal signal, negative and positive peaks will have same magnitude. In a cycle. For every positive value of the sine wave there will be an exactly equal negative value, so that, the average value of a sinusoidal signal over a cycle or 2π is zero. So instead of taking simple average, square root of the sum of squares of the

sine function is defined, and this is called root mean square value or simply r.m.s. value. It is the value, we get when an ac signal value is measured on a multimeter in a.c setting.

2.11 Self assessment Questions

Long answer Questions

1. Explain the working of an unregulated power supply with shunt capacitor filter.
2. What are the problems associated with such a power supply.
3. Explain the working of a choke input filter. Compare its performance with a shunt capacitor filter.
4. What is an L- section filter. Explain the working of an unregulated power supply with an L-section filter.
5. Explain the role of a π filter in removing ripple in an unregulated power supply with a π filter.
6. Draw the circuit diagram of a full-wave rectifier with π filter. Can we replace the choke with a resistor and yet obtain the filter action?
7. Derive expressions for the ripple factor, V_{DC}, and rectifier efficiency of a full-wave rectifier with choke input filter.
8. Derive expressions for the ripple factor, V_{DC}, and rectifier efficiency of a full-wave rectifier with shunt capacitor filter.
9. Derive expressions for the ripple factor, V_{DC}, and rectifier efficiency of a full-wave rectifier with a π filter.

Short answer questions

1. Explain about π - section filter.
2. Write notes on various smoothing filters
3. Explain with diagrams, the changes that occur when a shunt capacitor is added across a full-wave rectifier.
4. Compare a full-wave rectifier with two diodes with that of a full-wave bridge rectifier with same type of filter.

2.12 TEXT AND REFERENCE BOOKS

1. Integrated Electronics by Millman and Halkias
2. Basic Electronics and Linear Circuits - Bhargava etc

REFERENCE BOOKS

1. A text lab manual in Electronics by ZBAR (Tata Mc graw Hill)
2. Electronics fundamentals by JD Ryder
3. Electronic Devices and Circuits by Samuel Seely.

REGULATED D.C. POWER SUPPLIES

OBJECTIVES OF THE LESSON: To learn about Zener stabilized power supply and Series regulated Transistor power supply.

STRUCTURE OF THE LESSON

3.1 INTRODUCTION:

In the lessons 1 and 2 of this unit, we studied about the various types of rectifiers and how their output can be made to contain only D.C. Voltage. These unregulated power supplies will not give constant D.C. output if load current increases or in put mains voltages changes from 230V A.C. However there is need to keep the output D.C. voltage of a power supply constant irrespective of the above mentioned variations in load current and mains voltage. In this lesson we learn about these techniques.

3.2 THE POWER SUPPLY (UNREGULATED)

The power supply unit is an essential type of radio and electronic equipment, as it supplies voltages and currents to various components of the circuit. It consists of four units, namely, transformer, rectifier, filter and voltage divider. The values of output voltage and current required will determine the rating of transformer and the type of the rectifier to be used. The percentage of ripple voltage allowable will determine the type of the filter circuit and it components.

The circuit diagram of power supply unit with Π-section filter is shown in Fig.3.1 The voltage regulation can be calculated by measuring the voltage at no load and different loads. It can be shown that the voltage regulation will be better if an L-section filter is also added to the Π section filter.. It can be seen that the ripple percentage varies directly as the load current and inversely as the load resistance.

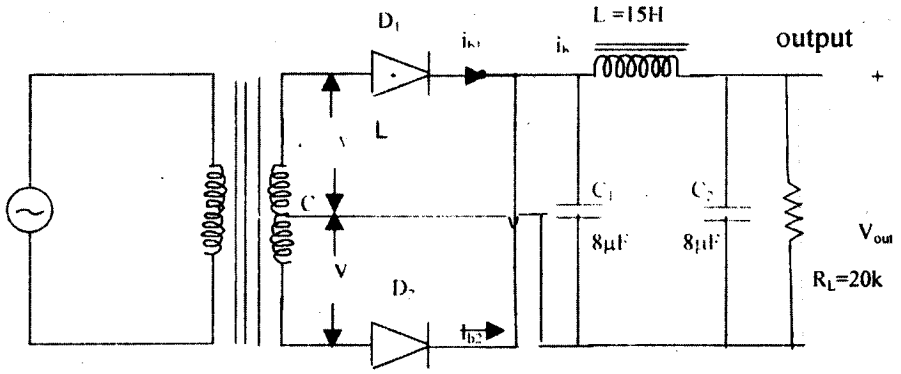


Fig 3.1: Unregulated D.C. Power supply

Circuit components

1. Potential source: A.C. supply is generally used as potential source or the input of the power supply unit.
2. Transformer: A step-down transformer with low resistance of its secondary and negligible leakage reactance is used. For a full wave circuit, the transformer secondary must have centre tap. Owing to the effect of leakage, the secondary diode may conduct before the first ceases with an overlap of the current of voltage.
3. Rectifier circuits: The rectifier circuit may be either of half wave or full wave type. The latter may use either two diodes (centre tap rectifier) or four diodes (bridge type rectifier).
4. Filter circuit : The full wave rectifier does not provide ripple free dc voltage. The various types of filter or smoothing circuits are used, depending upon the requirement of the output.
5. Load : A non inductive high resistance is used as a load. The output of the power supply is taken across this load.

Characteristics of a power supply:

The quality of a power supply depends on the following terms.

a) Load regulation – The load regulation, also called load effect, is defined as the charge in the output voltage for a change in load current from the minimum to the maximum values.

Load regulation (L.R.) = $(V_{no\ load} - V_{full\ load}) / V_{no\ load}$

$$\% L.R. = \frac{V_{NL} - V_{FL}}{V_{NL}} \times 100, \qquad (3.1)$$

Where V_{NL} is the load voltage with no load current and V_{FL} is the load voltage with full load current.

b) Source regulation- the Source regulation, also called loads effect or line regulation is the change in the load voltage for the specific range of line voltage.

Source regulation (S.R.) = load voltage charge

$$\%S.R = \frac{change\ in\ load\ voltage}{norinal\ load\ voltage} \times 100 \qquad (3.2)$$

c) Ripple Rejection:- The filter circuit reduces the ripples from the output of the rectifier. The voltage regulators are used in regulated power supplies to attenuate the ripple. The Ripple Rejection (RR) is usually specified in decibels.

An RR of 80 dB means that the output ripple is 80dB less than the input ripple,

i.e., output ripple is 10^4 times smaller than the input ripple.

d) Rectification Efficiency: - the rectification efficiency is defined as the ratio of the dc power delivered to the load to the total input ac power.

Rectification Efficiency (R.E) = P_{DC} / P_{AC}.

3.3 REGULATED POWER SUPPLY

The dc output voltage of the power supply is not constant but fluctuates with variations in the load. The fluctuation in the output is measured in terms of voltage regulation which is usually expressed as:

$$\%\ Voltage\ \text{Re}gulation = \frac{V_{no\ load} - V_{full\ load}}{V_{full\ load}} \times 100. \qquad (3.3)$$

The dc output voltage also varies directly as the ac input voltage to the rectifier. When Zener diodes are used in power supplies with a series resistor, output voltage is constant for both input or load changes and is thus called regulator. Zener diode is therefore called voltage regulator and the whole arrangement the regulated power supply. The voltage regulators reduce the ripple on the output. Let us discuss in brief both devices of regulation:

3.3.1 Voltage regulations by Zener diode: Zener diodes can regulate the voltages from about 2 to 200 volts. Some of these diodes have a power dissipation of 50 (or more) Watts.

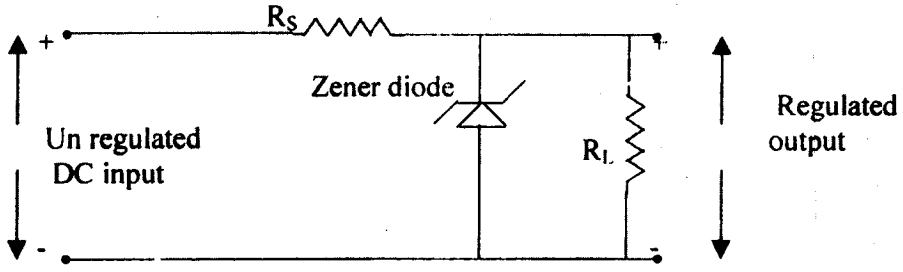


Fig 3.2 voltage regulation with Zener diode

The circuit employing a Zener diode as a voltage regulator is shown in Fig 3.2 . It is to be noted that the Zener diode is connected in the reverse direction i.e., reverse biased. The regulated output voltage is obtained across the Zener to which the load R_L is connected. In the reverse breakdown region of the Zener diode, increasing the reverse voltage across the Zener increases the number of carriers produced by the break of covalent bonds, which reduces the diode resistance. Decreasing the reverse voltage reduces the number of carriers and thus increases the diode resistance.

Let V_{dc} be the unregulated dc input voltage applied across the series combination of resistor R_S and Zener diode. The regulated output voltage V_{out} is the voltage across the load resistance R_L connected across the Zener diode. The voltage across the Zener is very close to $V_{out} = V_L$ Let I be the total current drawn from the supply (or voltage input), I_Z the current flowing through Zener and I_L the current through the load R_L. Therefore

$I = I_Z + I_L$ and $I_Z = V_L/R_L$.

Applying Kirchoff's second law to the left part of the circuit (Fig.3.2), we get

$$V_{dc} = R_S I + R_Z I_Z ,$$

Where R_Z is the dc-resistance of the Zener diode, since $V_L = I_L R_Z = I_Z R_Z$, therefore, we get

$$V_{dc} = R_S(I_Z + I_L) + I_L R_L = R_S I_Z + I_L(R_S + R_L)$$

$$= R_S I_Z + V_L(1 + R_S / R_L). \qquad (3.4)$$

This equation relates the current and voltage drop in the Zener diode. Let us explain the voltage regulation in the Zener diode:

Equation 3.4 is the equation of a straight line and is called the load line. For a given load R_L, the intersection of the load line AB with the Zener characteristic gives the operating point P of the Zener diode (see Fig.3.3). If the load is increased (R_L

decreased), I_L, increased and I_Z decreases. For this new load, AB' will be the new load line and P' the operating point. As is clear from the figure, though the change in current though Zener diode is large ($I_Z + I'_Z$), but change in the voltage drop across the Zener is very small. The voltage drop remain almost constant at V_Z (as the curve is almost a vertical line). Thus the voltage drop across the Zener is independent of fluctuations in the load resistance R_L.

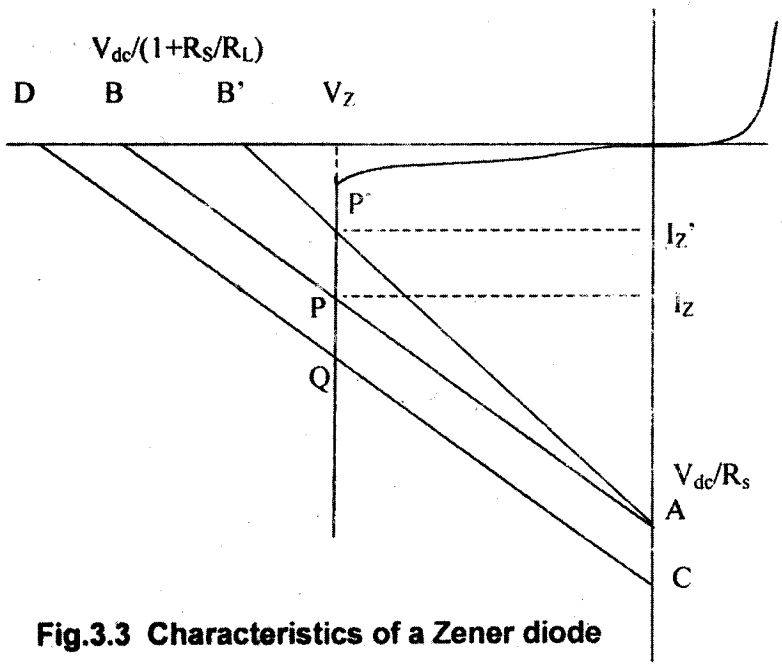


Fig.3.3 Characteristics of a Zener diode

Let us assume that R_L remains fixed, and the fluctuations are in the input voltage V_{dc} is increased, I and I_Z will increase. The load line thus shifts to a new position CD with the corresponding operating point at Q. Though the current through the Zener increases, but the voltage drop across the Zener remains almost the same at V_Z Thus the voltage drop across the Zener is practically independent of fluctuations in the input voltage and the Zener diodes regulate the rectifier voltages.

POWER SUPPLY PERFORMANCE:

Source Effect

The ac supply to the input of a transformer in a dc power supply does not always remain constant. A ± 10% variation in the ac source voltage (V_S) (also termed line voltage) is not unusual. When the source voltage varies, there is some variation in the output voltage from supply; this output voltage change (ΔV_0) due to a change in the input is termed the source effect. In the output varies by100 mV when the source

voltage changes by ±10%, the source effect is 100 mV. an alternative way of stating this output voltage (V_0). In this case, the term line regulation is used.

$$Source\ effect \quad \Delta V_0 \ for\ a\ 10\%\ change\ in\ V_S$$

$$Line\ \text{Re}gulation = \frac{(\Delta V_0 \ for\ a\ 10\%\ change\ in\ V_S) \times 100\%}{V_0} \qquad (3.5)$$

Load Effect

Power supply output voltage is also affected by changes in load current (I_L). The output voltage decreases when I_L is increased, and rises when I_L is reduced. The load effect defines how the output voltage changes when the load current is increased from zero to its specified maximum level ($I_{L(max)}$). If the load current effect is 100mV. as for the source effect, the load effect can also be expressed as percentage of the output voltage. This is termed the load regulation.

$$Load\ Effect = \Delta V_0 \ for\ \Delta I_{L(max)}$$

$$Load\ \text{Re}gulation = \frac{(\Delta V_0 \ for\ \Delta I_{L(max)}) \times 100\%}{V_0} \qquad (3.6)$$

The performance of a Zener diode voltage regulator may be expressed in terms of the source and load effects, and the line and load regulations ma be calculated using. Eqs.3.5 and 3.6. If there is an input ripple voltage, the output ripple will be severely attenuated. The ripple rejection ratio is the ratio of the output to input ripple amplitudes.

To assess the performance of a Zener diode voltage regulator, the ac equivalent circuit first drawn by replacing the diode with its dynamic impedance (Z_Z), as shown in Fig.3.4

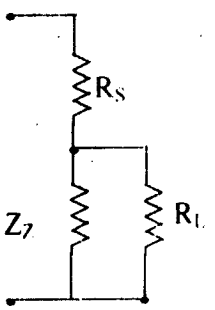


Fig 3.4 A.C. Equivalent circuit of Fig.3.3

The complete ac equivalent circuit is seen to be a simple voltage divider. When the input voltage changes by ΔV_s, the output voltage change is,

$$\Delta V_0 = \frac{\Delta V_S \times Z_Z}{R_S + Z_Z} \qquad (3.7)$$

Equation assumes that there is no load connected to the regulator output. When a load is present, R_L appears in parallel with Z_Z in the ac equivalent circuit. The equation for the output voltage change now becomes,

$$\Delta V_0 = \frac{\Delta E_S \times (Z_Z // R_L)}{R_S + (Z_Z // R_L)} \qquad (3.8)$$

The regulator source effect can be determined from eq 3.7 or eq, 3.8 as appropriate. The equations can also be used for calculating ripple rejection ratio. The input ripples amplitude (V_{ri}) and output voltages in Eq.3.7 and Eq.3.8. Thus Eq.3.7 can be modified to give a ripple rejection ratio equation,

$$\frac{\Delta V_{ro}}{\Delta V_{ri}} = \frac{Z_Z}{R_S + Z_Z} \qquad (3.9)$$

And, for a loaded regulator, Eq.3.8 gives,

$$\frac{\Delta V_{ro}}{\Delta V_{ri}} = \frac{Z_Z // R_L}{R_S + (Z_Z // R_L)} \qquad (3.10)$$

To determine the load effect of the Zener diode voltage regulator, the circuit output resistance has to be calculated. The regulator Thevenin equivalent circuit in fig. shows that, assuming a zero source resistance, the circuit output resistance is

$$R_0 = Z_Z // R_L \qquad (3.11)$$

When load current changes by ΔI_L, the output voltage change is

$$\Delta V_0 = \Delta I_L (Z_Z // R_L) \qquad (3.12)$$

Improved Voltage Regulation- The performance of a Zener diode is improved with an emitter follower. The combination of Zener diode/ regulator and an emitter follower is known as Zener follower. It has two advantages (1) less load on the Zener diode, and (2) lower output impedance. It thus increases the current handing capacity of a Zener regulator

3.3.2 TRANSISTOR SERIES REGULATOR

When a low - power Zener diode is used in the simple regulator , the load currents is limited by the maximum diode current,

. A high power Zener used in such a circuit can supply higher levels of load current, but much power is wasted when the load is light. The emitter follower regulator shown in Fig.3.5 is an improvement the simple regulator circuit because it draws a large current from the supply only when required by the load. In Fig 3.6 the circuit is drawn in the form of the common collector amplifier. In Fig3.6, the circuit is shown in

the form usually referred to as a Series Regulator. Transistor Q_1 is termed a Series-Pass transistor

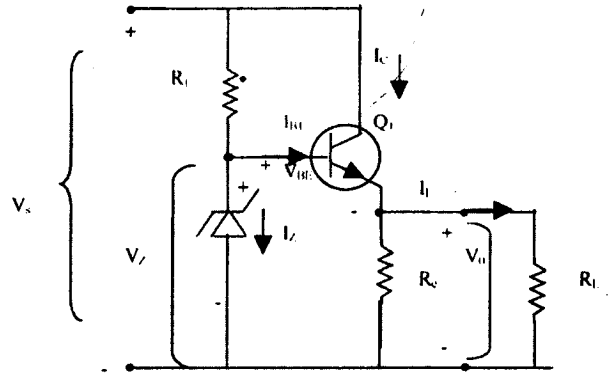


Fig.3.5 Emitter follower voltage regulator

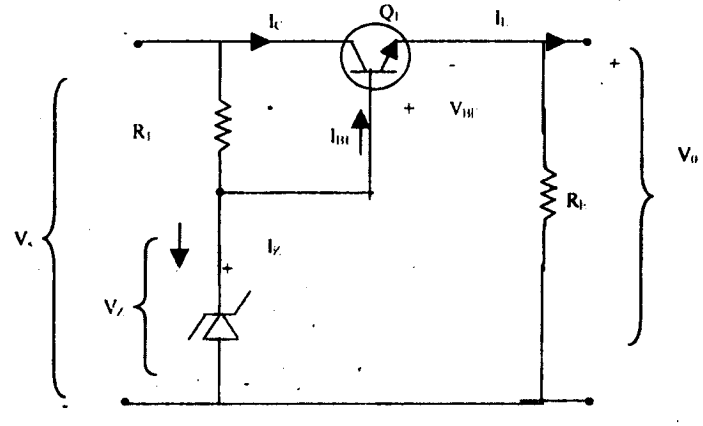


Fig.3.6 Series voltage regulator voltage regulator

The output voltage (V_0) from the Series Regulator is (V_Z -V_{BE}), and the maximum load current ($I_{L(max)}$) can be the maximum emitter current that Q_1 is capable of passing. For a 2N3055 transistor, I_L could approach 15A. When I_L is 0, the current drawn from the supply is approximately (I_Z + $I_{C(min)}$), where $I_{C(min)}$ is the minimum collector current to keep Q_1 operational. The Zener diode circuit (R_1 and D_1) has to supply only the base current of the transistor. The series voltage regulator is there, much more efficient than a simple Zener diode regulator.

Regulator with Error Amplifier

A Series Regulator using an additional transistor as an error amplifier is shown in Fig.3.8. The error amplifier improves the line and load regulation of the circuit, the amplifier also makes it possible to have an output voltage greater than the Zener diode voltage. Resistor R_2 and diode D_1 are the Zener diode reference source.

Transistor Q_2 and its associated components constitute the error amplifier that controls the series-pass transistor (Q_1).

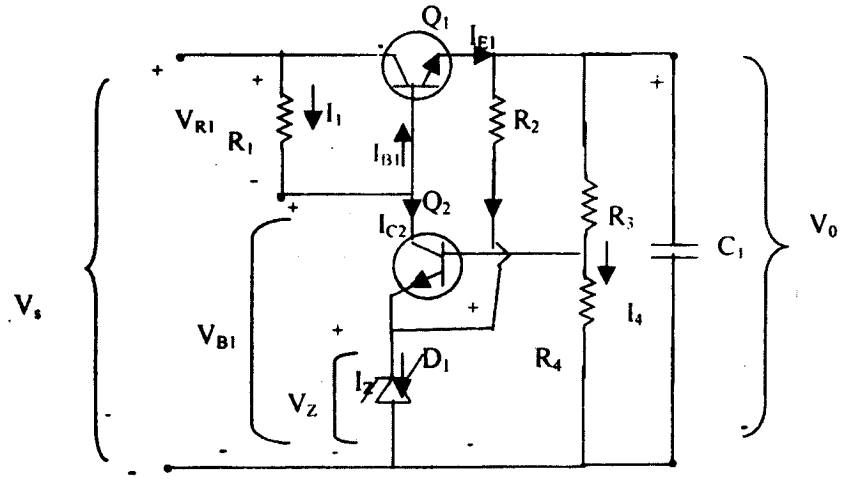


Fig.3.7 Series voltage regulator with error amplifier

The output voltage is divided by resistors R_3 and R_4, and compared to the Zener voltage level (V_Z). C_1 is a large value capacitor, usually 50μF to 100μF, connected at the output to suppress any tendency of the regulator to oscillate.

When the circuit output voltage changes, the change is amplified by transistor Q_2 and fed back to the base of Q_1 to correct the output voltage level. Suppose that the circuit is designed for $V_0 = 12V$, and that the supply voltage is $V_S = 18V$. A suitable Zener diode voltage in the case might be $V_Z = 6V$. For this V_Z level, the base voltage of Q_2 must be, $V_{B2} = V_Z + V_{BE2} = 6.7V$. So resistors R_3 and R_4 are selected to give $V_{BE2} = 6.7V$ and $V_0 = 12V$. The voltage at the base of Q_1 is, $V_{B1} = V_Z + V_{BE1} = 12.7V$ also, $V_{R2} = V_S + V_{B1} = 5.3V$ .The current through R_1 is largely the collector current of Q_2.

Now suppose the output voltage drops slightly for some reason. When V_0 decreases, V_{B2} decreases. Because the emitter voltage of Q_2 is held at V_Z, any decreases in V_{B2} appears across the base-emitter of Q_2. A reduction in V_{BE2} causes I_{C2} to be reduced. When I_{C2} falls, V_{R1} is reduced, and the voltage at the base of Q_1 rises ($V_{B1} = V_S + V_{R1}$) causing the output voltage to increase. Thus, a decrease in V_0 produces a feedback effect which causes V_0 to increase back toward its normal level. Taking the same approach, a rise in V_0 above its normal level produces a feedback effect which pushes V_0 down again toward it normal level.

When the input voltage changes, the voltage across resistor R_1 also changes, in order to keep the output constant. This change in V_{R1} is produced by a change in I_{C2} which itself is produced by a small change in V_0. Therefore, a supply voltage change

Transistor Q_2 and its associated components constitute the error amplifier that controls the series-pass transistor (Q_1).

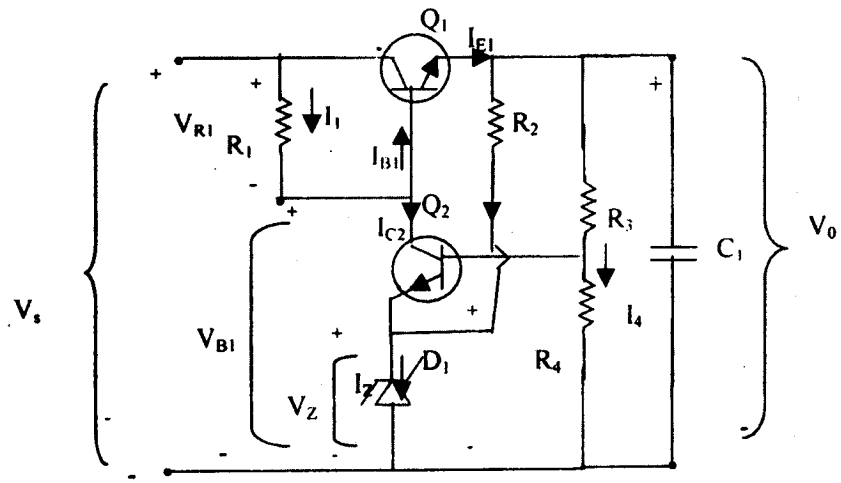


Fig.3.7 Series voltage regulator with error amplifier

The output voltage is divided by resistors R_3 and R_4, and compared to the Zener voltage level (V_Z). C_1 is a large value capacitor, usually 50μF to 100μF, connected at the output to suppress any tendency of the regulator to oscillate.

When the circuit output voltage changes, the change is amplified by transistor Q_2 and fed back to the base of Q_1 to correct the output voltage level. Suppose that the circuit is designed for $V_0 = 12V$, and that the supply voltage is $V_S = 18V$. A suitable Zener diode voltage in the case might be $V_Z = 6V$. For this V_Z level, the base voltage of Q_2 must be, $V_{B2} = V_Z + V_{BE2} = 6.7V$. So resistors R_3 and R_4 are selected to give $V_{BE2} = 6.7V$ and $V_0 = 12V$. The voltage at the base of Q_1 is, $V_{B1} = V_Z + V_{BE1} = 12.7V$ also, $V_{R2} = V_S + V_{B1} = 5.3V$ .The current through R_1 is largely the collector current of Q_2.

Now suppose the output voltage drops slightly for some reason. When V_0 decreases, V_{B2} decreases. Because the emitter voltage of Q_2 is held at V_Z, any decreases in V_{B2} appears across the base-emitter of Q_2. A reduction in V_{BE2} causes I_{C2} to be reduced. When I_{C2} falls, V_{R1} is reduced, and the voltage at the base of Q_1 rises ($V_{B1} = V_S + V_{R1}$) causing the output voltage to increase. Thus, a decrease in V_0 produces a feedback effect which causes V_0 to increase back toward its normal level. Taking the same approach, a rise in V_0 above its normal level produces a feedback effect which pushes V_0 down again toward it normal level.

When the input voltage changes, the voltage across resistor R_1 also changes, in order to keep the output constant. This change in V_{R1} is produced by a change in I_{C2} which itself is produced by a small change in V_0. Therefore, a supply voltage change

Since path AB is parallel to the output voltage V_0 across the load resistor R_L we have from the Kirchoff's voltage law

$$V_0 = -V_Z + V_{BE}$$

$$V_{BE} = V_0 - V_Z \qquad (1)$$

Since Zener voltage V_Z is fixed, any increase or decrease in V_0 will have a corresponding effect on V_{BE}.

Suppose V_0 decreases, than as is evident from equation 1, V_{BE} will decrease. Consequently, I_B decreases, therefore, I_C (= βI_B) will also decrease. It will lead to a decrease in I ($I_B+I_C+I_L$). Consequently, voltage (V_R =IR) across resistor R will decrease. As a result, output voltage V_0 will increase because

$$V_{in} = V_R + V_0$$

$$V_0 = V_{in} + V_R.$$

Thus the output voltage V_0 will remain at constant value or we get regulated voltage across R_L.

SUMMARY

The voltage regulation is further improved with the help of a negative feedback circuit. The highly stable zener voltage is amplified with a non-inverting voltage feedback amplifier to get higher output voltage. The regulated power supply usually includes current limiting, which protects the pass transistor and rectifier diodes in the case the load terminals are shorted accidentally. But it has the advantage of relatively large power dissipation in the pass transistor when the terminals are shorted.

It may be noted that the IC voltages regulators are recently being used in regulated power supplies. Switching regulators are also very popular now a days They produce large load currents with much less power dissipations in the transistor. Low power switching regulators are also available on chips. We learn about IC regulators in unit II.

3.4 KEY TERMINOLOGY

Emitter follower: It is a transistor amplifier where the output simply follows the variations in the input. The voltage gain is very nearly equal to 1 and current gain is high. The input and out put remain in phase with each other.

Darlington pair: Darlington transistors consisting of a pair of (low power and high power) BJTs fabricated together and packaged as a single device are available. There are usually referred to as Power Darlingtons. The 2N6039 is an npn Power Darlington.

3.5 SELF ASSESSMENT QUESTIONS:

Long answer questions:

1. Describe the construction and working of Zener diode. Explain its application in voltage stabilization.
2. Describe the circuit of a Zener diode regulator and explain its working.
3. Explain the working of a transistor series regulator.
4. Explain with a circuit diagram, the principle of working of a series regulated power supply.. What are its advantages over Zener diode regulator.
5. Define voltage regulation. Draw the circuit of a series transistor voltage regulator.
6. Draw characteristic of Zener diode. Explain with the help of a circuit diagram its use as a voltage regulator.
7. The supply voltage for the regulator in Fig.3.9 has 21V on no load, and V_S = 20V when $I_{L(max)}$ = 40mA. The output voltage is V_0 = 12V, and the regulator with a gain of 100. Calculate the source effect, load effect, line regulation, and load regulation for the complete power supply. Also calculate the ripple rejection ratio in decibels.

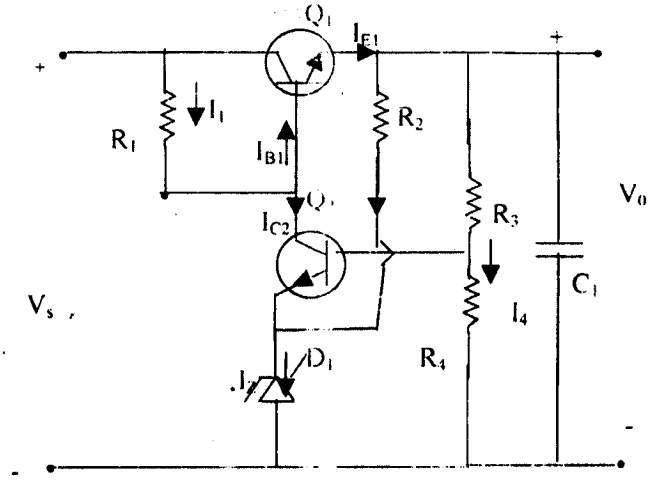


Fig.3.10 Series voltage regulator with error amplifier

Short answer questions

1. Explain the role of Zener diode in a series transistor regulator.
2. Explain the role of series pass transistor in a series transistor regulator.
3. Explain the role of error amplifier in a series transistor regulator.
4. Explain how the series transistor voltage regulator handles the variations in input supply.
5. Explain how the series transistor voltage regulator handles the variations in load current.
6. Calculate the voltage drop across 5Ω resistance and current passing through the Zener diode for the circuit given below.

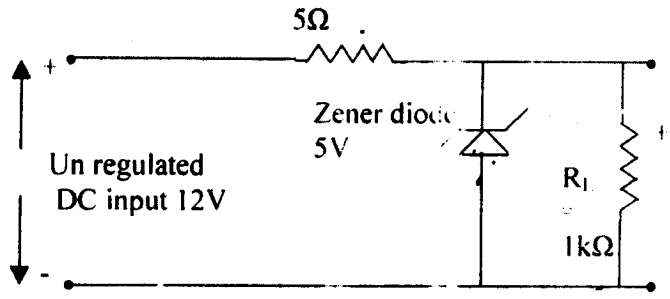


Fig 3.11

7. Explain the working of a transistor series voltage regulator.
8. Explain the working of a transistor shunt voltage regulator.
9. A power supply has a voltage regulation of 1%. If the no load voltage is 20V, what is the full-load voltage?.

3.6 TEXT AND REFERENCE BOOKS:

1. Integrated Electronics by Millman and Halkias
2. Basic Electronics and Linear Circuits - Bhargava etc

REFERENCE BOOKS

1. A text lab manual in Electronics by ZBAR (Tata Mc graw Hill)
2. Electronics fundamentals by JD Ryder
3. Op.Amp and linear integrated Circuits by Ramakant Gayakwad
4. Electronic Devices and Circuits by Samuel Seely.

UNIT – I **LESSON – 4**

POWER AMPLIFIERS

OBJECTIVE OF THE LESSON

To explain the use of power amplifiers and their working.

STRUCTURE OF THE LESSON

4.1 INTRODUCTION

In small signal amplifiers, the signal voltage and current are smaller, therefore, the amount of power handling capacity and power efficiency have little importance. The only requirements of small signal amplifiers are linearity and gain. When large signal are to be amplified for the operation of devices such as speakers and motors, the amplifier must be capable of handling large amount of power and its efficiency of converting input dc power to output ac power must be high. Such an amplifier is known as power amplifier. Hence the important requirements of power amplifiers are the power efficiency of the circuit, the maximum amount of power which the circuit can handle, and impedance matching between amplifier output and load, so that the maximum power is transferred to the output device.

4.1.1 CLASSIFICATION OF POWER AMPLIFIERS

As the power amplifiers have to handle large signals, the input signal may drive the collector to either the cut-off region or to saturation region. Consequently collector current may not flow during the entire period of the input signal. The power amplifier are classified according to the portion of the input signal for which collector current flows as class A, B, AB and C. In other words, this classification depends upon the

duration of the collector current flow with respect to the input signal, which is assumed to be a full 360^0.

In class – A amplifiers, there is always collector current regardless of the time in the cycle of the applied signal. The operating point Q is selected at the middle of the linear region of the transistor characteristic as shown in Fig 4.1(a). This class of amplifiers is considered to be linear because output signal is an exact replica of the input signal.

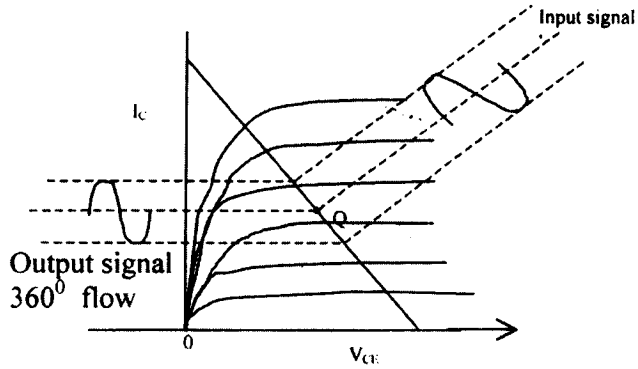


Fig.4.1(a) Operating conditions for power amplifiers class - A

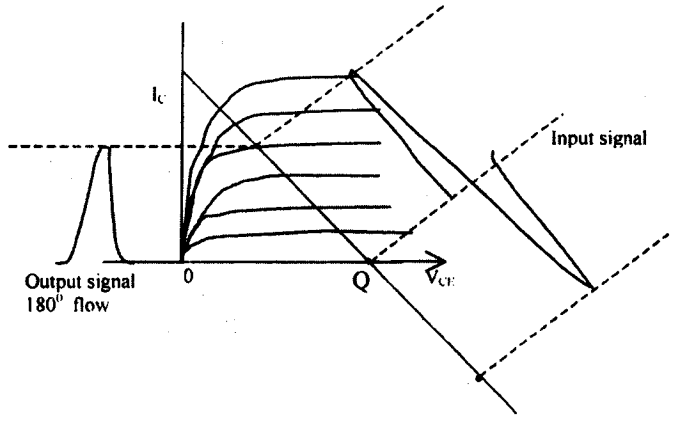


Fig.4.1(b) Operating conditions for power amplifiers class - B

In class – B amplifiers, the collector current flows only for one half of input signal. The operating point Q is located near the cut – off region as shown in Fig 4.1(b). In order to get the output current for full cycle, two Class–B amplifiers are used in a combination known as push – pull. In class – B amplifiers, the collector current flows only for one half of input signal. The operating point Q is located near the cut – off region as shown in Fig 4.1(b).

In class – C amplifiers, the collector current flows for less than the half cycle.

There are some amplifiers, which have operating parameters in between class-A and Class-B amplifiers. These amplifiers are designated as *class-AB*.

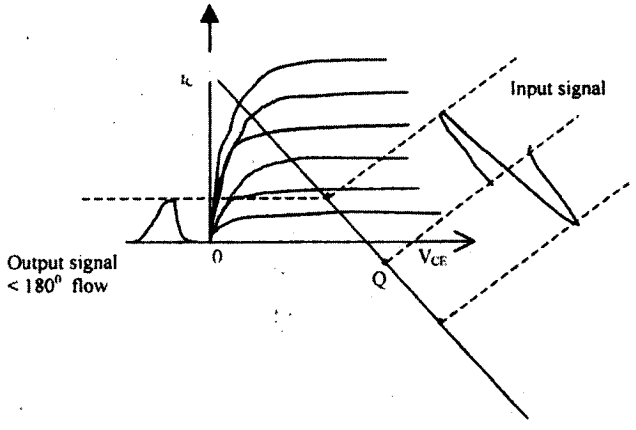


Fig.4.1(c) Operating conditions for power amplifiers class - C

4.2 Expression for Power and Efficiency of a Class -A power amplifier

Fig 4.2 shows a typical power amplifier circuit. The power P_s supplied by the battery V_{cc} is distributed in both load resistor R_L and the transistor as P_R and P_D respectively, i.e.,

$$P_S = P_R + P_D \qquad \text{---------- (4.1)}$$

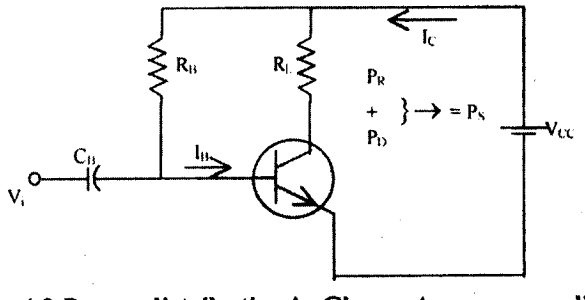


Fig.4.2 Power distribution in Class – A power amplifier circuit

In an amplifier circuit with the input signal, the current drawn from the battery V_{CC} has a wave shape having an ac signal component riding on a dc bias component. That is, the dc voltage source in an amplifier circuit furnishes a dc plus an ac current, which is not the case with input circuits having only passive elements such as resistors, capacitors and inductors. Hence the power across R_L is the sum of the powers owing to ac and dc currents i.e.

$$P_R = P_{RD} + P_{RA}$$

The power occurring due to ac current P_{RA} is the only useful component in an amplifier because it represents the ac output power P_0 i.e.,

$$P_{RA} = P_O$$

Hence $$P_S = P_O + P_{RD} + P_D \qquad \text{---------- (4.2)}$$

The terms P_{RD} and P_D represent the losses in the circuit. In fact, the operation of the power amplifier is to convert as much of the dc power P_S drawn from the battery into the ac power P_O across R_L. Hence, they efficiency of the circuit is defined as

$$\% \text{ Efficiency} = \eta = \frac{P_{O(ac)}}{P_{S(dc)}} \times 100$$

The power P_S and P_O can be expressed as

$P_S = V_{CC} \cdot I_C$, $P_O = I_C^2{}_{(rms)} \cdot R_L$ ---------- (4.3)

where I_C is the average current drawn from the battery and $I_{C(rms)}$ is the r.m.s. value of the ac current through R_L.

4.3 CLASS A DIRECT COUPLED POWER AMPLIFIER- Expression for power and efficiency

The circuit of a typical class A transistor power amplifier operating in the common emitter mode is shown in Fig.4.3. This mode of operation gives the largest power gain of all the three possible configurations. The amplifier is directly coupled to the load resistance R_L. The transistor is biased in class A condition, so that the collector current flows during the whole of the input signal cycle. The capacitor C_E is the emitter bypass capacitor and prevents the ac voltage from appearing across R_E. C_B is the blocking capacitor. This prevents the ac input signal voltage from interacting with the dc voltage in the base circuit.

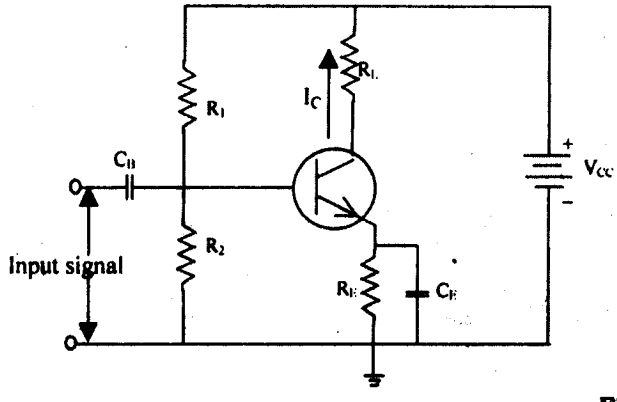


Fig.4.3a Circuit of a typical class – A power amplifier directly coupled to the load resistance

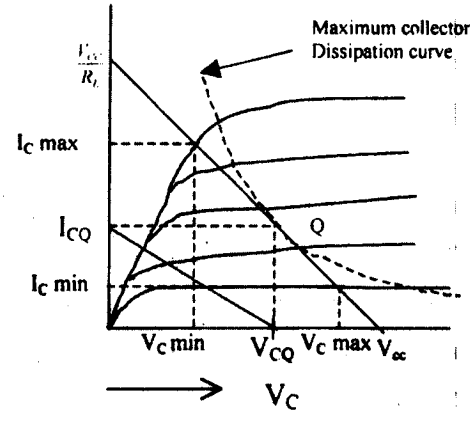


Fig.4.3b Collector characteristics with the load line for a direct coupled class – A power amplifier.

Fig.4.3b shows the collector characteristics of the transistor. The load line corresponding to R_L is drawn on the characteristics. Q is the quiescent operating point. This is located mid way upon the load line to ensure maximum output power. When the maximum input signal is applied, the quiescent operating point swings between cut off region and saturation. At cut off, the collector voltage is a maximum

and the collector current is a minimum. At saturation, reverse is the case, i.e., the collector voltage is a minimum and the collector current is a maximum.

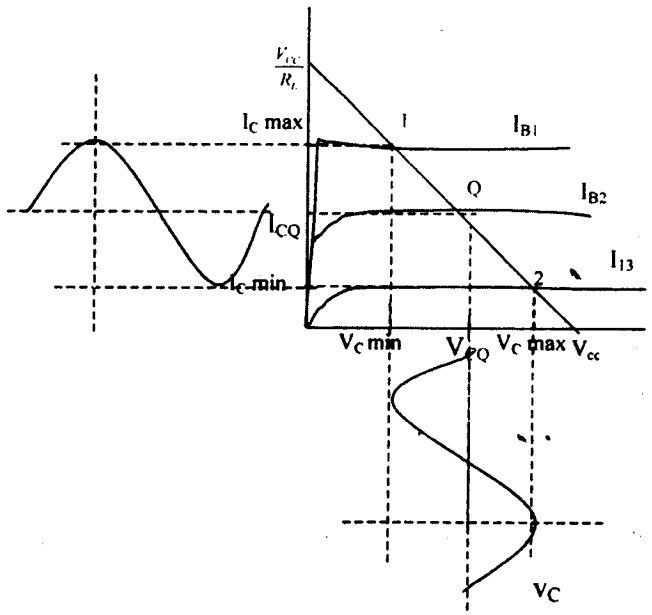


Fig.4. 3c Output characteristics and current voltage wave forms

In Fig.4.3c, V_{Cmax} and I_{Cmin}, represent the collector voltage and current corresponding to cut off condition; and V_{Cmin} and I_{Cmax} represent the same quantities corresponding to the saturation.

The input dc power supplied by the collector power supply is

$$P_{CS} = V_{CC}\ I_{CQ} \qquad \text{---------- (4.4)}$$

where I_{CQ} is the quiescent collector current.

The ac output power is given by

$$P_{ac} = V_{Crms}\ I_{Crms} \qquad \text{---------- (4.5)}$$

where V_{Crms} and I_{Crms} are the r.m.s. values of ac collector voltage and current respectively.

Assuming that the operating point swings equal distances on each side of the quiescent point Q, the peak value of the ac voltage V_{cm} and current I_{cm} are given by (see Fig.4.3c)

$$V_{Cm} = \frac{V_{Cmax} - V_{Cmin}}{2} \qquad \text{---------- (4.6)}$$

$$I_{Cm} = \frac{I_{Cmax} - I_{Cmin}}{2} \qquad \text{---------- (4.7)}$$

Therefore, the ac output power is

$$P_{ac} = \left(\frac{V_{Cmax} - V_{Cmin}}{2\sqrt{2}}\right)\left(\frac{I_{Cmax} - I_{Cmin}}{2\sqrt{2}}\right)$$

$$P_{ac} = \frac{(V_{Cmax} - V_{Cmin})(I_{Cmax} - I_{Cmin})}{8} \quad \text{---------- (4.8)}$$

Therefore, the collector efficiency is

$$\eta = \frac{P_{ac}}{P_{CS}} = \frac{(V_{Cmax} - V_{Cmin})(I_{Cmax} - I_{Cmin})}{8V_{CC}I_{CQ}} \quad \text{---------- (4.9)}$$

If the collector characteristics are ideal, then $V_{Cmin} = 0$, and $I_{Cmax} = 2I_{CQ}$, $V_{Cmax} = V_{CC}$ and $I_{Cmin} = 0$, substituting these values in Eq.(4.9), we get,

$$\eta = \frac{2V_{CC}I_{CQ}}{8V_{CC}I_{CQ}} = 0.25 \quad \text{---------- (4.10)}$$

Therefore, the maximum efficiency that can be obtained from a class-A power amplifier when coupled directly to the load resistance, is 0.25 or 25%.

4.4 TRANSFORMER COUPLED CLASS-A POWER AMPLIFIER

When the transistor works into a load resistance that is different from its output resistance, to obtain maximum power output, the load resistance is coupled to the power amplifier by a transformer. This is shown in Fig.4.4.

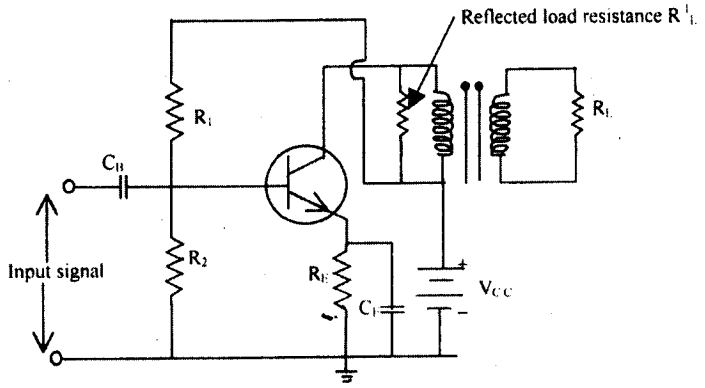


Fig.4.4 Transformer coupled class – A transistor power amplifier

In this circuit, the value of the base bias resistors R_1 and R_2 are adjusted to give class A operation with the expected input signal voltage. C_E is the emitter bypass capacitor and C_B is the blocking capacitor that prevents the ac input signal voltage from being interacted by dc base bias voltage.

The dc resistance of the transformer primary is small. This resistance serves as the collector load of the amplifier for dc currents. Hence the load line corresponding to this resistance will be almost vertical. This load line is the dc load line, and is shown in Fig.4.5. When the ac input signal source is connected to the input of the amplifier, resistance in the collector circuit is formed by the reflected

resistance of the load R_L. The load resistance reflected to the transformer primary is given by

$$R_L^{'} = a^2 R_L \qquad \text{---------- (4.11)}$$

where 'a' is the ratio of the number of turns N_p, in the primary to the number of turns N_s in the secondary and is called the turns ratio of the transformer.

If the resistance of the secondary windings of the transformer is R_s, then Eq.(4.11) becomes

$$R_L^{'} = a^2 (R_s + R_L) \qquad \text{----------(4.12)}$$

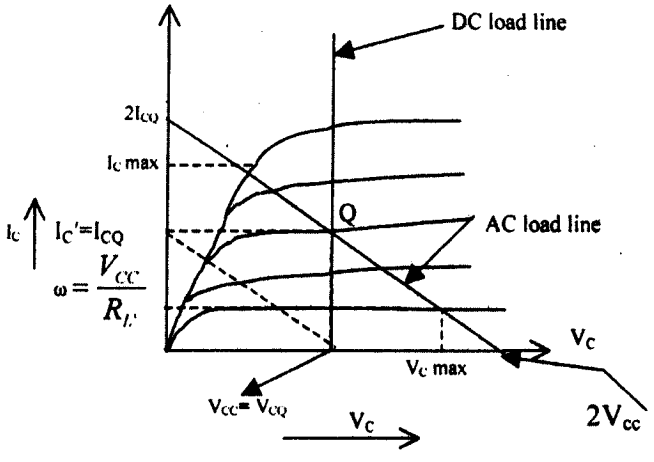


Fig.4.5 Collector characteristics with the dc load line, and ac load line for the transformer coupled class A power amplifier

$R_L^{'}$ is the load resistance actually seen by the collector for ac currents. This resistance is made equal to V_{Cmax}/I_{Cmax} by properly choosing the load line corresponding to this resistance. It is called dc load line and is shown in Fig.4.5. This line has a slope. $-1/R_L^{'}$. To locate this ac load line, the following method is adopted.

a) First assume some convenient value of the power supply voltage, say V_{CC}

b) Determine the current $I_C^{'} = \dfrac{V_{CC}}{R_L^{'}}$ and locate the point on the I_c axis.

c) Draw the line joining (V_{CC}, 0) and (0, I'_C) on the collector characteristics (the dotted line in Fig 4.5)

d) Now, draw a line through the quiescent operating point Q and parallel to the line V_{CC} I'_C. This line through the Q point is the desired ac load line.

When the ac signal is applied to the input of the amplifier, the collector current fluctuates and the operating point moves along the ac load line both sides of the

Q-point. Thus the instantaneous value of the collector voltage V_C will exceed the collector supply voltage V_{CC} during a part of the cycle. This is because of the fact that the induced voltage across the transformer primary windings adds to the supply voltage during part of the cycle.

For maximum output, the Q point is located on the dc load line to give a quiescent collector current $I_{CQ} = \frac{I_{C\,max}}{2}$. Hence, when the transistor operates at maximum capacity and its collector characteristics are ideal, the instantaneous collector voltage V_C swings from V_{Cmax} to zero and the collector current from zero to I_{Cmax}. This gives

$$V_{Cmax} = 2\,V_{CC} \qquad \text{----------} \qquad (4.13)$$

and

$$I_{Cmax} = 2\,I_{CQ} \qquad \text{----------} \qquad (4.14)$$

Also, for ideal collector characteristics, $V_{Cmin} = 0$, and $I_{Cmin} = 0$,

The expression for the actual collector efficiency is the same as that for a direct- coupled class – A amplifier and is given by eqn (4.9).

$$\eta = \frac{2V_{CC}.2I_{CQ}}{8V_{CC}I_{CQ}} = 0.5 \qquad \text{----------} \qquad (4.15)$$

Thus the theoretical maximum efficiency of transformer- coupled class A power amplifier is 50%. This is twice as great as that for direct- coupled class A amplifier.

4.5 HARMONIC DISTORTION

In the earlier sections we considered the transistor as a linear device, However, the dynamic transfer characteristics are not linear. This non-linearity arises because the static output characteristics are not equidistant straight lines for constant increments of input excitation. If the dynamic curve is non-linear over the operating range, the wave form of the output voltage differs from that of the input signal. Distortion of this type is called nonlinear, or amplitude distortion.

For a power amplifier with a large input swing, it is necessary to express the dynamic transfer curve with respect to operating point by a power series of the form

$$I_C = G_1 i_b + G_2 i_b^2 + G_3 i_b^3 + \ldots\ldots \qquad (4.16)$$

If we assume that the input wave is a simple cosine function of time, of the form,

$$I_b = I_{bm} \cos \omega t \qquad (4.17)$$

The output current will be given by

$$I_c = G_1 I_{bm} \cos \omega t + G_2 I_{bm} \cos^2 \omega t + G_3 I_{bm} \cos \omega t + \ldots\ldots \qquad (4.18)$$

The above equation can be rewritten as

$$I_C = I_C + i_c = I_C + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + \ldots\ldots \qquad (4.19)$$

That the output wave form must be represented by a relationship of this form is evident from an inspection of Fig.4.3c. It is observed from this figure that the output current curve must possess zero-axis symmetry, or that the current must be an even function of time. Expressed mathematically,

$$I(t) = i(-t).$$

Physically it means that the wave shape for every quarter cycle of the output-current curve as the operating point moves from point Q to point 1 is similar to the shape of the curve that is obtained as the operating point moves from point 1 to Q. Similarly, the wave shape of the current generated by the operating point as it moves from point Q to point 2 is symmetrical with that generated as it moves from point 2 back to point Q. These conditions are true regardless of the curvature of the characteristics. Since i_C is an even function of time the Fourier series in Eq.4.19 representing a periodic function of this symmetry, contains only cosine terms. The values of Fourier coefficients can be determined from the graph pertaining to the $i_c - i_b$ characteristic of the transistor.

The harmonic distortion is defined as

$$D_2 = \frac{|B_2|}{|B_1|} \quad D_3 = \frac{|B_3|}{|B_1|} \quad D_4 = \frac{|B_4|}{|B_1|} \qquad (4.20)$$

Where D_s (s =2,3,4,...) represent the distortion of the s^{th} harmonic.

If the distortion is not negligible, the power delivered at fundamental frequency is

$$P_1 = \frac{B_1^2 R_L}{2} \qquad (4.21)$$

However, the total power output is,

$$P = \left(B_1^2 + B_2^2 + B_3^2 + ...\right)\frac{R_L}{2} = \left(1 + D_2^2 + D_3^2 + ...\right)P_1$$

Or $$P = \left(1 + D^2\right)P_1 \qquad (4.22)$$

Where the total distortion, or distortion factor, is defined as

$$D = \sqrt{D_2^2 + D_3^2 + D_4^2 + ...}$$

If the total distortion is 10% of fundamental, then

$$P = \left[1 + (0.1)^2\right]P_1 = 1.01P_1$$

The total power output is only 1 percent higher than the fundamental power when the distortion is 10%. Hence little error is made in using only the fundamental term P_1 in calculating the power output.

PUSH-PULL CONNECTIONS

The amplifier circuits of Fig.4.3 and Fig.4.5 employ a single transistor as the amplifying active device. Hence, they are called ***single ended power amplifiers***. There is a definite limit to the power output obtainable from single ended amplifier. The power output can, however, be increased by using two transistors connected in parallel. Another method of obtaining greater output power is to connect two transistors in such a way that the collector current in one transistor decreases when that in the other transistor increases. This type of connection is commonly called the ***push-pull connection***. The push-pull connection can produce a power output of the same order of magnitude that a parallel connection can produce, but other additional advantages over parallel operation, the most important one of which is the elimination of the even order harmonic distortion. Hence, a push-pull operation is widely used when a greater maximum power output with a prescribed amount of harmonic distortion is required. The push-pull connection can be used for class A, B, AB, and C operations.

4.6 Push Pull Power Amplifier - Class A

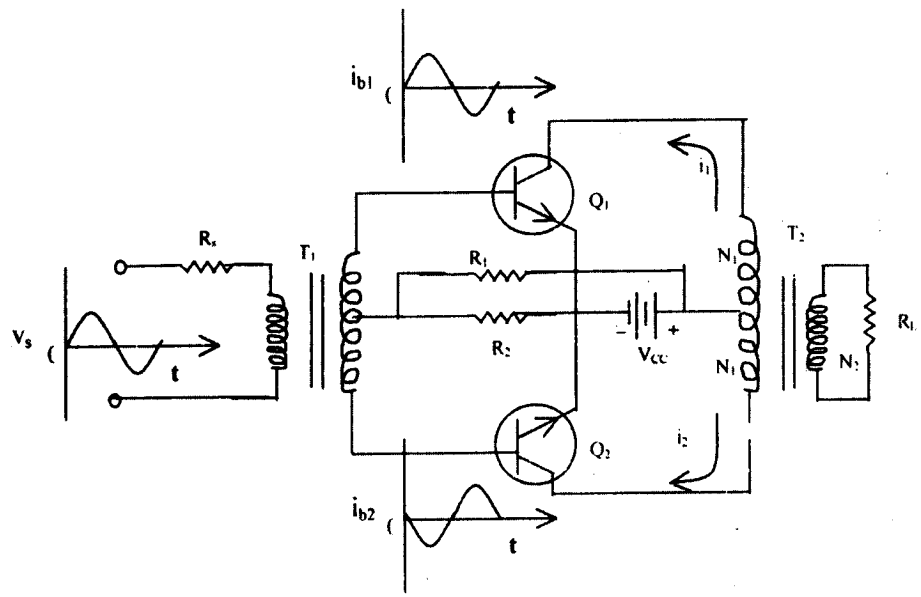


Fig.4. 6 Push-pull class – A Transistor power

A push –pull circuit employs two active devices (Fig 4.6) and requires two equal input signals 180^0 out of phase with each other derived from a centre-tapped input transformer (T_1). The output circuit also consists of a centre-tapped output transformer (T_2) so that the instantaneous currents flowing in the two devices are in opposite directions. Hence the magnetic fields of the two primary half windings are opposed. Therefore, saturation of the transformer core due to the d.c. components

and the resulting distortion are avoided. The output current is proportional to the difference of two primary currents and this leads to the cancellation of even harmonic distortions terms if the two halves of the push –pull amplifier are balanced.

By class A, we mean that the current flows in the output of the active device (each transistor) for the whole of the input cycle. In Fig.3.6, resistor R_1 and R_2 provide the correct amount of forward bias on the transistor bases, so that the collector current will flow in each transistor for the whole cycle of input signals. The transistor T_1 usually provides proper matching between source resistance R_s and the resistance to the transistor bases.

In order to understand the operation of the circuit, let us suppose that the input signal is going positive. Using the polarity dots on T_1, it will mean that the base of Q_1 will become more positive, while that of Q_2 less positive. Thus i_{C1} will increase and i_{C2} will decrease. The voltage induced in the secondary of T_2 across R_L will be proportional to the difference in the collector current, i.e., i_{C1}- i_{C2} since their magnetizing forces are opposite.

Similarly, when transistor input signal goes negative, the base of Q_1 will become less positive, with a decrease in base current and with a corresponding decrease in i_{C1}. The voltage across R_L is again due to the difference, i_{C1}~ i_{C2} but since i_{C1} is now greater than i_{C2}, the polarity of voltage induced across R_L is reversed. This "pushing and pulling" action in the output circuit is responsible for the decrease in harmonic by canceling of the even harmonics, with increasing odd harmonics.

Consider an input signals (base current) of the form $i_{b1} = i_{bm} \cos \omega t$ applied to Q_1. The output current of this transistor is given by eq 4.18 and is repeated here for convenience:

$$i_1 = I_{c'} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + \ldots\ldots\ldots\ldots \quad \text{------} \quad (4.23)$$

The corresponding input signal to Q_2 is

$$i_{b2} = -i_{b1} = I_{bm} \cos(\omega t + \pi)$$

The output current of this transistor is obtained by replacing ωt by $(\omega t + \pi)$ in the expression for i_1. That is,

$$i_2(\omega t) = i_1(\omega t + \pi) \quad \ldots\ldots\ldots (4.24)$$

hence

$$i_2 = I_{c'} + B_0 + B_1 \cos(\omega t + \pi) + B_2 \cos 2(\omega t + \pi) + \ldots\ldots\ldots\ldots$$

which is

$$i_2 = I_{c'} + B_0 - B_1 \cos \omega t + B_2 \cos 2\omega t - B_3 \cos 3\omega t + \ldots\ldots\ldots\ldots \quad (4.25)$$

As illustrated in Fig 4.6 , the current i_1 and i_2 are in opposite directions through the output –transformer primary windings. The total output current is then proportional to the difference between the collector currents in the two transistors. That is

$$i = k(i_1 - i_2) = 2k(B_1 \cos \omega t + B_3 \cos 3\omega t + ...) \qquad (4.26)$$

This expression shows that a push – pull circuit will balance out all even harmonics in the output and will leave the third - harmonic term as the principal source of distortion. This conclusion was reached on the assumption that the two transistors are identical. If their characteristics differ appreciably, the appearance of even harmonics must be expected.

The fact that the output current contains no even harmonic terms means that the push –pull system possesses "half-wave", or "mirror", symmetry, in addition to the zero-axis symmetry. Half-wave symmetry requires that the bottom loop of the wave, when shifted 180^0 along the axis, will be the mirror image of the top loop. The condition of mirror symmetry is represented mathematically by the relation.

$$i(\omega t) = -i(\omega t + \pi) \qquad (4.27)$$

If $(\omega t + \pi)$ is substituted for (ωt) in Eq .4.26, it will be seen that Eq.4.27 is satisfied.

Advantages of a Push Pull System:

1. The magnetic saturation of the transformer core by dc does not occur because the dc components of collector currents oppose each other in the transformer resulting in zero dc flux in the core. It will reduce the cost because we can use small size transformers.
2. Distortion in the output much reduced due to cancellation of all the even harmonic components. Hence the circuit gives more output power per transistor.

Disadvantages of a Push Pull System:

1. Power supply hum is not eliminated by push –pull circuit.
2. Two identical transistors are needed
3. In transformer, central tapping is required.
4. Entire system becomes bulky with the use of two transformers.
5. Due to stray intertwining capacitances the frequency response of the amplifier becomes poor.

4.7 PUSH-PULL POWER AMPLIFIER - CLASS – B

The circuit diagram of a push-pull Class – B transistor power amplifier is shown in Fig.4.7. The bases and the collectors of the two transistors are connected to the opposite ends of the center-tapped input and output transformers T_1 and T_2

respectively. The transistors are biased to cut-off so that no collector currents, except the leakage or cut-off currents, flow when the input signal is zero.

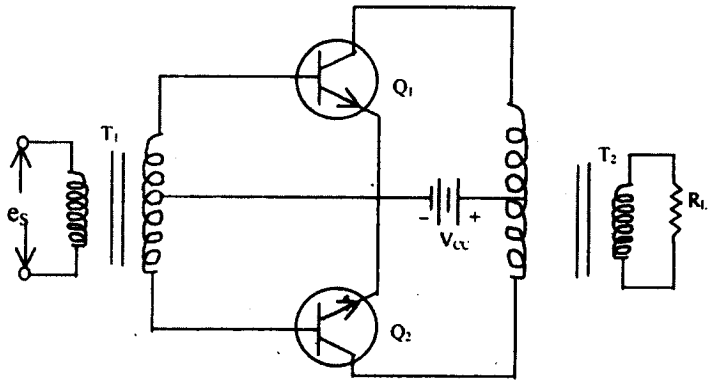


Fig.4.7 Push-pull class – B Transistor power amplifier

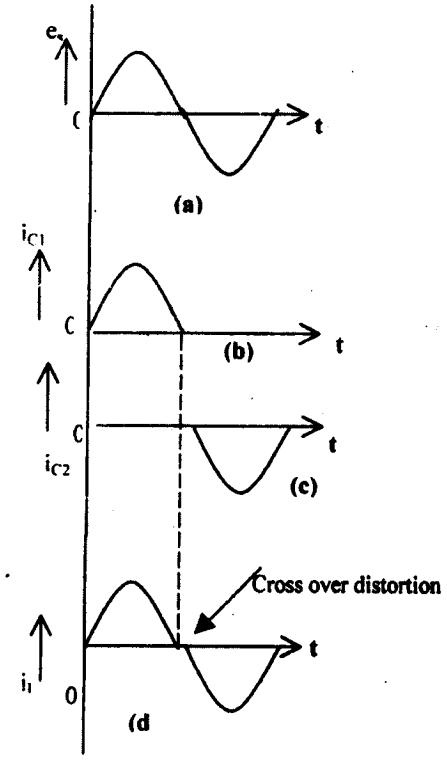


Fig.4.7.1 Waveform of (a) input voltage (b) collector current of Q_1 (c) collector current of transistor Q_2 and (d) the total load current of the class – B push-pull amplifier

During one half-cycle of the input signal (Fig.4.7), the upper end of the secondary of the input transformer T_1 becomes positive with respect to its center, and the lower end becomes negative during the next half cycle, the lower end is positive and the upper end is negative with respect to the center.

Hence, during one half cycle of the input signal, the transistor Q_1 is forward biased and conducts and the transistor Q_2 remains at cut-off. During the next half cycle of the input signal, the reverse is the case; i.e., Q_2 conducts and Q_1 is cut off. Therefore the collector current for each transistor has half sinusoidal waveform as shown in Fig 4.7.1 (b) and (c).

The total load current i_L is, however, a complete sine wave [Fig 4.7.1(d)] because the collector current for each transistor flows through each half of the primary of the output transformer T_2.

Assuming the dc resistance of the primary of the transformer T_2 to be very small, the dc load line is drawn almost vertical. A collector characteristic of a transistor operating under class – B conditions is shown in (Fig 4.7.2)

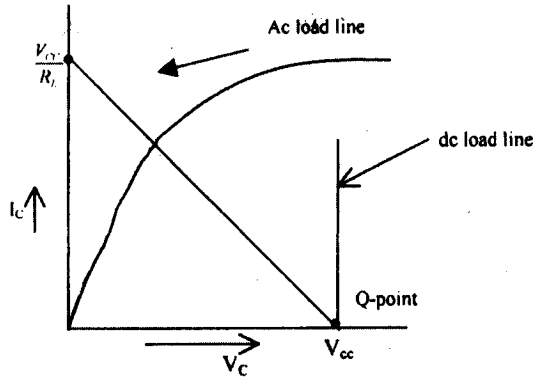


Fig 4.7.2 The ac and dc load lines on a collector characteristics of a transistor used in a push pull class – B power amplifier.

The reflected resistance across the primary of T_2, if the secondary winding resistance R_S is neglected, is given by

$$R_L^{II} = a^2 R_L \qquad \text{---------- (4.28)}$$

The resistance appears from the collector to collector of the two transistors. The load impedance R_L^I seen by each transistor is that appearing between one end of the transformer and the center tap. Therefore,

$$R_L^I = \left(\frac{a}{2}\right)^2 R_L = \frac{a^2}{4} R_L \qquad \text{----------(4.29)}$$

The ac load line corresponding to R_L^I is drawn on the collector characteristic of a transistor in the Fig 4.7.2. Since the amplifier operates under class-B condition, the voltage across a transistor is $V_C = V_{CC}$ when the collector $I_C = 0$ for that transistor. Also for $V_C = 0$, I_C is given by $\frac{V_{CC}}{R_L^I}$. Therefore the ac load line passes through (V_{CC},

0) and (0, $\frac{V_{CC}}{R_L^1}$) co-ordinates. Since the collector current and voltage are half sinusoidal for class B operation, the relationship between the root mean square (rms) and the peak values are given by

$$V_{C\,rms} = \frac{V_{C\,max}}{\sqrt{2}} \qquad \text{---------- (4.30)}$$

And $$I_{C\,rms} = \frac{I_{C\,max}}{\sqrt{2}} \qquad \text{---------- (4.31)}$$

Hence, the output power due to one transistor is given by

$$P_{ac} = V_{C\,rms}\, I_{C\,rms} = \frac{V_{C\,max}\, I_{C\,max}}{2} \qquad \text{---------- (4.32)}$$

As only one transistor is conducting at a time, the total output power is

$$(P_{ac})_{total} = \frac{V_{C\,max}\, I_{C\,max}}{2} \qquad \text{-------- (4.33)}$$

Fig 4.7.2 shows that the maximum collector voltage swing that can occur is given by $V_{Cmax} = V_{CC}$, hence Eq. 4.33 becomes

$$(P_{ac})_{total} = \frac{V_{CC}\, I_{C\,max}}{2} = \frac{V_{CC}^2}{2R_L^1} \qquad \text{---------- (4.34)}$$

Eq.4.34 gives the maximum output power. Further the dc power supplied by the transistor is given by

$$P_{Cs} = V_{CC}\, I_{Cav} \qquad \text{---------- (4.35)}$$

Where I_{Cav} the average value of half sinusoidal and is given by

$$I_{Cav} = \frac{I_{C\,max}}{\pi} \qquad \text{---------- (4.36)}$$

There fore, the total power supplied by the two transistors is given by

$$(P_{cs})_{total} = 2\,P_{cs} = \frac{2V_{CC}\, I_{C\,max}}{\pi} = \frac{2V_{CC}^2}{\pi R_L^1} \qquad \text{---------- (4.37)}$$

Finally, the maximum efficiency of the class B push-pull power amplifier is

$$\eta_{max} = \frac{(P_{ac})_{total}}{(P_{cs})_{total}} = \frac{V_{CC}^2}{2R_L^1} \times \frac{\pi R_L^1}{2V_{CC}^2} = \frac{\pi}{4} \qquad \text{---------- (4.38)}$$

Hence, the efficiency that can be obtained with a push-pull class B operative is $\frac{\pi}{4}$ or 78.5%

4. 8 PUSH-PULL AMPLIFIER - CLASS – AB

The avoid the effect of cross-over distortion, the base-emitter junctions of both transistors are slightly forward biased by the amounts of certain voltage, so that when an a.c. signal is applied to the base, collector current starts flowing immediately and thus linearizes the near-origin part of curve. This is achieved by adding biasing resistors R_1 and R_2 in the class B push –pull circuit as in a class A push –pull amplifier. But now R_1 and R_2 are chosen to place the operating point much closer to cut-off than class B operations. This stage is then, ***a class AB push –pull stage*** (fig) but it is normally treated as class B, since the stand- by current is very small percentage of the peak current. In a class AB operation the device current flows for more than 180^0 but less than 360^0 of the input signal cycle. The resistance R_e, although causes some decrease in the output power by the degenerative feedback action, but it helps to reduce the distortion considerably.

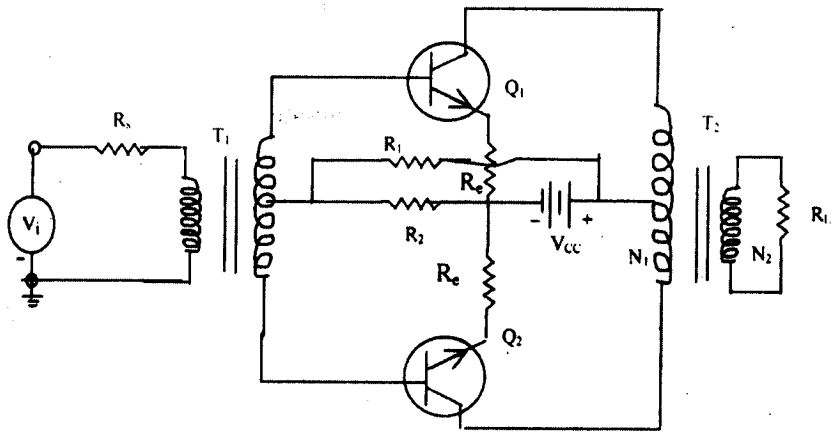


Fig.4. 8 Push-pull class – AB Transistor power amplifier

Advantage of Class AB Amplifiers:

1. Minimum cross over distortion.
2. Small standby current flows at zero excitation.
3. Class AB operation results in the less distortion than class B.

Disadvantage of Class AB Amplifiers

1. Getting less distortion must be paid for this improvement is a loss in efficiency.
2. Waste of standby power.

COMPLEMENTARY-SYMMETRY PUSH PULL AMPLIFIER

Two transistors- one NPN and other PNP, having identical characteristics, are said to have complementary symmetry. Current conduction in such transistors are complementary to each other, i.e., they conduct in opposite half cycles of the input signal. A complementary symmetry push –pull class B power amplifier circuit that

It transistors do not have perfect complementary symmetry, considerable distortion in produced

4.9 SUMMARY

When large input signals are to be amplified for the operation of output device such as speakers and motors, the amplifier must be capable of handling large amount of power and its efficiency of converting input dc power to output ac power must be high. Such an amplifier is known as a power amplifier. Power amplifiers are classified on the basis of their operating point as class A, B, AB, C etc.

In class A amplifiers, there is always collector current regardless of the time in the cycle of the applied signals. As a result, power losses many be increased. Since the collector current flows only for one half of the input signal in class B amplifier and in order to get output power for full cycle, two class B amplifiers are used in a combination known as push-pull. Therefore, the power losses may be minimized and simultaneously the collector efficiency also increases in class B push-pull power amplifier.

4.10 KEY TERMINOLOGY

1. **Quiescent (Q) point**: The operating point in the absence of signal is called Quiescent point or simply the Q point of the device. The particular Q point at which the device will operate depends on the base current(I_B) and V_{CE}..
2. **Direct Coupling**: To amplify all the frequencies in the signal, signal source is coupled to the amplifier stage directly without using DC blocking capacitors and isolation transformers. In the same manner amplifier output is connected to the load. Direct coupling may be used to connect to the amplifier stage to the other. However precautions must be taken to provide level shifting so that satisfactory biases are established at various points in the circuit. This type of coupling is preferred in the fabrication of the integrated circuits (ICs).
3. Push-Pull Configuration: Two transistors amplifiers are said to be connected in push-pull configuration when the amplifiers are connected such that as current in one stage pushes forward, in the other, current pulls back. This configuration avoids the power losses in the transformer core and results in higher efficiency than a two transistor parallel coupled amplifier.
4. Complimentary Symmetry Amplifier: Push pull action is produced by using one NPN and one PNP transistor. As the current direction are opposite in them for the given input, we need not use a driver transformer. Due to the same reason we can avoid the output transformer and at the same time get the push-pull action with this arrangement. In the ordinary push pull amplifier circuit, transformers

occupy major space and contribute heavily for the weight and cost. Complimentary symmetry circuit can be very compact and cheap.

4.11 SELF-ASSESSMENT QUESTIONS

Long answer questions

4.1 Describe the various classes of power amplifier in terms of the operating point.

4.2 Define efficiency of power amplifier and compare efficiencies in case of A, B and C classes of amplifiers.

4.3 Obtain an expression for the collector efficiency of transformer coupled class-A transistor power amplifier.

4.4 Describe a class-B push-pull power amplifier and obtain an expression for its efficiency. How the class-B push-pull amplifier is an advantageous over the class-A amplifier?

4.5 Classify power amplifiers as class A, class B and class AB. Discuss their advantages and disadvantages.

4.6 Explain the second harmonic distortion in power amplifiers. How is it eliminated in push-pull amplifiers?.

4.7 A class B transformer coupled audio amplifier is fed to 20V dc. Transformer turns ratio is 4. If a 4Ω load is connected, find (i) Power dissipation rating of each transistor. (ii) Power delivered to the load. [Ans (i) 1.26W (ii). 3.125W]

4.8 A class B transformer coupled audio amplifier is fed to 20V dc. Output load impedance of the amplifier is 10Ω. The peak voltage across the load is 15V. Find the efficiency of the amplifier [Ans 58.9%]

SHORT ANSWER QUESTIONS

1. Discuss class AB amplifier.
2. What are the advantages of push-pull amplifiers?.
3. Write a short note on harmonic distortion.
4. Explain the cross-over distortion in class B amplifiers. How it can be eliminated?
5. A 25Ω loads has to be matched to an amplifier so that the reflected impedance is 10 kΩ. Find the turns ratio of output transformer.

4.12 TEXT AND REFERENCE BOOKS

1. Integrated Electronics by Millman and Halkias
2. Basic Electronics and Linear Circuits - Bhargava etc

REFERENCE BOOKS

1. Solid state electronics circuits and digital electronics by Agarwal & Agarwal
2. Electronic Devices and Circuits David A.Bell (PHI)
3. A text lab manual in Electronics by ZBAR (Tata Mc Graw Hill)
4. Electronic Devices and Circuits by Samuel Seely
5. Electronics fundamentals by JD Ryder

UNIT II

LESSON 5

OPERATIONAL AMPLIFIERS I

OBJECTIVES OF THE LESSON: To explain the basic differential amplifier, to introduce ar operational amplifier and to discuss the properties of the operational amplifier.

STRUCTURE OF THE LESSON

5.1 INTRODUCTION

The differential amplifier, also called a difference amplifier, as the name implies, amplifies the difference between two signals. Because of its balanced nature and symmetry, it can amplify very small signals. It usually requires a minimum number of capacitors and can operate without bypass and coupling capacitors. It is the basic building block of operational amplifiers, which are most widely used in integrated circuits.

Fig 5.1 Schematic diagram of a differential amplifier

For a linear active device with two input signals v_1 and v_2 and the output signals v_0 each measured with respect to ground, we have

$$v_0 = A\,(v_1 - v_2) \qquad \text{------ (5.1)}$$

where A is the voltage gain of the differential amplifier. In actual practice, the output depends not only upon the difference of the two input signals but also upon the average level. In symmetrical circuits, we talk about the in-phase signals (called common mode (CM) signals v_c) and the difference or anti-phase signals (called differential mode (DM) signals v_d). They are defined as

$v_c = \frac{1}{2}(v_1+v_2)$, and $v_d = (v_1 - v_2)$ ---------(5.2)

The output v_0 can be expressed as linear combination of the two input voltages, as

$v_0=A_1 v_1 +A_2 v_2$ --------- (5.3)

where A_1 and A_2 are the voltage amplifications from input 1 and 2 respectively. From Eqs .(5.2) and Eq.(5.3) we get

$$v_o = A_1(v_c + \frac{1}{2} v_d) + A_2(v_c - \frac{1}{2} v_d)$$

$$= (A_1 + A_2)v_c + \frac{1}{2}(A_1 - A_2) v_d = A_c v_c + A_d v_d \quad \text{----------(5.4)}$$

where $A_c = A_1 + A_2$ and $A_d = \frac{1}{2}(A_1 - A_2)$, are voltage gains for the signals in common mode and differential modes respectively. They may be defined as

$$A_d = \left(\frac{v_0}{v_d}\right)_{V_c=0} \text{ and } A_c = \left(\frac{v_0}{v_c}\right)_{V_d=0} \quad \text{----------(5.5)}$$

Thus A_d can be measured directly by setting $v_c = 0$, or $v_2 = - v_1$.

The A_c can be measured by setting $v_d = 0$, or $v_2 = v_1$, generally the desired signals in differential amplifier are DM and undesired signals are CM. The figure of merit for differential amplifier in defined as

$$\rho = \left[\frac{A_d}{A_c}\right] \quad \text{---------- (5.6)}$$

This is called the common-mode rejection ratio (CMRR) and is also some times referred to as the discrimination factor of a differential amplifier. Ideally $A_c=0$, and CMRR= ∞ . In practice, A_c is non-zero but very small, where as A_d is very large. The combination of Eqs. (5.4) and (5.6) gives

$$Vo = A_d v_d \left[1 + \frac{A_c v_c}{A_d v_d}\right] = A_d v_d \left[1 + \frac{v_c}{v_d}.\frac{1}{CMRR}\right]$$

$V_0 = A_d v_d$ (since CMRR = ∞) ----------(5.7)

A basic differential amplifier circuit, consisting of two interlocked common emitter amplifier stages is shown in Fig.5.2. The two stages are linked by having both emitters connected to a constant current generator. As current through one emitter increases, current through the other decreases.

The circuit is symmetric about the vertical dashed line and the two transistors and resistors R_c form a bridge circuit that is balanced under zero input signal. The resistors and the transistors are simultaneously fabricated in adjacent areas on a small chip. They will be at

the same temperature. A simultaneous change in h_{FE} or V_{BE} will produce equal changes in the voltages at a and b and v_0 will not be affected.

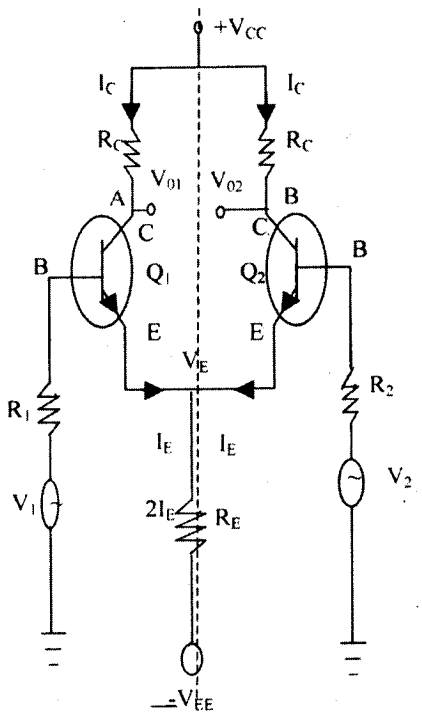


Fig.5.2 Basic differential amplifier

Consider the circuit operation with no input signals. For $v_1 = v_2 = 0$, an emitter current I_E flows in each BJT. Therefore $I_C = I_E$ and

$$V_{01} = V_{02} = V_{CC} - I_C R_C \qquad \text{----------(5.8)}$$

$$\text{thus the base current } I_B = \frac{I_E}{h_{FE}} \qquad \text{----------(5.9)}$$

$$\text{and } V_E = -I_B R_1 - V_{BE} \qquad \text{----------(5.10)}$$

If V_{CE} is chosen large enough to bias each BJT in the center or the linear operating region, then

$$V_{CC} = V_{EE} + 2 I_E R_E + V_{CE} + I_C R_C \qquad \text{----------(5.11)}$$

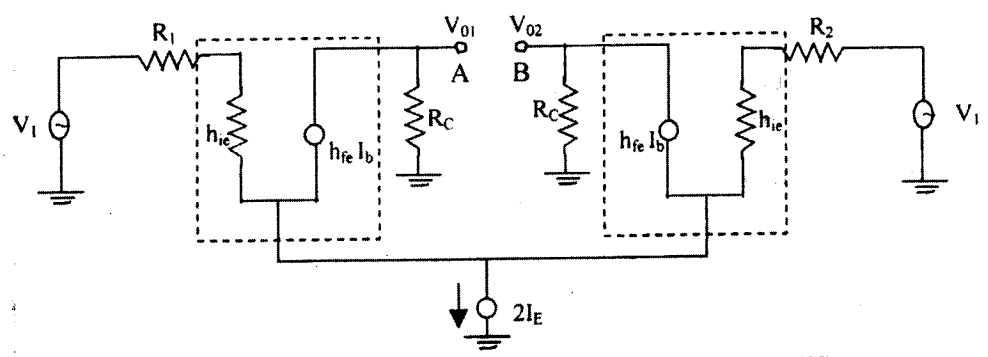


Fig.5.3 AC equivalent circuit of basic differential amplifier

The ac equivalent circuit for use as differential amplifier is shown in Fig.5.3. Here it is assumed h_{oe} R_C <<1 or h_{oe} <<1/R_C and thus h_{oe} is omitted in this figure. The collector current $I_c = h_{fe}$ I_b. The voltage h_{re} v_c is neglected in comparison with the h_{ib} I_b drop across h_{ie}

Common mode voltage gain :

Let $v_1 = v_2 = v_s$, user $A_c = \frac{v_o}{v_c} = \frac{v_o}{v_s}$.

Due to symmetry, each input at the base, sees a common emitter circuit, with a unbypassed emitter resister of $2R_E$ (the emitter resistor is effectively doubled, as it carries the emitter current for both transistors). Thus we have

$$Z_i=R_1+h_{ie}+2R_E(1+h_{fe}) \text{ and } Z_0 = R_c \quad \text{----------(5.12)}$$

$$\text{Current gain} = A_i = \frac{-I_c}{I_b} = \frac{-h_{fe} I_b}{I_b} = -h_{fe} \quad \text{----------(5.13)}$$

$$\text{Voltage gain } A_v = \frac{A_i Z_0}{Z_i} = \frac{-h_{fe} R_c}{(R_1 + h_{ie} + 2R_E(1+h_{fe}))} \quad \text{----------(5.14)}$$

Since usually $(1+h_{fe})$ $2R_E >> h_{ie}$ and $1+h_{fe} = h_{fe}$. The source resistance $R_i << h_{ie}$. Therefore

$$A_v = \frac{-R_C}{2R_E} = \text{common mode voltage gain } A_c.$$

Differential mode voltage gain:-

$$\text{Let} \qquad -v_2 = v_1 = \frac{v_s}{2};$$

Therefore, $v_d = v_1, -v_2 = v_s$ and $A_d = \frac{v_0}{v_d} = \frac{v_0}{v_s}$.

From the symmetry of Fig (5.2) for $v_1 = -v_2$.

The emitter of each transistor is grounded for small signal operation i.e., $R_E = 0$ and

$$Z_i = 2(R_i + h_{ie}),\ Z_o \cong R_c,\ A_i \cong -h_{fe}. \quad \text{----------(5.15)}$$

$$A_v = \frac{A_i Z_0}{Z_i} = \frac{-h_{fe} R_c}{2(R_i + h_{ie})} \quad \text{---------- (5.16)}$$

= Differential mode voltage gain A_d.

Common mode rejection ratio:-

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{-h_{fe} R_c}{2(R_i + h_{ie})} \div \left(-\frac{R_c}{2R_E}\right) = \frac{-h_{fe} R_c}{(R_1 + h_{ie})} \quad \text{--------- (5.17)}$$

Thus we see that CMRR increases with R_E as desirable.

Constant current generators

Instead of resistor R_E, a constant current generator is used. It may be a JFET with its gate tied to its source. A BJT can be used in a similar way with voltage divider bias. In both

cases, the output current is approximately constant as long as the voltage across the device is sufficient.

Constant current bias:-

In the differential amplifier discussed so far, the combination of R_E & V_{EE} is used to set up the dc emitter current. We can also use constant bias to set up the dc emitter current if desired. In fact the constant current bias is better because it provides current stabilization and in turn, assures a stable operating point for the differential amplifier. Fig.5.4 shows the dual input balanced output differential amplifier using a resistive constant current bias. Notice that the resistor R_E is replaced by a constant current source transistor (Q3) circuit. The dc collector current in the transistor Q_3 is established by resisters R_1, R_2 and R_E and can be determined as follows. Applying the voltage divider rule, the voltage at the base of transistor Q_3 (neglecting base loading effect) is

$$V_{B3} = \frac{-R_2 V_{EE}}{(R_1 + R2)} \qquad \text{----------(5.18)}$$

$$V_{E3} = V_{B3} - V_{BE3} = \left(\frac{-R_2 V_{EE}}{(R_1 + R2)}\right) - V_{BE3} \qquad \text{---------- (5.19)}$$

$$I_{E3} = I_{C3} = \frac{(V_{E3} - (-V_{EE}))}{R_E} \qquad \text{---------- (5.20)}$$

$$I_{C3} = v_{EE} - \left(\frac{-R_2 V_{EE}}{(R_1 + R2)}\right) \cdot \frac{V_{BE3}}{R_E} \qquad \text{----------(5.21)}$$

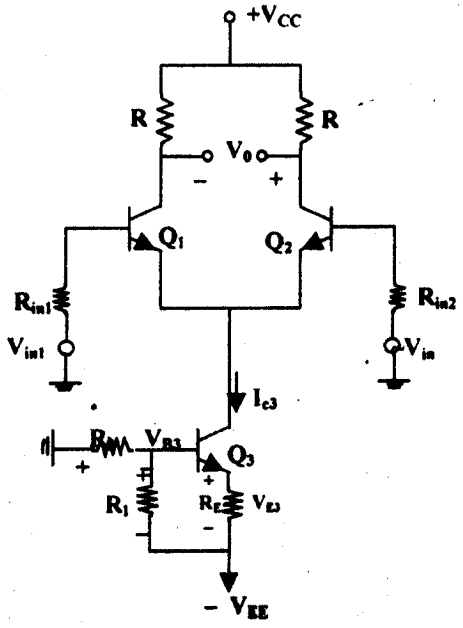


Fig.5.4 Differential amplifier using constant current bias.

Because two halves of the differential amplifier are symmetrical, each has half of current I_{ce3}.

That is $$I_{E1} = I_{E2} = \frac{I_{C3}}{2} = V_{EE} - \left(\frac{R_2 V_{EE}}{(R_1 + R2)}\right) \cdot \frac{V_{BE3}}{2R_E} \quad \text{----------(5.22)}$$

The collector current I_{c3} in transistor Q_3 is fixed and must be invariant because no signal is injected into either the emitter or the base of Q_3. Thus the transistor Q_3 is a source of constant emitter current for transistors Q_1 and Q_2 of the differential amplifier. Besides supplying constant emitter current, the constant current bias also provides a very high source resistance since the ac equivalent of the dc current source is ideally an open circuit.

5.2 OPERATIONAL AMPLIFIER

An operational amplifier is a direct-coupled high gain amplifier usually consists of one or more differential amplifiers and usually followed by a level translator and an output stage. The output stage is generally a push pull or push pull complementary symmetry pair. An operational amplifier is available as a single integrated circuit package. The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication and integration. Thus the name operational amplifier stems from its original use for doing these mathematical operations and so is abbreviated to op-amp. With the addition of suitable external feedback component, the modern day operational amplifier can be used for a variety of applications. Such as ac and dc signal amplification, active filters, oscillators, comparators, regulators and others.

Block diagram representation of a typical op-amp

Since an op-amp is a multistage amplifier. It can be represented by a block diagram shown in Fig.5.5.

The input stage is the dual input balanced output differential amplifier. This stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the op-amp. The intermediate stage is usually another differential amplifier, which is driven by the output of the first stage.

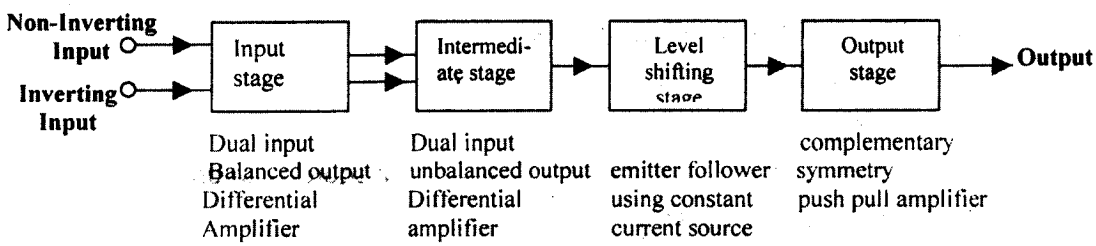


Fig.5.5 Block diagram of a typical op-amp

In most amplifiers, the intermediate stage is dual input unbalanced (single ended) output. Because direct coupling is used, the dc voltage at the output of the intermediate stage is well

above ground potential. Therefore, the level translator circuit is used after the intermediate stage to shift the dc level at the output of the intermediate stage downward to zero voltage with respect to ground. The final stage is usually a push pull complementary amplifier output stage. The output stage increases the output voltage swing and raises the current supplying capabilities of the op-amp. The well designed output stage also provides low output resistance.

Schematic symbol:

The most widely used symbol for a circuit with two inputs and one out put is shown in Fig. 5.6

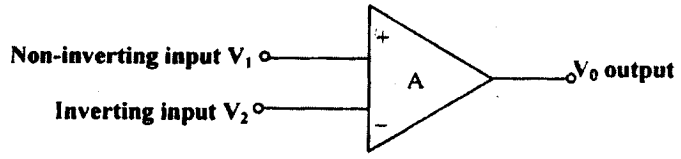


Fig.5.6 Schematic symbol of op-amp

In Fig.5.6,

v_1 = voltage at the non-inverting input (volts)

v_2 = voltage at the inverting input (volts)

v_o = output voltage (voltage)

All these are measured w.r.t. ground

A = large signal voltage gain that is specified on the data sheets for an op-amp

For amplifier, power supply and other pin connections are omitted. Since the input differential amplifier stage of the op-amp is designed to be operated in the differential mode, the differential inputs are designated by the (+) and (-) notations, the (+) input is used for non-inverting input. An ac signal (or dc voltage) applied to this input produces an in-phase (or same polarity) signal at the output. On the other hand the (-) input is the inverting input because an ac signal (or dc voltage) applied to this input produces an 180 out of phase (or opposite polarity) signal at the output.

5.3 CHARACTERISTICS OF AN IDEAL OP-AMP

An ideal op-amp exhibits the following electrical characteristics.

(1) Infinite voltage gain A_V.

(2) Infinite input resistance R_i, so that, almost any signal source can drive it and there is no loading of the preceding stage.

(3) Zero output resistance R_o, so that, output can drive an infinite number of other devices

(4) Zero output voltage when the input voltage is zero.

(5) Infinite bandwidth, so that, any frequency signal from 0 to ∞ Hz can be amplified with out attenuation.

(6) Infinite common mode rejection ratio so that output common mode noise voltage is zero.

(7) Infinite slew rate so that voltage changes occur simultaneously with input voltage changes.

There are practical op-amps that can be made to achieve some of these characteristic using a negative feedback arrangement. In particular, the input resistance, the output resistance, and bandwidth can be brought close to ideal values by this method.

EQUIVALENT CIRCUIT OF AN OP-AMP

Fig.5.7 shows an equivalent circuit of an op-amp. The circuit includes important values from the data sheets: A , R_i and R_o.

Note that A v_{id} is an equivalent Thevenin voltage source, and R_o is the Thevenin equivalent resistance looking back into the output terminal of an op-amp.

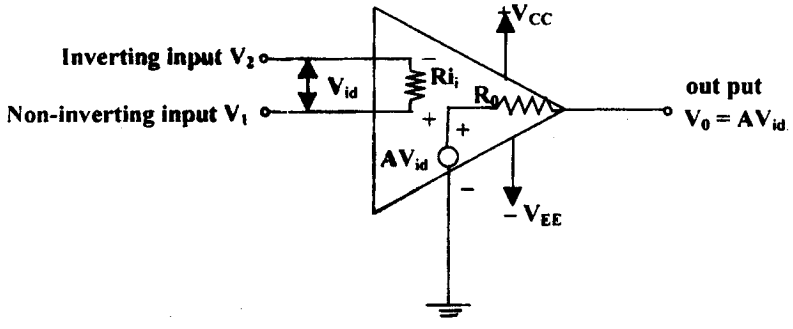


Fig.5.7 Equivalent circuit of op-amp

The equivalent circuit is useful in analyzing the basic operating principles of op-amps and in observing the effectiveness of feed back arrangement. For the circuit shown in Fig.5.7, the output voltage is

$$v_0 = Av_{id} = A\,(v_1 - v_2) \qquad (5.23)$$

where A = large- signal voltage gain

v_{id} = difference input voltage

v_1 = voltage at the non-inverting input terminal w.r.t. ground.

v_2 = voltage at the inverting input terminal w.r.t. ground.

Eq.(5.23) indicates that the output voltage v_0 is directly proportional to the algebraic difference between the two input voltages. In other words, the op-amp amplifies the difference between the two input voltages; it does not amplify the input signal voltages themselves. For this reason, the polarity of the output voltage depends upon the polarity of the difference voltage.

5.4 Properties of practical op-amp:

To enhance our understanding of op-amps, we need to define some parameters that appear on data sheet of practical op-amp.

(1) Voltage gain:

Fig.5.8 shows an idealized transfer characteristic

In the active region, the slope of the curve is the differential mode voltage gain A_d is defined as

$$A_d = \frac{\Delta v_0}{\Delta v_d}, \text{ where } v_d = v_1 - v_2, \text{ the differential mode input. } A_d \text{ is very large } \sim 10^6.$$

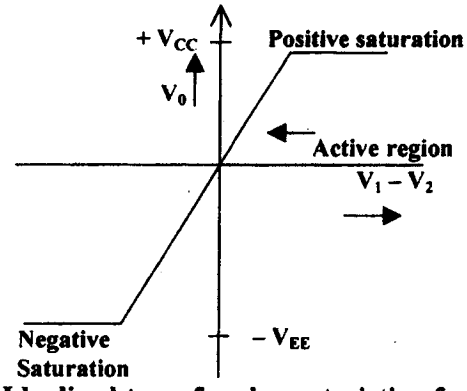


Fig.5.8 Idealized transfer characteristic of op-amp

To stabilize the voltage gain, negative feedback is always used. Fig 5.8 shows that the voltage gain is virtually zero when the output is at saturation level.

(2) Input impedance R_i:

It is the open loop incremental impedance looking into the two input terminals. It is large (~M Ω)

(3) Output impedance R_o:

It is the open loop impedance across the output. It is low (~ 100 Ω)

(4)): Common mode rejection ratio (CMRR):

The op-amp should ideally respond to a difference mode signal only. There will also be an output for the common mode input, because of the nature of the input circuit any (differential amplifier). The common mode gain $A_c = \frac{\Delta v_0}{\Delta v_c}$

The ratio of these two gains is defined as common mode rejection ratio

$$CMRR = \left|\frac{A_d}{A_c}\right| \quad \text{---------- (5.24)}$$

It is usually expressed in decibels, as $20 \log_{10}(CMRR) = 20 \log_{10} |A_d| - 20 \log_{10} |A_c|$

It is having a value 70 dB to 100 dB

Op-amps are further classified into two groups: general- purpose and special purpose. General- purpose op-amps may be used for a variety of applications such as integrator, differentiator, summing amplifier and others. An example of a widely used general-purpose op-amp is the 741/351. On the other hand, special purpose op-amps are used only for the specific applications they are designed for. For example the LM 380 op-amp can be used only for audio power applications;

The pin configuration of most widely used 741 op-amp is given below

It is the most commonly used general-purpose op-amp. It has an integrated 30pF MOS capacitor. It has high input impedance (> MΩ), low output impedance (750 Ω) and large voltage gain (200,000). From here onwards, all the discussions are confined to μA741 op-amp.

The electrical parameters of op-amp are defined in the following paragraphs.

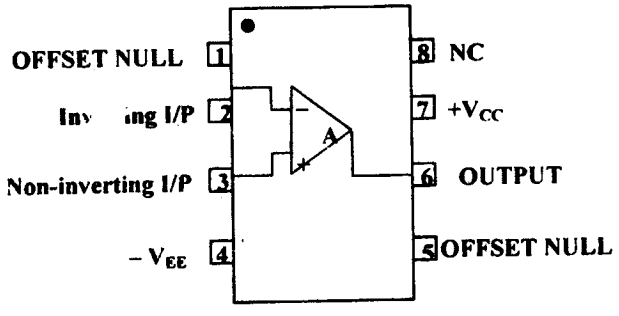


Fig.5.9 Pin configuration of μA-741 op-amp

Input offset voltage: Input offset voltage is the voltage that must be applied between the two input terminals of an op-amp to null the output as shown in Fig.5.10. In Fig.5.10, V_{dc1} and V_{dc2} are dc voltages and R_s represents the source resistance. We denote input offset voltage by V_{i0}. This voltage V_{i0} could be positive or negative;

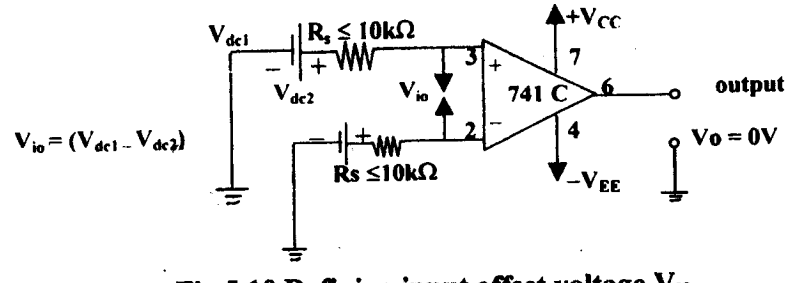


Fig.5.10 Defining input offset voltage V_{i0}

For 741C, the maximum value of V_{io} is 6 mV DC. The smaller the value of v_{io}, the better the input terminals are matched.

Input offset Current:

The algebraic difference between the currents into the inverting and non-inverting terminals is referred to as input offset current I_{io} (see Fig.5.11). In the form of an equation

$$I_{io} = |I_{B1} - I_{B2}|$$

where I_{b1} is the current into the non-inverting input I_{b2} is the current into the inverting input

The input offset current for the 741C is 200 nA maximum. As the matching between the two input terminals is improved, the difference between I_{B1} and I_{B2} becomes smaller; that is, the I_{io} value decreases further.

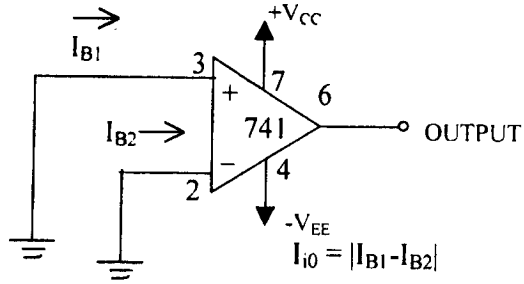


Fig.5.11 defining input offset current I_{i0}

Input Bias current:

Input bias current I_B is the average of the currents that flow into the inverting and non-inverting input terminals of the op-amp. In equation form

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

I_B = 500 nA maximum for the 741C, where as I_B for the precision 741C is ± 7 nA

Note: The input currents I_{B1} and I_{B2} are actually the base currents of the first differential amplifier stage.

Differential input resistance:

Differential i/p resistance R_i (often referred to as i/p resistance) is the equivalent resistance that can be measured at either the inverting or non-inverting i/p terminal with the other terminal grounded. For the 741C the i/p resistance is relatively high 2 MΩ.

Input capacitance: Input capacitance C_i is the equivalent capacitance that can be measured at either the inverting or non-inverting terminal with the other terminal grounded. A typical value of C_i is 4.4 pF for the 741C. This parameter is not listed in all op-amp-data sheets.

Offset voltage adjustment ratio: One of the features of the 741 family op-amps is an offset voltage null capability. The 741 op-amps pins 1 and 5 marked as offset null are for this purpose. As shown in Fig.5.11, a 10kΩ potentiometer can be connected between offset null pins 1 and 5, and the wiper of the potentiometer can be connected to the negative supply $-V_{EE}$.. By varying the potentiometer, the output offset voltage can be reduced to zero volts. Thus the offset voltage adjustment range is the range through which the i/p offset voltage can be adjusted by varying the 10kΩ potentiometer. For the 741C, the offset voltage adjustment range is ±15mV. Very few op-amps have the offset voltage null capability. This means that for most op-amps, we have to design an offset voltage compensating network in order to reduce the o/p offset voltage to zero.

Common mode rejection ratio: The common-mode rejection ratio (CMRR) is defined in several essentially equivalent ways by the various manufactures. Generally it can be defined as the ratio of the differential voltage gain A_d to the common mode voltage gain A_{cm}. That is

$$CMRR = \frac{A_d}{A_{cm}}$$

The differential voltage gain A_d is the same as the large signal voltage gain A, which is specified on the data sheets; The common mode voltage gain can be determined from the circuit.

$$A_{cm} = \frac{v_{ocm}}{v_{cm}}.$$

v_{0cm} = o/p common mode voltage.

v_{cm} = i/p common mode voltage.

A_{cm} = common mode voltage gain.

Generally the A_{cm} is very small and $A_d = A$ is very large; therefore the CMRR is very large, being a large value, CMRR is most often expressed is decibels (dB) for the 741C, CMRR is 90 dB typically.

Slew rate (S.R): Slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per microseconds. In equation form

$$S.R = \frac{dv_o}{dt} / \text{maximum } V/\mu s$$

Slew rate indicates, how rapidly the output of an op-amp can change in response to changes in the input frequency with input amplitude constant. The slew rate changes with change in voltage gain and is normally specified at unity (+1) gain. The slew rate of an op-amp is fixed, therefore if the slope requirements of the o/p signal are greater than the slew rate, distortion occurs. The slew rate is one of the important factors in selecting the op-amp for an

application, particularly at relatively high frequencies. One of the drawbacks of the 741C is its low slew rate (0.5 V/μs).

5.5 OPEN-LOOP OP-AMP CONFIGURATIONS

In the case of amplifiers, the term "open-loop" indicates that no connections either direct or via another network exists between the o/p and i/p terminals. That is, the o/p signal is not fedback in any form as part of the input signal and the "loop" that would have been formed with feedback is open.

When connected in open loop configuration, the op-amp simply functions as a high gain amplifier. There are three open loop op-amp configurations:

1. The differential amplifier.
2. The inverting amplifier.
3. The non-inverting amplifier.

The differential amplifier:

Fig.5.12 shows the open loop differential amplifier in which input signals v_{is1} and v_{is2} are applied to the positive and negative input terminals.

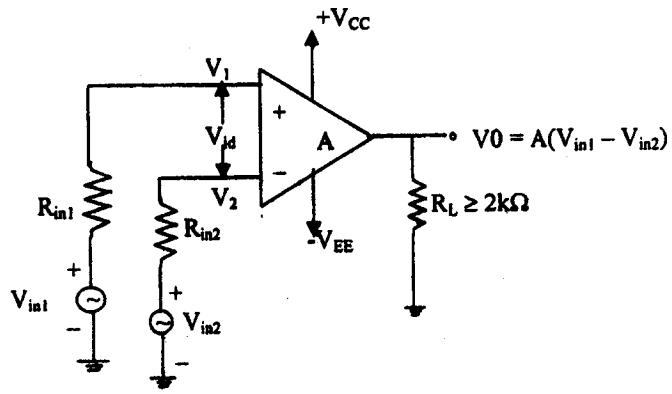


Fig.5.12 Open loop differential amplifier

Since the op-amp amplifies the difference between the two input signals, this configuration is called the **Differential amplifier**. The op amp is a versatile device because it amplifies both ac and dc input signals. This means that v_{is1} and v_{is2} could be either ac or dc voltages. The source resistance R_{in1} and R_{in2} are normally negligible compared to the input resistance R_i. Therefore, the voltage drops across the resistors can be assumed to be zero, which then implies that $v_1 = v_{in1}$, and $v_2 = v_{in2}$. Substituting these values of v_1 and v_2 in equation for output voltage, we get

$v_0 = A (v_{in1}-v_{in2})$

Thus, as expected the output voltage is equal to voltage gain A times the difference between the two input voltages. Also notice that the polarity of the output voltage is dependent on the polarity of the input difference voltage ($v_{in1}-v_{in2}$). In open loop configurations, gain A is

THE INVERTING AMPLIFIER

In the inverting amplifier, only one input is applied and that, to the inverting input terminal. The non-inverting input terminal is grounded. Since $v_1 = 0$ and $v_2 = v_{in}$.

$V_0 = - AV_{in}$

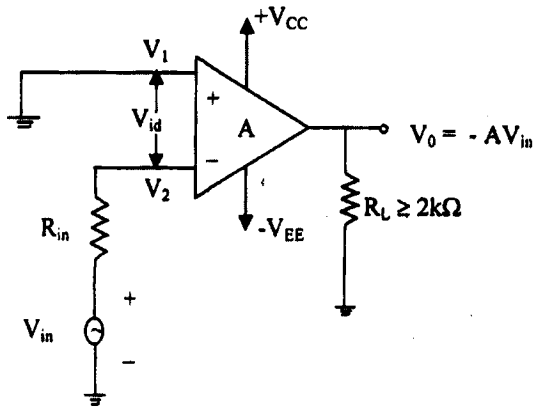


Fig 5.13 Inverting amplifier

The negative sign indicates that the output voltage is out of phase with respect to input by 180^0 or is of opposite polarity. Thus in the inverting amplifier the input signal is amplified by gain A and is also inverted at the output.

THE NON-INVERTING AMPLIFIER

Fig.5.14 shows the open loop configurations of non inverting amplifier. In this configuration, the input is applied to the non inverting input terminal and the inverting input terminal is grounded. In the circuit shown below $v_1 = v_{in}$ and $v_2 = 0v$. Therefore, according to equation $v_0 = Av_{in}$. This means that the output voltage is larger than the input voltage. By gain A and is in phase with input signal. In all the three open loop configurations, any input signal that is only slightly greater than zero drives the output to saturation level. This results from the very high gain A of the op-amp. Thus when operated in open loop, the output of the op-amp is either at negative saturation or positive saturation or switches between positive and negative saturation levels. Due to this reason, the open loop configurations are not used in linear applications.

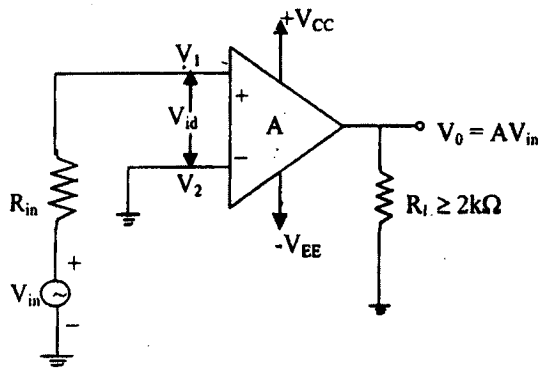


Fig.5.14 Non-inverting amplifier

5.6 SUMMARY

A differential amplifier consists of two symmetrical common emitter stages and is capable of amplifying the difference between two input signals. Differential amplifier is capable of amplifying ac as well as dc input signals because it employs direct coupling. For proper operation of the differential amplifier, a transistor array and matched components must be used. The differential amplifier can be biased by using emitter bias (a combination of R_E and V_{EE}), a constant current bias. The constant current bias is more preferable in differential amplifiers because it maintains the infinite input impedance for all the desired values of emitter currents I_E.

An ideal op-amp has infinite voltage gain, input resistance, CMRR and slew rate together with zero output resistance and output offset voltage. The equivalent circuit of op-amp is useful in analyzing the basic operating principles of an op-amp and in observing the effects of feedback arrangements. The voltage transfer characteristic curve of an op-amp is the graph of output voltage versus the differential input voltage. Differential, inverting and non-inverting amplifiers are the three open loop op-amp configurations in which the output signal is not fed back in any

form as part of the input signal. When operated in the open loop; generally the op-amp's output is either at positive or negative saturation or switches between positive and negative saturation levels. This action is undesirable in linear applications, hence the op-amp's are rarely used in open loop configuration for the linear applications.

5.7 KEY TERMINOLOGY

Configuration: Design of the circuit by employing the various possible networks is called configuration.

Decibel (dB): 1/ tenth of a Bell; Bell is unit of power ratio

Milli volts (mV); 1/1000 of a volt

Nano Ampere (nA); $1nA = 10^{-9}$ A

Pico Farad (pF); $1pF = 10^{-12}$ F

Saturation: when input voltage in the circuit exceeds a certain value, the output goes to the maximum value is called saturation

Pot (Potentiometer): variable wire wound resistor

5.8 SELF-ASSESSMENT QUESTIONS

LONG ANSWER QUESTIONS:

1. Explain the working of differential amplifier with a diagram.
2. Derive expressions for the common mode voltage gain and differential mode voltage gain of a transistor differential amplifier and show that the common mode rejection ratio increases with emitter resistance.

4. What are the important stages of a typical operational amplifier?
5. How far IC 741 electrical characteristics are nearer to the ideal characteristic of op-amp.
6. Explain the terms input offset voltage; input offset current, input bias current.
7. Explain why op-amp is not used in open loop configuration for linear applications.
8. An Op amp has a CMRR value of 60 dB. Find the differential mode gain if the common mode gain is 3.

5.9 TEXT AND REFERENCE BOOKS

TEXT BOOKS:

1. Integrated Electronics by Millman and Halkias
2. Basic Electronics and Linear Circuits - Bhargava etc
3. Electronic devices and circuit theory by Robert Boylsted and Louis Neshalasky(PHI)
4. Basic Electronics by DC Tayal, Himalaya Publish Co.,

REFERENCE BOOKS

1. A text lab manual in Electronics by ZBAR (Tata Mc graw Hill)
2. Electronics fundamentals by JD Ryder
3. Op.Amp and linear integrated Circuits by Ramakant Gayakwad
4. Semiconductor Electronics by A K. Sharma
   New Age International Publishers
5. Foundations of Electronics
   By D. Chattopadhyay, PC Rakshit, B. Saha, M.N. Purohit
   Second Edition, Wiley Eastern Ltd., .

OPERATIONAL AMPLIFIERS - II

OBJECTIVES OF THE LESSON

To understand 1). The effect of negative feedback on Op Amp, 2). The concept of virtual ground. 3). the working of inverting, non-inverting and summing amplifiers

STRUCTURE OF THE LESSON

6.1 INTRODUCTION

As the open loop gain of op-amp is very high, only very small signals (of the order of micro-volts or less) having very low frequency may be amplified accurately without distortion. However, signals this small are very susceptible to noise. Besides being large the open loop gain of the op-amp is not constant. The voltage gain varies with changes in temperature and power supply as well as with mass production techniques. The variations in voltage gain are relatively large in open-loop op-amp, in particular, which makes the open-loop op-amp unsuitable for many linear applications. In most linear applications, the output is proportional to the input and is of the same type.

Further, the bandwidth (band of frequencies for which the gain remains constant) of most open-loop op-amps is negligibly small - almost a zero. For this reason, the open-loop op-amp is impractical in ac applications. For instance, the open loop bandwidth of the 741C is approximately 5Hz. However, in almost all ac applications a bandwidth larger than 5Hz is needed.

Because of the above stated reasons, the open loop op-amp is generally not used in linear applications. Nevertheless, in certain applications, the open-loop op-amp is purposely used as a nonlinear device; that is a square ware output is obtained by deliberately applying a relatively large input signal. Open-loop op-amp configurations are most suitable in such applications.

We will be able to select as well as control the gain of the op-amp, if we introduce a modification in the basic circuit. This modification involves the use of feedback, that is, an output signal is fed back to the input either directly or via another network. If the signal fed back is of opposite polarity or out of phase by 180^0 with respect to input signal, the feedback is called of **Negative feedback.** An amplifier with negative feedback has a self - correcting ability against any change in output voltage caused by changes in environmental conditions. Negative feedback is also known as degenerative feedback because when used it degenerates (reduces) the output voltage amplitude and in turn reduces the output gain.

Suppose the signal fed back is in phase with the input signal, the feedback is called **Positive feedback.** In positive feedback, the feed back signal aids the input signal. For this reason it is also known as regenerative feedback. Positive feedback is necessary in oscillator circuits.

Therefore negative feedback stabilizes the gain, increases the bandwidth and changes the input and output resistances, when used in amplifiers. The price paid for these improvements is reduced voltage gain. Other benefits of negative feedback include a decrease in harmonic distortion and reduction in effect of input offset voltage at the output. Negative feedback also reduces the effect of variation in temperature and supply voltages on the output of the op-amp

6.2 Effect of negative feedback on closed loop Op Amp parameters:

6.2.1 Closed loop voltage gain:

As defined previously, the closed loop voltage gain

$$A_f = \frac{v_o}{v_{in}} \qquad \ldots\ldots \quad (6.1)$$

However by equation $v_0 = A\,(v_1 - v_2)$,

Referring to Fig.6.2, we see that

$v_1 = v_{in}$

$$v_2 = v_f = \frac{R_1 v_0}{R_1 + R_F} \text{ since } R_i >> R_1$$

Therefore $v_0 = A\left(v_{in} - \frac{R_1 v_0}{R_1 + R_F}\right)$

Rearranging the above equation, we get

$$v_o = \frac{A(R_1 + R_F)\, v_{in}}{R_1 + R_F + AR_1}$$

$$\text{Thus } A_F = \frac{v_o}{v_{in}} = \frac{A(R_1 + R_F)}{R_1 + R_F + AR_1} \text{ (exact)} \quad \text{--------- (6.2)}$$

Generally, A is very large (typically 10^6), therefore,

$AR_1 >> R_1+R_F$ and $R_1+R_F+AR_1 \cong AR_1$

$$\text{Thus } A_F = \frac{v_o}{v_{in}} = 1 + \frac{R_F}{R_1} \text{ (ideal)} \quad \text{--------- (6.3)}$$

Eq.(6.3) is important because, it shows that the gain of a voltage series feedback amplifier is determined by the ratio of the two resistors, R_1 and R_F. For instance, if a gain of 11 is desired, we can then choose R_1 = 1kΩ and R_F = 10kΩ or R_1 = 100Ω and R_F = 1kΩ.

Another interesting result can be obtained from Eq.(6.3). As defined previously, the gain or the feedback circuit (B) is the ratio of v_f to v_0. Referring to Fig.6.2, the gain is

$$B = \frac{v_f}{v_o}$$

$$B = \frac{R_1 v_0}{(R_1 + R_F) v_0} = \frac{R_1}{R_1 + R_F} \quad \text{- --------- (6.4)}$$

Comparing Eq.(6.3) and Eq.(6.4) we can conclude that

$$A_F = \frac{1}{B} \text{ (ideal)} \quad \text{---------- (6.5)}$$

This means that gain of the feed back circuit is the reciprocal of the closed loop voltage gain. In other words for given R_1 and R_F the values of A_F and B are fixed. Besides that Eq.6.5 is an alternative to Eq.6.3. Finally, the closed loop voltage gain A_F can be expressed in terms or open loop gain A and feedback circuit gain B by rearranging Eq. (6.2) in the following manner, we get

$$A_F = \frac{A\left(\frac{R_1 + R_F}{R_1 + R_F}\right)}{\frac{R_1 + R_F}{R_1 + R_F} + \frac{AR_1}{R_1 + R_F}} \quad \text{---------- (6.6)}$$

Using Eq.(6.4), we get $A_F = \frac{A}{1+AB}$ ---------- (6.7)

Where A_F = closed loop gain

A = open loop gain

B = gain of the feed back circuit ; AB = "loop gain"

6.2.2 Effect of feedback on Input resistance

A voltage series feedback amplifier with the op-amp equivalent circuit is shown in Fig .6.3. In this circuit, R_i is the input resistance (open-loop) of the op-amp, and R_{if} is the input resistance of the feedback amplifier. The input resistance with feedback is defined as

$$R_{if} = \frac{v_{in}}{i_{in}} = \frac{v_{in}}{v_{id}/R_i} \quad \text{---------- (6.8)}$$

However,

$$V_{id} = \frac{v_0}{A} \text{ and } v_0 = \frac{A}{1+AB} v_{in} \quad \text{---------- (6.9)}$$

$$R_{if} = R_i . \frac{v_{in}}{v_0 / A} \quad \text{---------- (6.10)}$$

$$R_{if} = AR_i \frac{v_{in}}{\frac{Av_{in}}{(1+AB)}} = R_i(1+AB) \quad \text{---------- (6.11)}$$

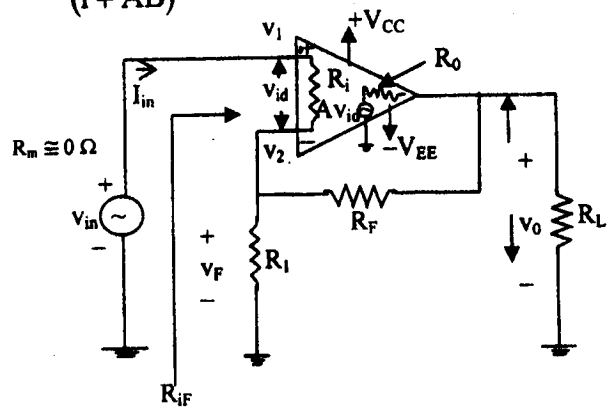


Fig.6.3 Circuit for deriving input resistance with feedback.

It means, the input resistance of the op-amp with feedback is (1+AB) times that input resistance without feedback.

6.2.3 Output resistance with feedback:

Output resistance is the resistance determined looking back into the feedback amplifier from the output terminal, as shown in Fig 6.4. This resistance can be obtained by using Thevenin's theorem for dependent sources. Specifically, to find output resistance with feed back R_{OF}, reduce the independent source v_{in} to zero, apply an external voltage v_o and then calculate the resulting current i_o in short the R_{OF} is defined as follows:

$$R_{OF} = \frac{v_o}{i_o}.$$

Writing Kirchoff's current equation at the output node N, we get

$$i_o = i_a + i_b \qquad \text{----------(6.12)}$$

Since $R_F + R_1 \| R_i >> R_0$, $i_a >> i_b$ therefore

$$i_o \cong i_a \qquad \text{---------- (6.13)}$$

The current i_o can be found by writing Kirchoff's voltage equation for the output loop

$$v_0 - R_0 i_0 - A v_{id} = 0 \qquad \text{---------- (6.14)}$$

$$i_0 = \frac{v_0 - A v_{id}}{R_0}$$

$$v_{id} = v_1 - v_2 = -v_f = -\frac{R_1 v_0}{R_1 + R_F} = -Bv_o$$

therefore $$i_0 = \frac{v_0 + A.Bv_0}{R_0}$$

substituting the value of i_o in equation, we get

$$R_{oF} = \frac{v_0}{(v_0 + ABv_0)/R_0} = \frac{R_0}{1 + AB} \qquad \text{---------- (6.15)}$$

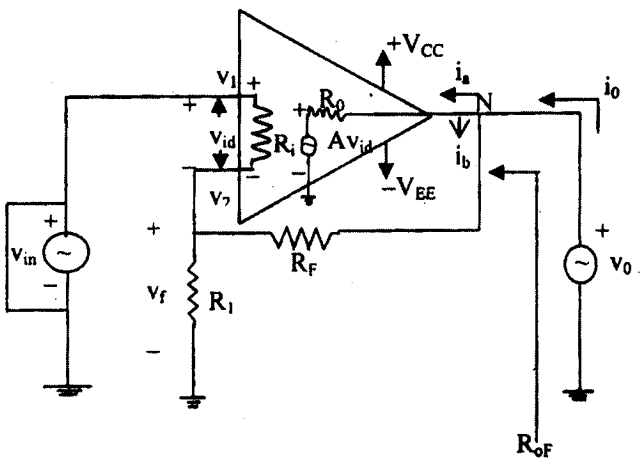


Fig 6.4 Diagram to derive the output resistance with feedback

This result shows that the output resistance of the voltage series feedback amplifier is 1/(1+AB) times the output resistance R_o of the op-amp. That is, the output resistance of the op-amp with feedback is much smaller than the output resistance without feedback.

6.2.4 Bandwidth with feedback:

The bandwidth of an amplifier is defined as the band (range) of frequencies for which the gain remains constant. Manufacturers generally specify either the gain bandwidth product or supply open loop gain versus frequency curve for the op-amp. For the 741 op-amp the latter is typical.

The open loop gain versus frequency curve of the 741C op-amp is shown in Fig 6.5. From this curve for a gain of 200,000 the bandwidth is approximately 5Hz. In other extreme, the bandwidth is approximately 1MHz when the gain is unity. The frequency at which the gain equals 1 is known as **Unity gain-band width.** It is the maximum frequency, the op-amps can be used for. Furthermore, the gain bandwidth product obtained from the open loop gain versus frequency curve of Fig.6.5 is equal to the unity gain bandwidth of an op-amp. However this holds true only for those op-amps like 741, which have just one break frequency below unity gain bandwidth.

Since the gain bandwidth product is constant, obviously the higher the gain the smaller the bandwidth and vice versa. As we have seen if negative feedback is used gain A decreases to A / 1+AB. Therefore to obtain the closed loop bandwidth, the open loop bandwidth must be multiplied by the same factor, by which the gain is divided, that is, by the factor (1+AB).

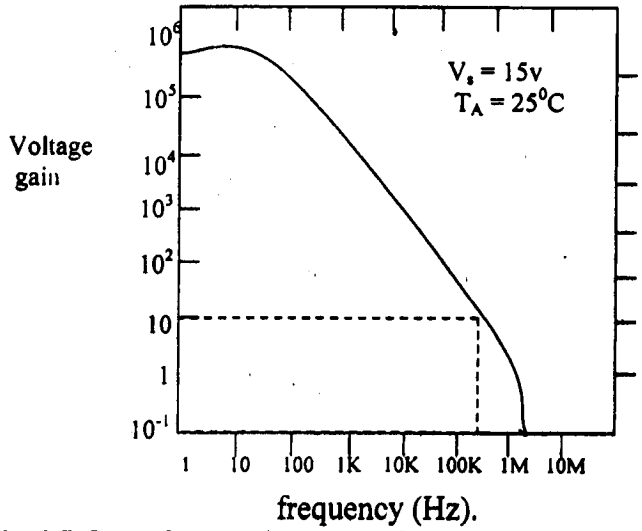


Fig 6.5 Open loop gain versus frequency curve of 741c.

In short,

bandwidth with feed back = (band width without feedback) (1+AB)

$f_F = f_0 (1+AB)$ ---------- (6.16)

or alternatively,

f_F = unity gain band width/closed loop gain = U.G.B.W /A_F ---------- (6.17)

The closed loop bandwidth can also be determined from the open loop gain versus frequency plot. To do this we locate the closed loop voltage gain value on the gain axis and draw a parallel line through this value to the frequency axis. Then we project the point of inter section of the line with the curve on the frequency axis and read the value of the closed loop bandwidth. Using this procedure in Fig 6.5, the bandwidth is approximately 100 KHz. for a closed loop gain of 10.

6.3 CONCEPT OF VIRTUAL GROUND

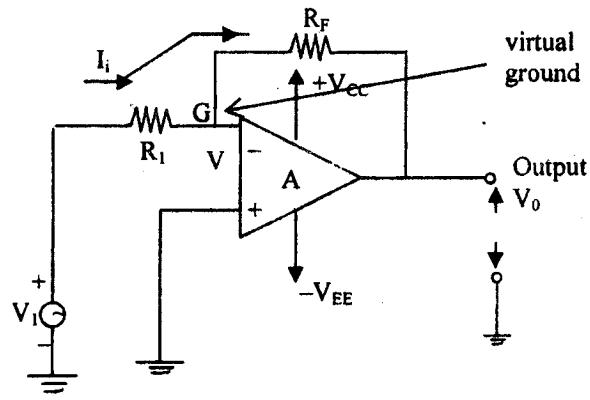


Fig.6.7 Op amp with negative feedback

The branch point G has a special significance in operational amplifier. This may be illustrated by determining the effective impedance between G and ground which is given by the ratio of V_1 to the input current,

$$Z_G = \frac{V_1}{I_i} = \frac{V_1 R_F}{V_1 - V_0} = \frac{R_F}{1 - \frac{V_0}{V_1}} = \frac{R_F}{1 + A}$$

According to this equation, the impedance of G with respect to ground is very low if the gain is very large. Typical values of $R_F = 10^4\ \Omega$ and $A = 10^5$, so that the impedance is 0.1 ohms. This low impedance results from the negative feedback voltage, which cancels the input signals at G and tends to keep the branch point at ground potential. For this reason, point G in op amp is called a **Virtual ground**. Although G is kept at ground

potential by feedback action, no current ground exists at this point. The virtual ground G shows immediately that the impedance viewed from the input terminals is equal to R_1. Here the term virtual ground is used to imply that although the feedback from output to input R_f serves to keep the voltage at G at zero, no current flows into the amplifier inputs i.e. no current flows into short.

6.4 INVERTING AMPLIFIER: The basic inverting amplifier with an input resistor R_1 and feedback resistor R_F is shown in Fig 6.7a.

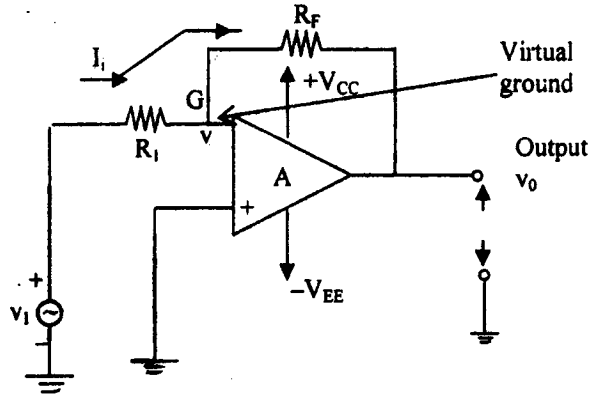


Fig 6.7a Inverting amplifier.

The non-inverting input terminal is grounded and the input voltage is v_1 and the output voltage is v_0. Since the gain 'A' of the operational amplifier is very large, the voltage v at the inverting input terminal is very small. In fact, the voltage v is very close to the ground potential. That is, although the point G is not actually connected to the ground, it is held virtually at ground potential irrespective of magnitudes or the potentials v_1 and v_0, the current i, flowing through resistor R_1 is given by $i = \frac{v_1 - v}{R_1}$. Assuming that the operational amplifier is ideal, having infinite input impedance, the current i will flow through R_F and not into the op-amp. Applying the Kirchoff's current law at the point G., we can have

$$\frac{v_1 - v}{R_1} = \frac{v - v_0}{R_F} \qquad \text{--------- (6.18)}$$

Since the point 'G' is virtually ground i.e. $v \approx 0$

From Eq.(6.18), we get $\frac{v_i}{R_1} = \frac{-v_0}{R_F}$

Rearranging Eq.(6.18).

We have $\frac{v_0}{v_i} = -\frac{R_F}{R_1}$ ---------- (6.19)

The ratio of the output voltage to the input voltage is the gain of the amplifier. Hence the voltage gain is the ratio of feedback resistor R_F to the input resistance R_1. The negative sign indicates that the output voltage is inverted w.r.t. the input voltage. The input resistance (R_{in}) of the whole amplifier is given by the ratio of voltage v_1 and the input current $\frac{v_i - v}{R_1}$ that is

$$R_{in} = \frac{v_i}{\frac{v_i - v}{R_1}} \approx R_1 \qquad \text{---------- (6.20)}$$

since $v \approx 0$, note that R_{in} refers to the whole of the amplifier not to the op-amp which has an infinite input resistance

6.4.1 SCALE CHANGER

If use ratio $\frac{R_F}{R_1}$ is denoted by k, a real constant, we get $v_0 = -kv_1$. That is, input voltage has been multiplied by the factor '- k' to give the output voltage scale. The circuit shown in Fig 6.7, acts as scale changer. For such applications, precision resistors are used to get accurate values for the scale factor 'k'

6.4.2 Phase shifter:

If the resistance R_F and R_1 in the circuit are replaced respectively by impedances z_F an z_1 which are equal in magnitude but differ in phase angle, we can write

$$\frac{v_0}{v_i} = -\frac{z_F}{z_i} = -\frac{|z_F|}{|z_1|}\cdot\frac{\exp(j\phi_F)}{\exp(j\phi_1)} = \frac{|z_F|}{|z_1|} e^{j[\Pi + \phi_F - \phi_1]}$$

$$\frac{v_0}{v_i} = \exp j[\Pi + \phi_F - \phi_1] \qquad \text{---------- (6.21)}$$

Since $|z_F| = |z_1|$ and $e^{j\Pi} = -1$, the angles ϕ_F and ϕ_1 represent respectively, phase angles of the independences z_F and z_1. The circuit is capable of shifting the phase of a

sinusoidal input signal voltage without changing its magnitude. The amount of phase shift can be any thing between 0 and 360^0.

6.5 NON- INVERTING AMPLIFIER

The circuit diagram of non-inverting amplifier is shown in Fig.6.8.

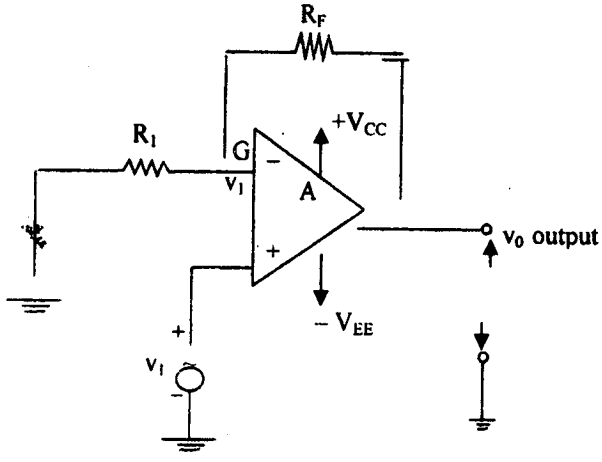


Fig 6.8 Circuit of non-inverting amplifier.

In this case, the input voltage v_i is applied to the non-inverting input terminal. The potential of the point G is also v_1, since the op-amp gain is infinite. Then, as mentioned before, since the input current to the op-amp is negligible, we can write using Kirchoff's current law at the point G.

$$\frac{v_0 - v_1}{R_F} = \frac{v_1}{R_1} \qquad \text{--------- (6.22)}$$

Therefore, the gain of the amplifier is

$$\frac{v_0}{v_i} = 1 + \frac{R_F}{R_1} \qquad \text{--------- (6.23)}$$

Since the gain of the op-amp is 1 plus the ratio of the two resistors R_F and R_1. And also note that the output voltage is in phase with the input voltage.

6.6 SUMMING AMPLIFIER:

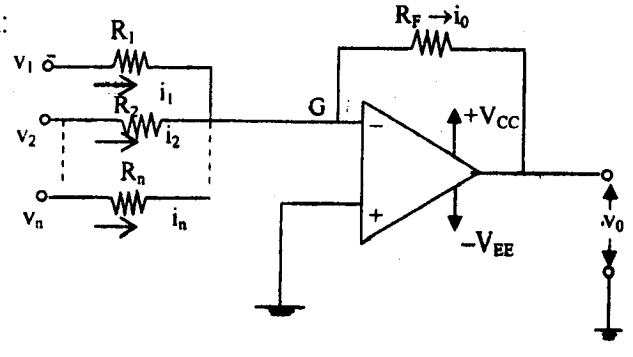


Fig 6.9 An adder or summing amplifier.

$$i_1 + i_2 + \ldots\ldots\ldots + i_n = i_0 \qquad \text{---------- (6.24)}$$

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \ldots\ldots\ldots + \frac{v_n}{R_n} = -\frac{v_0}{R_F} \qquad \text{---------- (6.25)}$$

Solving Eq.(6.25) for v_0, we get

$$v_0 = -R_F \left[\frac{v_1}{R_1} + \frac{v_2}{R_2} + \ldots\ldots\ldots + \frac{v_n}{R_n}\right] \qquad \text{---------- (6.26)}$$

If $R_1 = R_2 \ldots\ldots = R_n = R$, we obtain $v_0 = -\frac{R_F}{R}[v_1+v_2+\ldots.+v_n]$ --------(6.27)

Again if $R_F = R$, we get

$v_0 = -[v_1+v_2+\ldots..+v_n]$ --------(6.28)

Eq.(6.28) shows that the output voltage v_0 is numerically equal to the negative sum of all input voltages v_1 through v_n. Hence it was named as adder or summing amplifier.

6.7 OP AMP VOLTAGE FOLLOWER

DC voltage follower

The simple configuration Fig.6.10 approaches the ideal voltage follower. Since the two inputs are tied together, then $V_0 = V_S$ and the output follows the input.

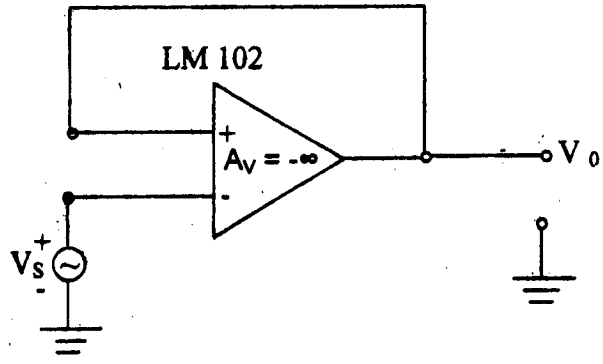


Fig 6.10 Voltage follower

The LM102 (National semiconductor corporation) is specifically designed for voltage follower usage and has very high input resistance, very low input current and very low output resistance.

AC VOLTAGE FOLLOWER

A circuit for an ac voltage follower is shown in Fig 6.11 using the LM102 OP-AMP. This circuit is used to provide impedance buffering. Thus, it can be used to connect a single source with high internal source resistance to a load of low impedance. This load

may be capacitive or resistive. We assume that C_1 and C_2 represent short circuits at all frequencies of operation of this circuit. Resistors R_1 and R_2 are used to provide RC coupling and allow a path for the dc input current into the non-inverting terminal. In the absence of the boot-strapping capacitor C_2, the ac signal source would see an input resistance only $R_1 + R_2 = 300K\Omega$.

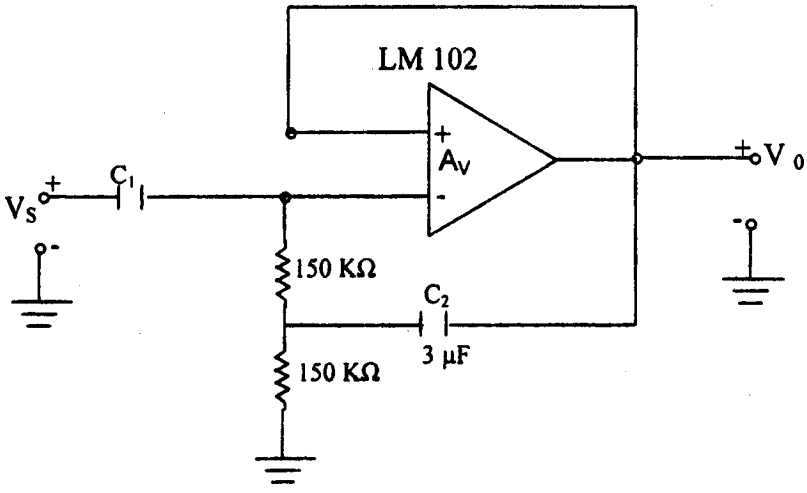


Fig 6.11 AC voltage follower

Since the LM102 is connected as a voltage follower, the voltage gain between the output terminal and the non -inverting terminal is A_V =+1. Hence in the presence of boot strapping capacitor C_2, the input resistance becomes approximately

$$R_{in} = \frac{R_1}{1 - A_V}$$

For typical circuit components

$$R_{in} = 10M\Omega \; at \; f = 100Hz$$

And $$R_{in} = 100M\Omega \; at \; f = 1Hz$$

6.8 OP AMP CURRENT FOLLOWER

In an inverting amplifier, if the input resistance R_1 is zero then the resulting circuit in known as "Current Follower".

Using this current follower circuit, we can measure very small currents ($\sim 10^{-9}$A).

At the summing point S, $I_N = I_1 + I_f$

$$\therefore V_0 = -I_N R_f \; (I_1 = 0)$$

In a currents follower $I_{in} = I_{out}$.

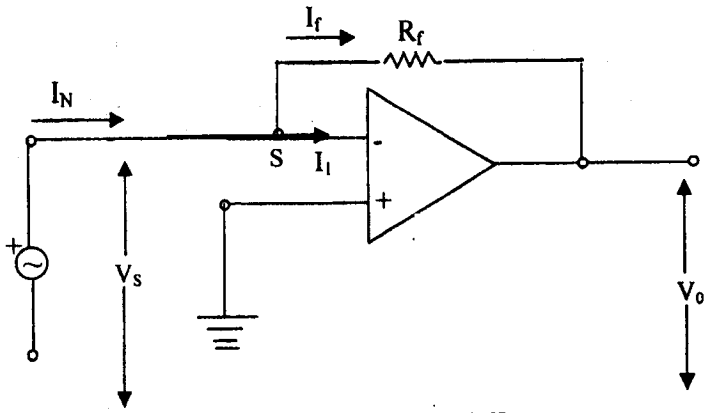


Fig 6. 12. Current follower

6.9 SUMMARY

Open loop op amp configuration is unsuitable for linear applications because of its very high voltage gain as well as its variation with temperature, power supply etc. Therefore, we can select, as well as, control the gain of the op-amp, if we introduce a modification in the basic circuit This modification involves the use of feedback, that is, the output signal is fed back to the input either directly or via another network. If the signal feed-back is 180^0 out of phase with respect to. the input signals. Such a type of feedback is called **negative feedback**. Negative feedback is also known as **degenerative feedback**, because when used, it reduces the output voltage and in turn reduces the voltage gain and stabilizes the gain.

On the other hand if the signal fed back is in phase with the input signal such type of feedback is called **positive feedback**. Positive feedback is also known as **regenerative feedback**, because the feedback signals aid the input signal. Positive feedback is needed in the oscillator circuits.

There are four types of closed loop configurations using negative feedback: voltage series, voltage shunt, current series and current shunt. Further these configurations are labeled according to whether the voltage or current is fed back to the input in series or in parallel. The voltage series negative feedback configuration is generally known as non inverting amplifier if the feedback and the ideal closed loop voltage gain of the configuration depends only on the feedback network (components) and is independent of the internal or open loop gain A of the op-amp.

Introduction of the negative feedback in non-inverting amplifier, increases the input impedance and bandwidth and decreases the output resistance; total output- offset

voltage and the effect of varying environmental conditions on the gain. The voltage follower is the special case of non-inverting amplifier.

Summing, scaling amplifiers can be constructed by using inverting, non-inverting and differential configurations. The integrator and differentiator are most widely used in signal wave shaping applications. Besides, the integrator is used in analog computers and the differentiator is used as a rate of change detector in FM modulators.

6.10 KEY TERMINOLOGY

1. Active components: Active components can generate voltage or current or power
   Example: Battery, signal generator.
2. Passive components: The components only dissipate power
   Example: Resistor, capacitor.
3. Degenerative feedback: The output voltage is fed back to the input such that this voltage is 180^0 out of phase w.r.t. the source voltage. As a result, the effective input voltage decreases (degenerates) and this is called degenerative feedback or negative feedback.

6.11 SELF-ASSESSMENT QUESTIONS

1. Mention two reasons why an open loop op-amp is unsuitable for linear applications.
2. What do you mean by feedback? List two types of feedback. Which type is used in linear applications?
3. Describe the four negative feedback configurations. Which configuration is most widely used?
4. Explain briefly why negative feedback is desirable in amplifier applications.
5. How does negative feedback affect the close loop voltage gain, input resistance, output resistance and band width of voltage series feedback amplifier (closed loop non- inverting amplifier)
6. Explain the inverting and non-inverting amplifiers?

6.12 TEXT AND REFERENCE BOOKS

(1) Operational Amplifiers and Linear Integrated Circuit Technology by Ramakanth A. Gaykwad Prentice Hall Inc.,

(2) Basic Electronics by DC Tayal, Himalaya Publish Co.,

(3) Semi Conductor Electronics by A K. Sharma
New Age International Publishers

(4) Foundations of Electronics By D. Chattopadhyay, PC Rakshit, B. Saha, M.N. Purohit , Second Edition, Wiley Eastern Ltd.,

OPERATIONAL AMPLIFIERS - III

OBJECTIVES OF THE LESSON

To learn about the various applications of OP-Amp like voltage follower,. comparator, voltage regulator, free running multivibrator , developing circuits to solve simple second order differential equation, logarithmic amplifier, anti-log amplifier, logarithmic multiplier etc..

STRUCTURE OF THE LESSON

7.1 INTRODUCTION

The variations in voltage gain are relatively large in open-loop op-amp, in particular, which makes the open-loop op-amp unsuitable for many linear applications. In most linear applications, the output is proportional to the input and is of the same type.

Further the bandwidth (band of frequencies for which the gain remains constant) of most open-loop op-amps is negligibly small - almost a zero. For this reason, the open-loop op-amp is impractical in AC applications. For instance the open loop bandwidth of the 741C is approximately 5Hz. However, in almost all ac applications a bandwidth larger than 5 Hz is needed.

Because of the above stated reasons, the open loop op-amp is generally not used in linear applications. Nevertheless, in certain applications the open-loop op-amp is purposely used as a nonlinear device; that is a square ware output is obtained by

deliberately applying a relatively large input signal. Open-loop op-amp configurations are most suitable in such applications.

Op-amps have many applications. Some are described below

7.2 THE INTEGRATOR

A circuit in which the output voltage waveform is the integral of the input waveform is the integrator or the integration amplifier. Such a circuit obtained by using a basic inverting amplifier configuration, if the feedback resistor R_F is replaced by a capacitor C_F and the relevant circuit is shown in Fig 7.1a.

Fig.7.1(b, c) input and ideal output waveforms using sine wave and square wave respectively

$R_1 C_F = 1$ second and $v_{oo} = 0V$ assumed.

The expression for the output voltage v_0 can be obtained by writing Kirchhoff 's current equation at node v_2:

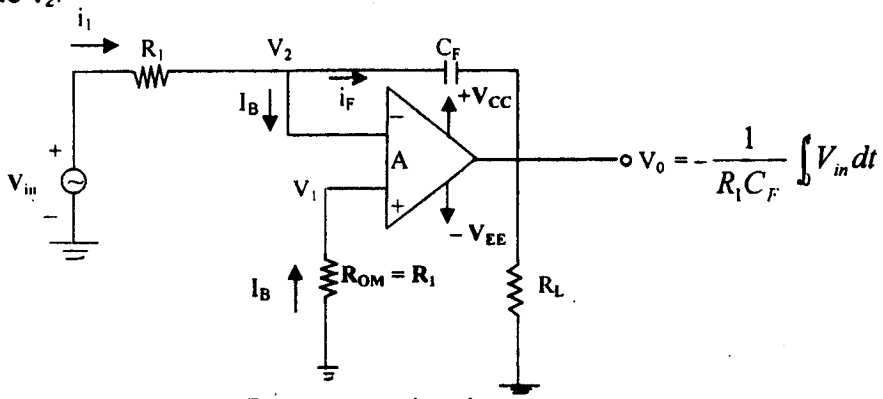


Fig.7.1(a) Integrator circuit.

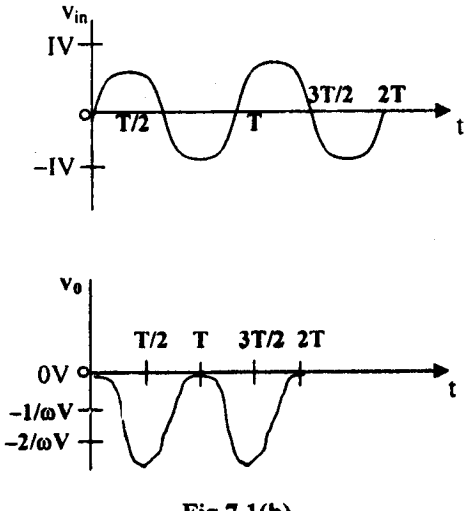


Fig.7.1(b)

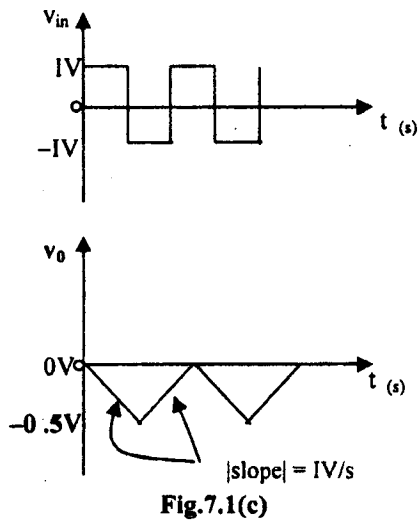


Fig.7.1(c)

$i_1 = I_B + i_F$

Since I_B is negligibly small, $i_1 = i_F$

Recall that the relationship between current through and voltage across the capacitor

$$i_c = C \cdot \frac{dv_c}{dt}$$

Therefore

$$\frac{v_{in} - v_2}{R_1} = C_F \left(\frac{d}{dt}\right)(v_2 - v_0)$$

However, $v_1 = v_2 \cong 0$ because A is very large. Therefore

$$\frac{v_{in}}{R_1} = C_F \frac{d}{dt}(-v_0)$$

The out put voltage can be obtained by integrating both sides w. r. t. time

$$\int_0^t \frac{v_{in}}{R_1} \cdot dt = \int_0^t C_F \frac{d}{dt}(-v_0) \cdot dt = C_F(-v_0) + v_0\big|_{t=0}$$

There fore

$$v_0 = -\frac{1}{R_1 C_F} \int_0^t v_{in}\, dt \qquad \text{--------(7.1)}$$

Eq.(7.1) says that the output voltage is directly proportional to the negative integral of the input and inversely proportional to the time constant R_1C_F. For example if the input is a sine wave, the output will be a cosine wave of if input is a square wave, the output will be a triangular wave as shown as Fig.7.1 (b) and (c) respectively. Note that the wave forms are drawn on the assumption that R_1C_F = 1second and v_{00} = 0V.

For accurate integration of the input waveform, the time period of the input signal T must be longer than or equal to R_1C_F. Again, the R_{oM} is used to minimize the effect or input bias current and the output offset voltage. The input offset voltage v_{i0} and the part of the input current charging the capacitor produce the error voltage at the output of the integrator. Therefore, in the practical integrator shown in Fig.7.1(a), a resistor R_F is connected across the feedback capacitor C_F to produce DC stabilization. In other words, R_F limits the low frequency gain and hence minimizes the variations is the output voltage. Generally, $R_F \cong 10R_1$. The integrator is most commonly used in analog computers and analog to digital converters (ADC) and signal wave shaping circuits.

7.3 THE DIFFERENTIATOR:

Fig.7.2 shows a differentiator or differentiating amplifier. As the name implies, the circuit performs the mathematical operation of differentiation: that is the output waveform is the derivative of the input waveform. The differentiator may be constructed form a basic inverting amplifier of an input resistor R_1 is replaced by a capacitor C_1

The expression for the output voltage can be obtained from Kirchoff's current equation written at node v_2 as follows:

$i_c = I_B + i_F$ since $I_B \cong 0$,

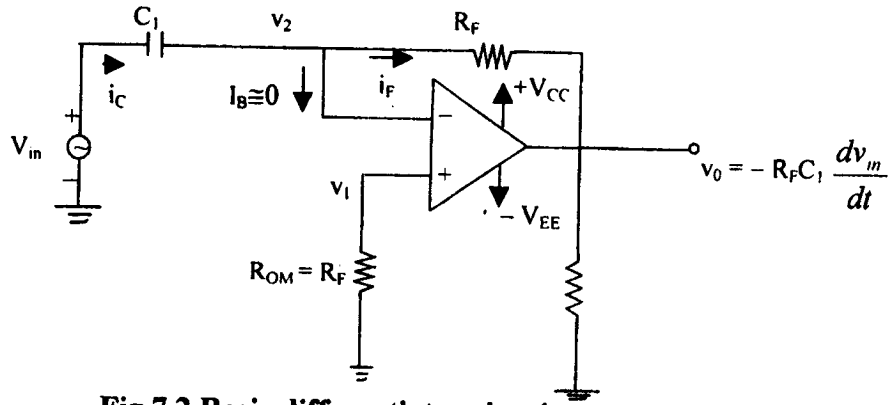


Fig 7.2 Basic differentiator circuit.

$I_c = I_F$

$$C_1 \frac{d(v_{in} - v_2)}{dt} = \frac{v_2 - v_0}{R_F}$$

But $v_1 = v_2 \cong 0v$, because A is very large, therefore

$$C_1 \frac{dv_{in}}{dt} = - \frac{v_0}{R_F}$$

or

$$v_0 = -R_F C_1 \frac{dv_{in}}{dt} \qquad \text{-------- (7.2)}$$

Thus the output v_0 is equal to the $R_F C_1$ times the negative instantaneous rate of change of the input voltage v_{in} with time. Since the differentiator performs the reverse operation of the integrators function a cosine wave input will produce a sine wave output or triangular input will produce a square wave output. However, the differentiator of Fig 7.62 will not do this because it has some practical problems. The gain of the circuit (R_F | X_{C1}) increases with increase in frequency at a rate of 20 dB/decade. This makes the

circuit unstable. Also, the input impedance X_{C1} decreases with increase in the frequency, which makes the circuit very susceptible to high frequency noise. When amplified, the noise can completely over ride the differentiated output signal.

Both the stability and the high frequency noise problems can be corrected by an addition of two components; R_1 and C_F as shown in Fig.7.3 this circuit is a practical differentiator (Fig.7.3a)

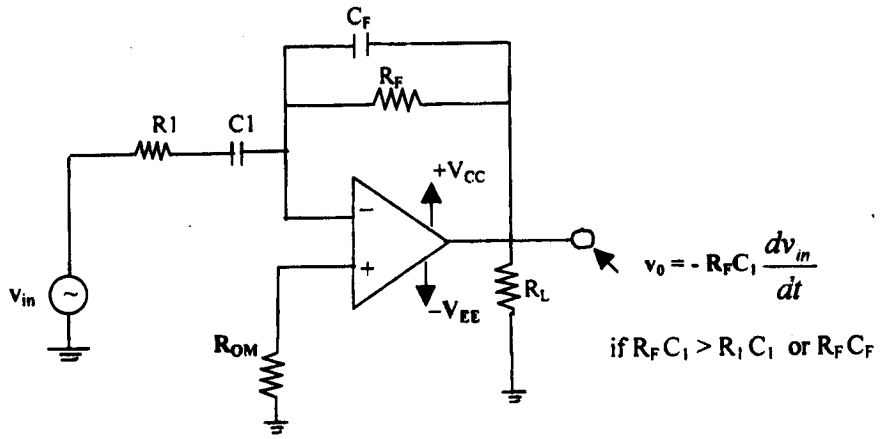


Fig.7.3(a) Practical differentiator

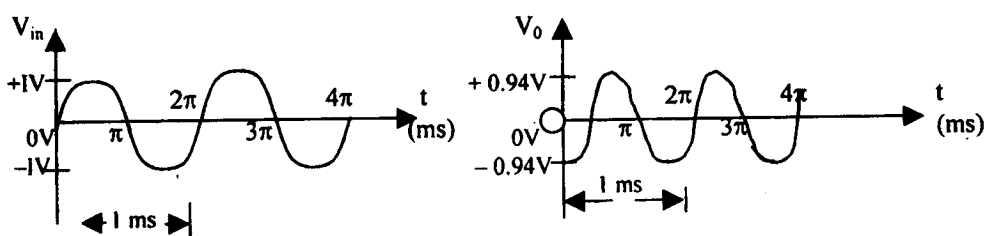


Fig.7.3(b) sine wave input and resulting cosine wave output.

7.4 SOLVING A SECOND ORDER DIFFERENTIAL EQUATION

Consider the differential equation

$$\frac{d^2V}{dt^2} + K_1 \frac{dV}{dt} + K_2 V - V_i = 0 \qquad \ldots\ldots (7.3)$$

where K_1 and K_2 are positive constants. We take the initial conditions as $\frac{dV}{dt} = 0$ and

$V = 0$ at $t = 0$

To solve the differential equation, we assume that $\frac{d^2V}{dt^2}$ is available. By integrating it successively we get $\frac{dV}{dt}$ and V. We rewrite the given differential equation as

$$\frac{d^2V}{dt^2} = -K_1\frac{dV}{dt} - K_2V + V_1$$

If we connect as shown in the diagram at the output of Op.Amp 4 we get

$$-\frac{R_3}{R_2}\frac{dV}{dt} - \frac{R_2}{R_1}V + V_1$$

If we take $\frac{R_2}{R_1} = K_2$ and $\frac{R_3}{R_2} = K_1$ we get at point P_2

$-K_1\frac{dV}{dt} - K_2V + V_1$, which we know is equal to $\frac{d^2V}{dt^2}$, with which we started. Thus point P_1 and P_2 may be connected together. The solution V is obtained at the output of amplifier 2.

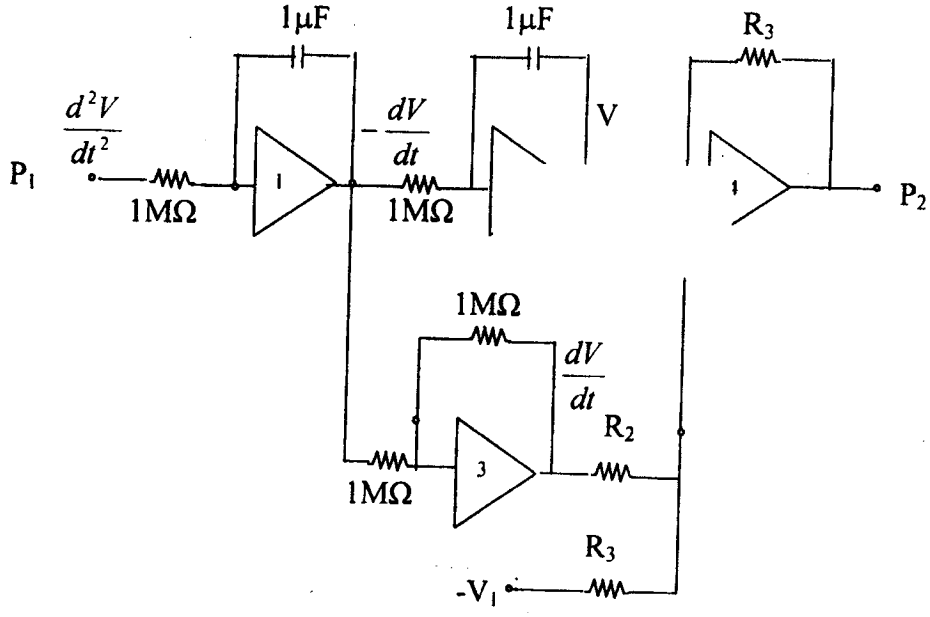


Fig.7.4 Circuit for solving second order differential equation given in Eq.(7.31)

7.5 Logarithmic amplifier

A logarithmic amplifier is that in which output voltage is proportional to the logarithm of the input voltage. The circuit of logarithmic amplifier using a diode is shown in Fig7.8a.

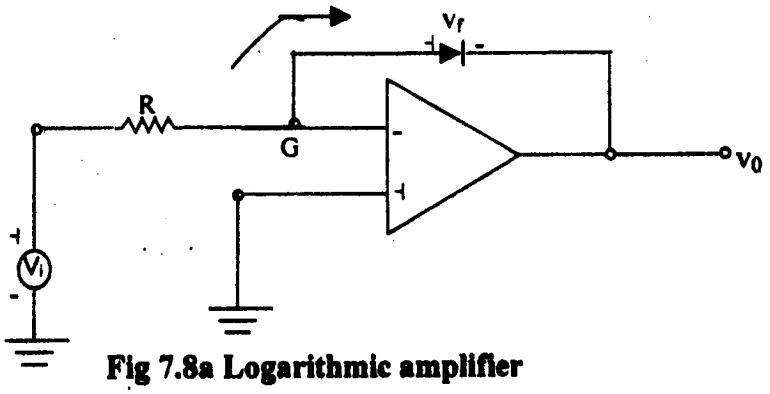


Fig 7.8a Logarithmic amplifier

The volt-ampere characteristics of the diode is given by

$$i = I_S\left[\exp\left(\frac{ev_f}{\eta kT}\right)-1\right]$$

Where I is the diode current for forward voltage v_f

If $$\frac{ev_f}{\eta kT} >> 1$$

Or $i = I_S$, then we have $i = I_S \exp\left(\frac{ev_f}{\eta kT}\right)$

Or $$\log\left(\frac{i}{I_S}\right) = \frac{ev_f}{\eta kT} \quad or \quad v_f = \frac{\eta kT}{e}\log_e\left(\frac{i}{I_S}\right)$$

G is a virtual ground at the amplifier input. Therefore $i = \frac{v_i}{R}$ and then the output voltage is

$$v_0 = -v_f = -\frac{\eta kT}{e}\log_e\left(\frac{v_i}{I_S R}\right)$$

Thus, output voltage v_0 responds to the logarithm of input voltage v_i.

OP-AMP AS A LOGARTHMIC AMPLIFIER USING TRANSISTOR

Fig.7.8b shows the circuit diagram of the fundamental logarithmic amplifier using transistor.

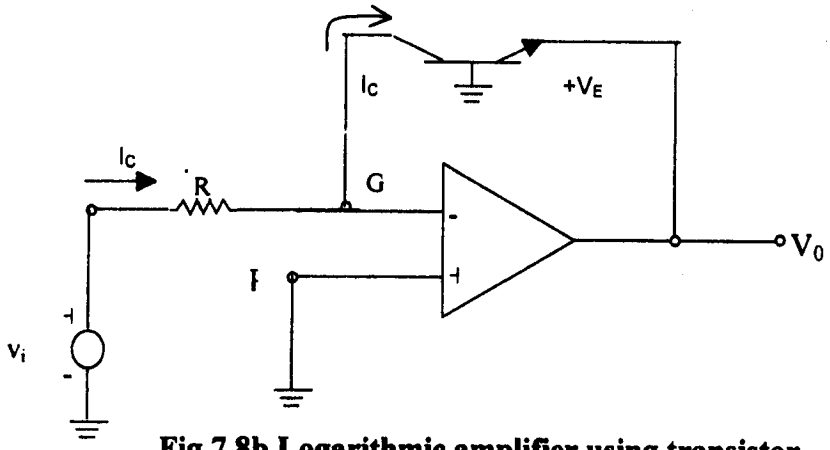


Fig.7.8b Logarithmic amplifier using transistor

In it, a grounded base transistor is placed in the feedback path. Since the collector is held at virtual ground and base is also grounded, the transistor's voltage current relationship becomes that of a diode and is given by,

$$I_E = I_S\left(e^{qV_E/kT} - 1\right) \qquad \ldots\ldots \quad (7.32)$$

Since, $I_C = I_E$ for a grounded base transistor,

$$I_C = I_S\left(e^{qV_E/kT} - 1\right) \qquad \ldots\ldots \quad (7.33)$$

Where I_S = *Emitter saturation current*

k = *Boltzmann's cons*tant

T = *Absolute Temperatire*

Therefore, $\dfrac{I_C}{I_S} = \left(e^{qV_E/kT} - 1\right)$ ..... (7.34)

Or $e^{qV_E/kT} = \dfrac{I_C}{I_S} + 1$

$$= \frac{I_C}{I_S}.$$

Taking natural log on both sides, we get

$$V_E = \frac{kT}{q}\log_e\left(\frac{I_C}{I_S}\right) \qquad \ldots\ldots \quad (7.35)$$

From the circuit diagram, we have

Collector current $I_C = \frac{V_i - V_B}{R} = \frac{V_i}{R}$, since $V_B = 0$

Substituting the value of I_C in Eq.(7.34), we get

$$V_E = \frac{kT}{q}\log_e\left(\frac{V_i}{RT_S}\right)$$

We know that $V_E = -V_0$ (from the circuit)

Let $RI_S = V_{ref}$, a reference voltage,

$$\therefore \text{Output voltage, } V_0 = \frac{kT}{q}\log_e\frac{V_i}{V_{ref}} \qquad (7.36)$$

In the above expression, for V_0, k, T *and* q are fixed, and $V_{ref}(= RI_S)$ are constants

$$\therefore \qquad V_0 \alpha \log_e(V_i) \qquad (7.37)$$

Thus, the output voltage is proportional to the logarithm of the input voltage. It is why the circuit is called logarithmic amplifier. In order that to make Eq.(7.35) holds good, it is essential that V_{ref} is constant. The emitter saturation current I_S varies from transistor to transistor and with temperature. Thus, a stable reference voltage V_{ref} can not be obtained. In order to remove the difficulty, the basic circuit it modified as shown in Fig.7.8c

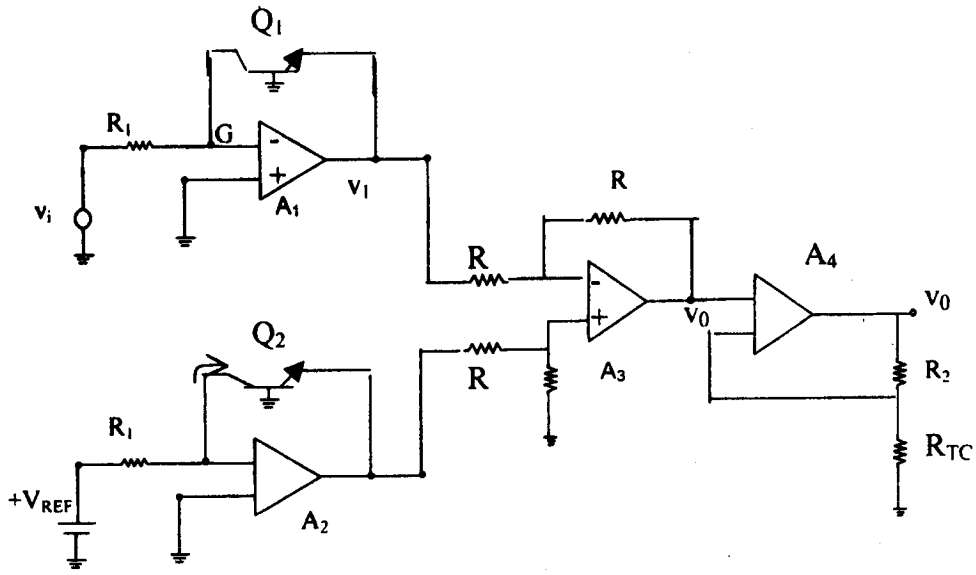


Fig.7.8c Logarithmic amplifier using transistor and a stable reference voltage source

The input signal is applied to A_1 log-amp while a reference voltage V_{ref} is applied to another A_2 log-amp.

The two OP-AMP A_1 and A_2 are integrated in close proximity on the same silicon wafer, so that their reverse saturation currents match at all temperature i.e.,

$$I_{S_1} = I_{S_2}$$

Let $$I_{S_1} = I_{S_2} = I_S$$

For OP-AMP A_1, output voltage $V_1 = \frac{kT}{q}\log_e\left(\frac{V_i}{R_1 I_S}\right)$

And For OP-AMP A_1, output voltage $V_2 = \frac{kT}{q}\log_e\left(\frac{V_{ref}}{R_1 I_S}\right)$

The two outputs form inputs top OP-AMP A_3 whose output is

$$V_0 = V_2 - V_1$$

$$V_0 = \frac{kT}{q}\left[\log_e\left(\frac{V_i}{R_1 I_S}\right) - \log_e\left(\frac{V_{ref}}{R_1 I_S}\right)\right]$$

Or $$V_0 = \frac{kT}{q}\log_e\left(\frac{V_i}{V_{ref}}\right)$$ (on simplification)

Thus reference level is set with a single external voltage source. Its dependence on device and temperature is removed.

The voltage V_0 is still dependent upon temperature and is directly proportional to temperature is compensated by the last OP-AMP stage A_4 which provides a non-inverting gain of $\left(1 + \frac{R_2}{R_{T_c}}\right)$ where R_{T_c} is a temperature sensitive resistance with a positive temperature coefficient (sensitor).

∴ Output of OP-AMP, A_4, voltage compensated,

$$V_{0(comp)} = \left(1 + \frac{R_2}{R_{T_c}}\right)\frac{kT}{q}\log_e\left(\frac{V_i}{V_{ref}}\right)$$

Since R_{T_c} is a sensistor, it helps to contain the slope of the equation of V_0 (comp) constant at all temperature changes.

$$V_{0(comp)} \alpha \log_e \left(\frac{V_i}{V_{ref}} \right)$$

Or $$V_{0(comp)} \alpha \log_e V_i. \qquad (since\ V_{ref}\ is\ fixed)$$

The same output with an inversion is obtained by the modified circuit using two Op-Amps. is shown in Fig.7.8(d)

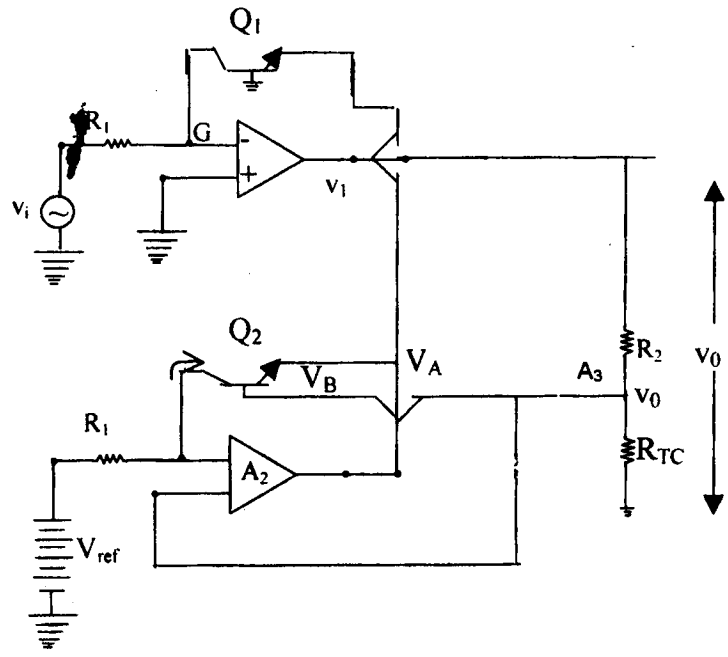


Fig.7.8d Logarithmic amplifier with two Op Amps

Hence, compensated output voltage, $V_{0(comp)} = -\left(1 + \frac{R_2}{R_{T_C}}\right)\frac{kT}{q}\log_e\left(\frac{V_i}{V_{ref}}\right)$

7.6 OP-AMP AS AN ANTILOG AMPLIFIER

The circuit of an Antilog Amplifier is shown in Fig.7.9

The input of V_i for the antilog-amp is fed into the temperature compensating voltage divider R_L and R_{TC} and then the base of transistor Q_2. The output V_0 of the antilog-amp is fed back to the inverting input of A_1through the resistor R_1. the base of emitter voltage of transistors Q_1 and Q_2 are

$$V_{Q_1 B-E} = \frac{kT}{q}\ln\left(\frac{V_0}{R_1 I_S}\right) \qquad \ldots\ldots\ldots\ldots\ldots\ldots (7.37)$$

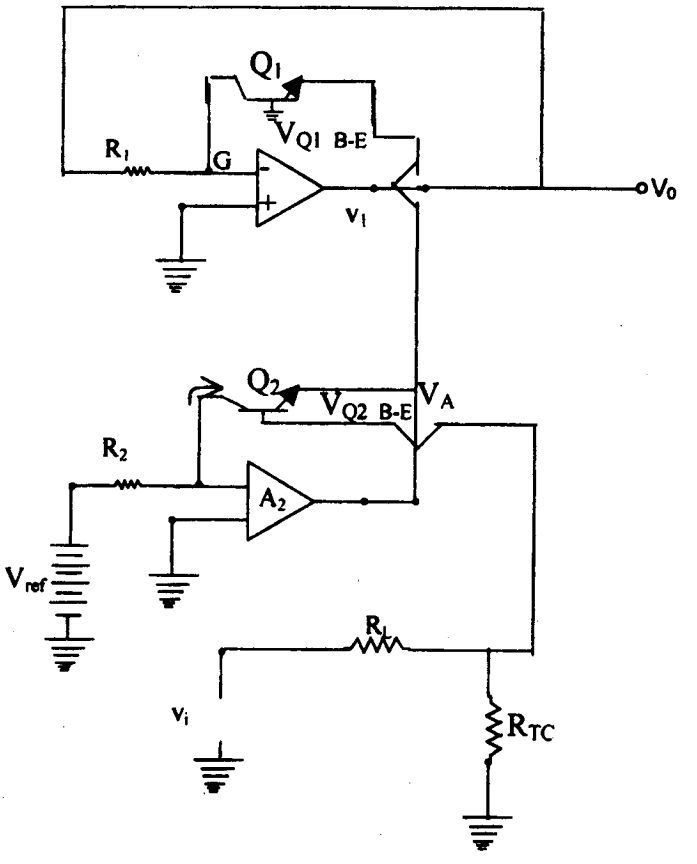


Fig.7.9 Anti-Log Amplifier

$$V_{Q_2B-E} = \frac{kT}{q}\ln\left(\frac{V_0}{R_1 I_S}\right) \qquad \text{..... (7.38)}$$

Since the base of transistors Q_1 is tied to ground, we get

$$V_A = V_{Q_1B-E} = -\frac{kT}{q}\ln\left(\frac{V_0}{R_1 I_S}\right) \qquad \text{..... (7.39)}$$

The base voltage V_B of transistor Q_2 is

$$V_B = \left(\frac{R_{T_C}}{R_2 + R_{T_C}}\right)V_0 \qquad \text{.....(7.40)}$$

The voltage at the emitter of Q_2 is

$$V_{Q_2E} = V_B + V_{Q_2E-B}$$

$$V_{Q_2E} = \left(\frac{R_{T_C}}{R_2 + R_{T_C}}\right)V_i - \frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

But the emitter voltage of Q_2 is V_A, that is,

$$V_A = V_{Q_2E}$$

$$\therefore \quad -\frac{kT}{q}\ln\frac{V_0}{R_1 I_S} = \left(\frac{R_{T_C}}{R_2 + R_{T_C}}\right)V_i - \frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

or
$$\left(\frac{R_{T_C}}{R_2 + R_{T_C}}\right)V_i = -\frac{kT}{q}\left(\ln\frac{V_0}{R_1 I_S} - \ln\frac{V_{ref}}{R_1 I_S}\right)$$

or
$$-\frac{q}{kT} + \left(\frac{R_{T_C}}{R_2 + R_{T_C}}\right)V_i = \ln\left(\frac{V_0}{V_{ref}}\right) \quad \ldots\ldots \quad (7.41)$$

Changing natural log i.e., ln to $\log_{10}$ using Eq. (7.41), we get

$$-0.4343\left(\frac{q}{kT}\right) + \left(\frac{R_{T_C}}{R_2 + R_{T_C}}\right)V_i = 0.4343 \times \log_{10}\left(\frac{V_0}{V_{ref}}\right)$$

$$-k'V_i = \log_{10}\left(\frac{V_0}{V_{ref}}\right) \qquad or \qquad \frac{V_0}{V_{ref}} = 10^{-k'V_i}$$

Since V_{ref} is of constant magnitude, therefore,

$$V_0 = V_{ref}\left(10^{-k'V_i}\right)$$

where
$$k' = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{T_C}}{R_2 + R_{T_C}}\right)$$

Hence an increase of input by one volt causes the output to decrease by a decade or 10 volts. Thus the circuit functions as antilog amplifier.

7.7 OP- AMP AS A LOGARTHMIC MULTIPLIER:

The log and antilog amplifiers can be used for the multiplication of two analog signals. The basic principle involved in the design of the analog multiplier is that the sum of the logarithms of the numbers is equal to the logarithm of the product of the two numbers, i.e.,

$$\log_e x + \log_e y = \log_e(xy)$$

$$\log_e v_x + \log_e v_y = \log_e\left(v_x v_y\right)$$

Thus in a logarithmic multiplier, the logarithm of each input V_{S1} and V_{S2} is taken, then two logarithms are added and finally the antilog of the sum gives the product of the two inputs. The basic circuit diagram of logarithmic multiplier of the two analog signals is shown in Fig.7.10

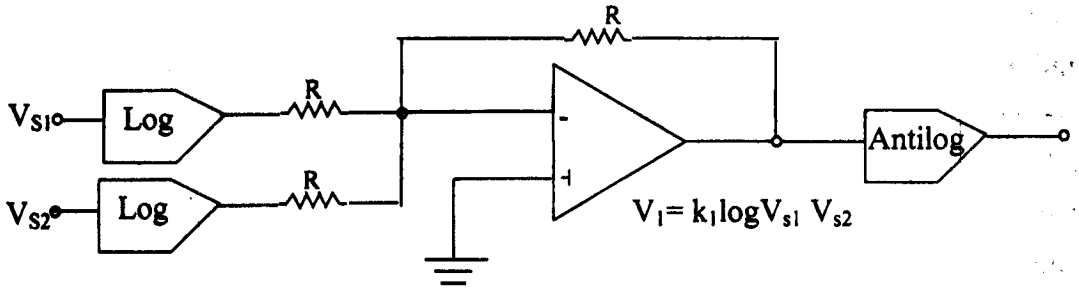


Fig 7.10 Logarithmic Multiplier

Thus

$$V_1 = k_1 \log_e V_{S_1} + k_1 \log_e V_{S_2} = k_1 \log_e V_{S_1} V_{S_2}$$

and $$V_0 = Anti\log\left[k_1 \log_e V_{S_1} V_{S_2}\right]$$

$$= k_2 \log_e^{-1} k_3 V_1 = k_2 \log_e^{-1}\left(k_3 k_1 \log_e V_{S_1} V_{S_2}\right)$$

If $k_3 k_1 = 1$, then we may put

$$V_0 = k_2 V_{S_1} V_{S_2}$$

7.8 SUMMARY

Summing, scaling amplifiers can be constructed by using inverting, non-inverting and differential configurations. The integrator and differentiator are most widely used in signal wave shaping applications. Besides, the integrator is used in analog computers and the differentiator is used as a rate of change detector in FM modulators. Logarithmic amplifiers are used to find sum of logarithmic values of two numbers (represented by some scaled voltages). Since log (a) + log (b) = log (ab), we get log of (ab). By giving this result to an antilog amplifier, we get the product of two numbers. Likewise, since log (a) - log (b) = log (a/b), we can perform arithmetic division of two numbers. With these fundamental building blocks analog computers were developed to perform complex scientific calculations. Comparators are used in open loop configuration. These form the basic circuits to construct analog to digital converters.

7.9 KEY TERMINOLOGY

Exponential: It is raising the number value by some power usually by Naperian base 'e'.

$Y = e^x$. Here x is called power or exponential.

Logarithm to the base e is an inverse operation of exponential operation.

Log (y) = x

Neperian base can be changed to the base 10 form and it is these logarithmic value we frequently find in mathematical tables.

Logarithmic value of numbers: By using the logarithmic method we can represent very large and very small numbers in a convenient way. As per logarithmic rules Logarithm of product of two numbers can be represented as sum of two numbers in logarithmic form. Difference of two numbers in logarithmic form is identical to log divided value of two numbers. Anti-logarithms are also defined to convert log value of numbers into normal numbers

7.10 SELF-ASSESSMENT QUESTIONS

Long answer questions

1. Explain the difference between the integrator and differentiator and give one application of each.
2. Describe an analog computation circuit using Op Amp to solve simple second order differential equation. Explain its working with a suitable example.
3. Draw the circuit diagrams to explain the use of Op Amp as an integrator and a differentiator.
4. Set up a circuit for an analog computer to solve

$$\frac{d^2y}{dx^2} + 2\frac{dy}{dx} + 5x = 2$$

For x as a function of time. Initial conditions are x(0) = 0,

$$\frac{dx}{dt}(0) = 0 \; at \quad t = 0$$

SHORT ANSWER QUESTIONS

1. In what way is the voltage follower is a special case of the non-inverting amplifier?
2. Explain comparator action of an Op Amp.
3. Explain how an Op Amp is used as an integrator?
4. Draw the Op Amp voltage regulator circuit and explain its operation.

7.11 Text and Reference Books

(1) Operational Amplifiers and Linear Integrated Circuit Technology by Ramakanth A. Gayakwad, Prentice Hall Inc.,

(2) Basic Electronics by D.C. Tayal, Himalaya Publish Co.,

(3) Semiconductor Electronics by A K. Sharma
New Age International Publishers

(4) Foundations of Electronics
By D. Chattopadhyay, PC Rakshit, B. Saha, M.N. Purohit
Second Edition, Wiley Eastern Ltd.,

OPERATIONAL AMPLIFIERS - IV

OBJECTIVES OF THE LESSON

To explain (i) the oscillator principle and discuss the various types of oscillators , (ii) the construction of square wave and triangular wave generators and (iii) the operation of the 555 Timer as an astable multi-vibrator.

STRUCTURE OF THE LESSON

8.1 INTRODUCTION

In the earlier lessons, we have seen how negative feedback provided virtual ground at the inverting input and resulted in developing various circuits whose performance is dependent on the circuit components only. In this lesson, we consider the effect of positive feedback on Op Amp performance. Various types of oscillators were developed using both Negative and positive feedback and suitable circuit elements to produce sine wave, square wave and other types of waveforms. We learn about these aspects in this lesson. Many of the circuits are useful in conducting prescribed experiments.

Basically the function of an oscillator is to generate alternating current or voltage waveforms. More precisely, an oscillator is a circuit that generates a repetitive waveform of fixed amplitude and frequency without any external input signal. Oscillators are used in radio, television, computers, and communications. Although there are different types of oscillators, all of them work on the same basic principle.

Oscillators are classified into two basic categories: sinusoidal and non-sinusoidal. If the waveform generated is a sinusoidal wave, the circuit is called a **Sinusoidal oscillator** and these circuits producing all other waveforms are called **non-sinusoidal oscillators**. Some times, the oscillators are also classified on the basis

of frequency of the generated waveform, viz., audio frequency, radio frequency and ultra high frequency oscillators.

8.2 Oscillator principle:

An Oscillator, as such, is a type of feedback amplifier in which part of the output is feed back to the input via a feedback circuit. If the signal feedback is of proper magnitude and phase, the circuit produces alternating currents or voltages. To visualize the requirement of an oscillator, consider the block diagram of Fig.8.1. However, here the input voltage is zero (v_{in} = 0). Besides that, the feedback is positive because most oscillators use positive feedback. Finally, the closed loop gain of the amplifier is denoted by A_v rather that A_F.

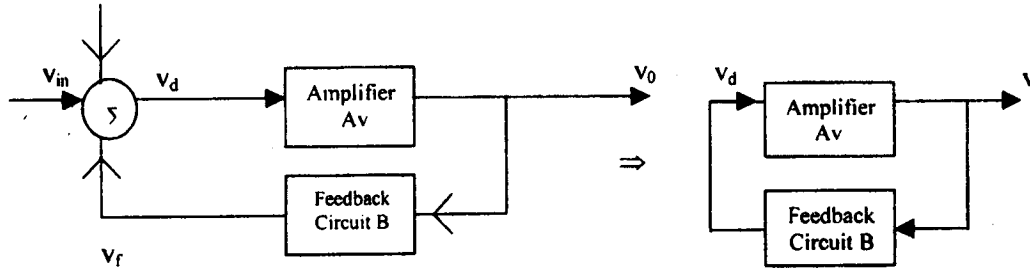


Fig.8.1 Oscillator block diagram

In Fig.8.1,

$$v_d = v_f + v_{in} \quad \text{-------- (8.1)}$$

$$v_0 = A_v v_d \quad \text{------- (8.2)}$$

$$v_f = B v_0 \quad \text{------- (8.3)}$$

Using these relation ships, the following equations are obtained

$$\frac{v_0}{v_{in}} = \frac{A_v v_d}{v_d - v_f} = \frac{A_v}{1 - (vf / vd)} \quad \text{--------- (8.4)}$$

From Eqs (8.2) and (8.3), we have

$$\frac{v_f}{v_d} = A_v B \quad \text{--------- (8.5)}$$

Substitute Eq.(8.5) in Eq.(8.4), we have

$$\frac{v_0}{v_{in}} = \frac{A_v}{1 - A_v B} \quad \text{--------- (8.6)}$$

However, v_{in} = 0, and $v_0 \neq 0$ implies that

$A_V B = 1$

Expressed in polar form

$A_v B = 1$ and $\phi = 0$ or 360^0 -------- (8.7)

Eq.(8.7) gives the two requirements for oscillators:

(1) The magnitude of the loop gain $A_v B$ must be at least 1, and

(2) The total phase of the loop gain $A_v B$ must be equal to 0^0 or 360^0. For instance, as indicated in Fig (8.1), if the amplifier causes a phase shift of 180^0

The feedback circuit must provide an additional phase shift of 180^0, so that, the total phase shift around the loop is 360^0. The waveforms shown in Fig 8.1 are sinusoidal and are used to illustrate the circuit's action. The type of waveform generated by an oscillator depends on the components in the circuit and hence, may be sinusoidal, square or triangular. In addition, the frequency of the oscillation is determined by the components in the feedback circuit.

Sine wave generators	**Other waveform generators**
1. RC Oscillator	1. Square wave oscillator
2. LC Oscillator	2. Triangular wave oscillator
8. Crystal Oscillator	3. Saw-tooth wave oscillator

8.3 PHASE SHIFT OSCILLATOR

Fig.8.2 shows a phase shift oscillator, which consists of an op-amp, as amplifying stage and three RC cascaded networks in the feedback circuit. The feedback circuit provides feedback voltage from the output back to the input of the amplifier. The op-amp is used in the inverting mode; therefore any signal that appears at the inverting terminal is shifted by 180^0 at the output. An additional 180^0 phase shift required for oscillation is provided by the cascaded RC networks. Thus the total phase shift around the loop is 360^0 (or 0^0). At some specific frequency, when the phase shift of the cascaded RC networks is exactly 180^0 and the gain of the amplifier is sufficiently large, the circuit will oscillate at that frequency. This frequency is called the frequency of oscillation f_0 and is given by

$$f_0 = \frac{1}{2\pi\sqrt{6}RC} = \frac{0.065}{RC} \qquad \text{--------- (8.8)}$$

At this frequency, the gain A_v must be at least 29. That is

$$\frac{R_F}{R_1} = 29$$

$$R_F = 29\, R_1 \qquad \text{--------- (8.9)}$$

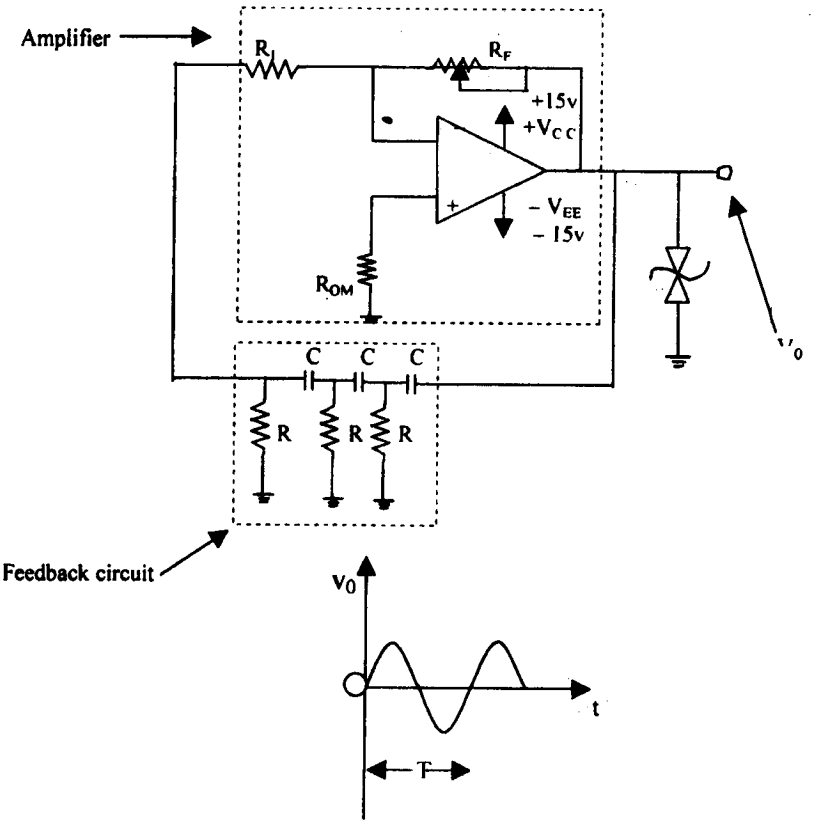


Fig.8.2 Phase shift oscillator and its output waveform

Then the circuit will produce a sinusoidal waveform of frequency f_0 if the gain is 29 and the total phase shift around the circuit is exactly 360^0. For a desired frequency of oscillator, choose a capacitor C_1 and then calculate the value of R from equation (8.8). A desired output amplitude, however, can be obtained with back-to-back Zeners connected at the output terminal shown in Fig.8.2

ANALYSIS

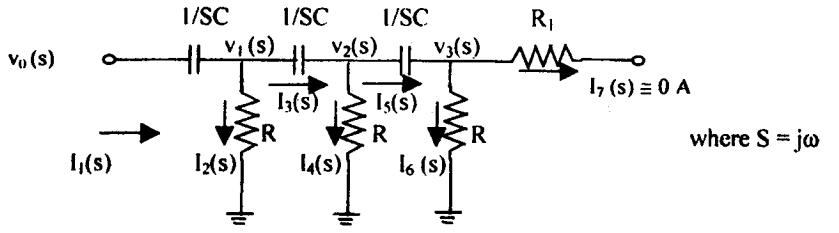


Fig.8.3 RC network of the phase shift oscillator

Nodal equations are transformed into the s domain

Writing Kirchoff's current law (KCL) at node $v_1(s)$, we get $I_1(s) = I_2(s) + I_3(s)$

$$\frac{V_0(s) - V_1(s)}{1/sC} = \frac{V_1(s)}{R} + \frac{V_1(s) - V_2(s)}{1/sC}$$

$$v_1(s)\left[\frac{1}{R} + 2sC\right] + v_2(s)(-sC) = v_0(s)(sC) \qquad \text{-------- (8.10)}$$

Writing KCL at node $v_2(s)$

$I_3(s) = I_4(s) + I_5(s)$

$$\frac{V_1(s) - V_2(s)}{1/sC} = \frac{V_2(s)}{R} + \frac{V_2(s) - V_3(s)}{1/sC}$$

$$v_1(s)[-sC] + v_2(s)\left[\frac{1}{R} + 2sC\right] + v_3(s)[-sC] = 0 \qquad \text{-------- (8.11)}$$

Writing KCL at node $v_3(s)$

$I_5(s) = I_6(s)$

$$\frac{V_2(s) - V_3(s)}{1/sC} = \frac{V_3(s)}{R}$$

$$v_2(s)[SC] + v_3(s)\left[-\frac{1}{R} - sC\right] = 0 \qquad \text{---------- (8.12)}$$

$$v_2(s) = v_3(s)\left[\frac{1}{RsC} + 1\right]$$

Substituting this in Eq.(8.11)

$$v_1(s)[-sC] + v_3(s)\left[1 + \frac{1}{sRC}\right]\left[\frac{1}{RsC} + 2\right] + v_3(s).(-sC) = 0$$

$$v_1(s) = v_3(s)\left[-1 + \left(1 + \frac{1}{RsC}\right)\left(2 + \frac{1}{RsC}\right)\right]$$

Substituting this in Eq.(8.10)

$$v_3(s)\left[-1+\left(1+\frac{1}{RsC}\right)\left(2+\frac{1}{RsC}\right)\right]\left[\frac{1}{R}+2sC\right]+v_3(s)\left[\frac{1}{RsC}+1\right](-SC)=v_0(s)(sC)$$

$$v_3(s)\left\{-1+\left(1+\frac{1}{RsC}\right)\left(2+\frac{1}{RsC}\right)\left(\frac{1}{R}+2sC\right)\right\}+v_3(s)\left((-sC)-\frac{1}{R}\right)=v_0(s)(sC)$$

$$v_3(s)\left[-\frac{1}{R}-2sC+\left[\frac{1}{RsC}+1\right]\left[2+\frac{1}{RsC}\right]\left[\frac{1}{R}+2sC\right]-sC-\frac{1}{R}\right]=v_0(s)(sC)$$

$$v_3(s)\left[(-3sC-\frac{2}{R})+\left(\frac{RsC+1}{RsC}\right)\left(\frac{2RsC+1}{RsC}\right)\left(\frac{1+2RsC}{R}\right)\right]=v_0(s)(sC)$$

$$v_3(s)\left[\frac{\left(-3R^3s^3C^3-2R^2s^2C^2\right)+(1+RsC)(1+4R^2s^2C^2+4RsC)}{R^3s^2C^2}\right]=v_0(s)(sC)$$

$$v_3(s)\,[R^3s^3C^3+6R^2s^2C^2+5RsC+1]=v_0(s)\,[R^3s^3C^3]$$

$$\frac{v_3(s)}{v_0(s)}=\frac{s^3R^3C^3}{s^3R^3C^3+6s^2R^2C^2+5sRC+1} \qquad \text{-------- (8.12 (a))}$$

Next consider the op-amp part of the phase shift oscillator, the voltage gain of the op-amp

$$A_v=\frac{v_0(s)}{v_3(s)}=-\frac{R_F}{R_1} \qquad \text{-------- (8.12 (b))}$$

For an oscillator

$$A_v B=+1. \qquad \text{-------- (8.13)}$$

Therefore, using Eqs.8.12(a) and 8.12(b), we have

Since it is an inverting amplifier $A_v=-\frac{R_F}{R_1}$

$$\left(-\frac{R_F}{R_1}\right)\left[\frac{S^3R^3C^3}{S^3R^3C^3+6R^2S^2C^2+5SRC+1}\right]=1$$

Substituting S = jω, and equating the real and imaginary parts, respectively, we get

$$\left(-\frac{R_F}{R_1}\right)\left[\frac{-j\omega^3R^3C^3}{-j\omega^3R^3C^3-6\omega^2R^2C^2+j5\omega RC+1}\right]=1$$

$$\left(-\frac{R_F}{R_1}\right)(-\ j\omega^3R^3C^3) = -\ j\omega^3R^3C^3 - 6\ \omega^2R^2C^2 + j5\omega RC + 1 \quad \text{------(8.14)}$$

$-6\omega^2R^2C^2 + 1 = 0$ (Real)

$$\omega^2=\frac{1}{6R^2C^2} \quad \text{--------- (8.14(a))}$$

$$f=\frac{1}{2\pi\sqrt{6}RC} \quad \text{---------- (8.15)}$$

$$\left(-\frac{R_F}{R_1}\right)(-\omega^3R^3C^3) = -\omega^3R^3C^3 + 5\omega RC \text{ (imaginary)}$$

$$\frac{R_F}{R_1} = -\ +\frac{5}{\omega^2R^2C^2} \quad \text{---------- (8.15 (a))}$$

From equation 8.14(a) and 8.15(a) we have

$$\frac{R_F}{R_1}=29 \quad \text{---------- (8.16)}$$

8.4 WIEN BRIDGE OSCILLATOR

The circuit diagram for typical Wien bridge oscillator is shown in Fig.8.4. This involves an RC bridge circuit in which a frequency adjusting network is constructed of series combination of R_1 and C_1 connected from the output of the op-amp to the non-inverting input of the op-amp and of a parallel combination of R_2 and C_2 from the non-inverting input of the op-amp to the ground connections. The resistances R_3 and R_4 form the non-inverting input of the op-amp to the ground connections. The resistors R_3 and R_4 make the feedback path and determine the gain of the amplifier. The bridge circuit causes a phase shift of 360^0 between the output and input of the op-amp.

In the circuit of Fig8.4, the voltage v_i across the parallel combination of R and C is fed back and is expressed as

$$v_i = \frac{v_0 Z_1}{Z_1 + Z_2} \qquad \text{---------- (8.17)}$$

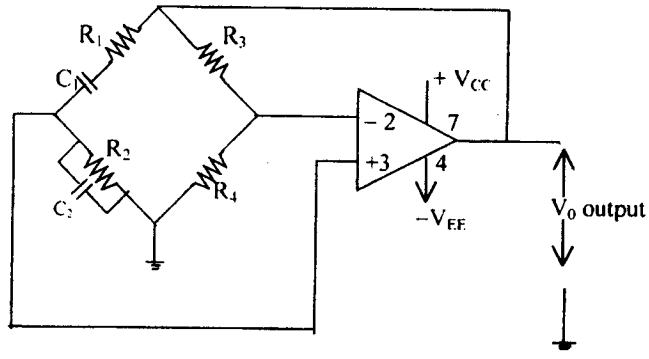


Fig.8.4(a) Circuit configuration for Wien bridge oscillator

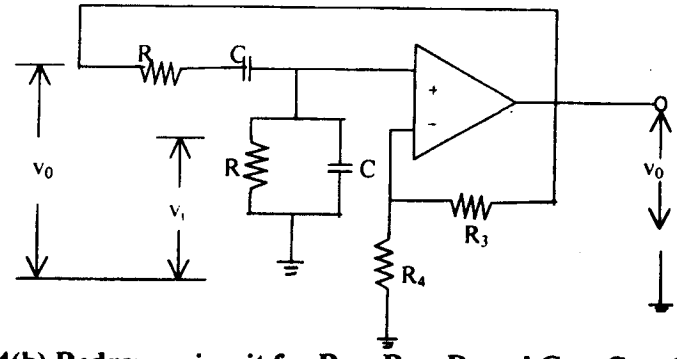


Fig.8.4(b) Redrawn circuit for $R_1 = R_2 = R$, and $C_1 = C_2 = C$

Where $Z_1 = R||C = \dfrac{R\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}}$ and

$$Z_2 \text{ (R in series with C)} = R + \frac{1}{j\omega C} \qquad \text{---------- (8.18)}$$

$$v_i = \frac{v_0\left(\dfrac{R\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}}\right)}{\left(\dfrac{R\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}}\right) + \left(R + \frac{1}{j\omega C}\right)} \qquad \text{---------- (8.19)}$$

$$v_i = v_0 \frac{R - \frac{1}{j\omega C}}{R\frac{1}{jC} + R^2 + 2R.\frac{1}{j\omega C} - \frac{1}{\omega^2 C^2}}$$

$$= v_0 \frac{1}{1 + j\omega RC + 2 - \frac{j}{\omega RC}} = v_0 \frac{1}{3 + j\left(\omega RC - \frac{1}{\omega RC}\right)} \quad \text{--------- (8.20)}$$

In order to have zero phase between v_i and v_0, the j-terms must be zero i.e.,

$$\omega RC - \frac{1}{\omega RC} = 0;$$

$$\omega^2 = \frac{1}{R^2C^2}$$

$$\omega = \frac{1}{RC};\ f = \frac{1}{2\pi RC} \quad \text{-------- (8.21)}$$

Substituting this frequency in equation (8.20)

$$v_i = \frac{1}{3} v_0 \quad \text{--------- (8.22)}$$

Eq.8.22 shows that there is a loss of voltage gain in the feedback network by a factor of 8. Therefore, the amplifier should have minimum voltage gain as 3 for oscillations.

The input voltage v_1 at the inverting point of the op-amp may be written as

$$v_i = \frac{v_0 R_4}{R_3 + R_4} \quad \text{--------- (8.23)}$$

Equating Eq.(8.22) and (8.23), we get

$$\frac{1}{3} = \frac{R_4}{R_3 + R_4}$$

$$R_3 = 2R_4 \quad \text{--------- (8.24)}$$

the flip-flop, with output going low. The discharge transistor also goes low, causing the capacitor to remain at near 0V until triggered again. Fig8.9d shows the input trigger signal and the resulting output waveform for the 555 timer operated as monostable multivibrator or one-shot. Time periods for this circuit can range from microseconds to many seconds, making the IC useful for a range of applications.

8.7 SUMMARY

Basically, the function of an oscillator is to generate alternating current or voltage waveforms. The oscillators are classified with two basic categories: sinusoidal and non-sinusoidal. If the waveform generated looks like a sine or cosine wave, the circuit is called a Sinusoidal oscillator and the circuits producing all other waveforms are called Non-sinusoidal oscillators.

There are two requirements for oscillations:

1. The magnitude of loop gain $A_V B$ must be greater than or equal to 1.
2. The total phase shift of the loop gain must be 0^0 or 360^0.

The Phase shift and Wien bridge are the most commonly used sinusoidal oscillators for frequencies below 100kHz. In all these oscillators the frequency of oscillation is a function of the RC time constant.

For frequencies above 100kHz, tunable oscillators like Hartley, Colpitt's oscillators and crystal oscillators are preferable.. The theory regarding these oscillators is available in standard text books and is left as an exercise to the students. For information on this topic students may refer to books mentioned under reference.

Square wave outputs are generated when the op-amp is forced to operate in the saturated regions, that is, the output of the op-amp is forced to swing repetitively between positive saturation $+V_{sat}$ ($\cong V_{CC}$) and $-V_{sat}$ ($\cong -V_{EE}$) resulting in the square wave output. One way to obtain the triangular wave is to integrate the square wave. Therefore, the triangular wave generator can be formed by using a comparator and integrator.

Signetics NE / SE 555 is a monolithic timing circuit, that can produce accurate and highly stable time delays or oscillations. Thus the 555 may be used as either a mono-stable or an astable multi-vibrator. This device can be used in such applications as waveform generators, digital logic probes, integrated transmitters, burglar alarms, toxic gas alarms and electronic eyes.

8.8 KEY TERMINOLOGY

1. Crystal oscillator: A crystal oscillator is also a resonance frequency oscillator in which a piezo electric crystal is used as tuned / resonant circuit because

Monostable operation

The IC555 timer is connected for monostable operation as shown in Fig.8.9c As the name indicates, this circuit has one stable state. i.e. it will be either in on-state or off-state unless acted upon by external trigger pulse. Application of a trigger pulse makes the circuit change from its stable state to move into an unstable state for a period determined by the time constant of RC circuit and the fall back to its original stable state. The transition from stable to unstable state and falling from unstable to stable state is very fast and we observe a rectangular pulse at the output, for every trigger pulse given to pin no.2

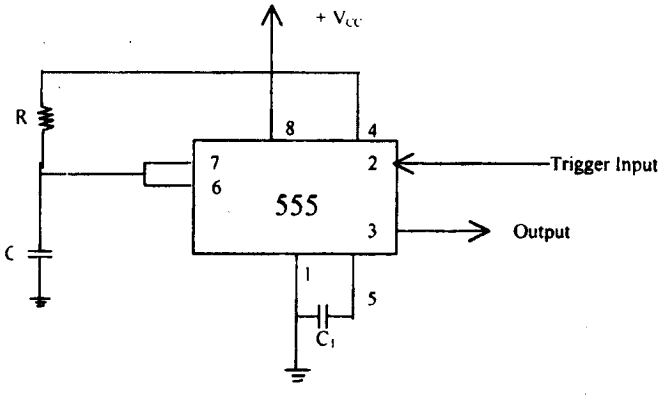


Fig.8.9c Monostable multivibrator

When the trigger input goes negative, it triggers the one shot, with output pin 3 then going high for a period

$$T_{high} = 1.1\ RC$$

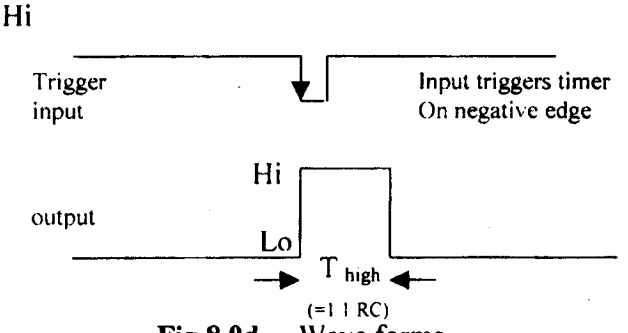


Fig.8.9d Wave forms

Referring back to Fig.8.8b, the negative edge of the trigger input causes comparator 2 to trigger the flip-flop, with the output at pin 3 going high. Capacitor charges toward V_{CC} through R. During the charging interval, the output remains high. When the voltage across capacitor reaches the threshold level of $2V_{CC}/3$, comparator 1 triggers

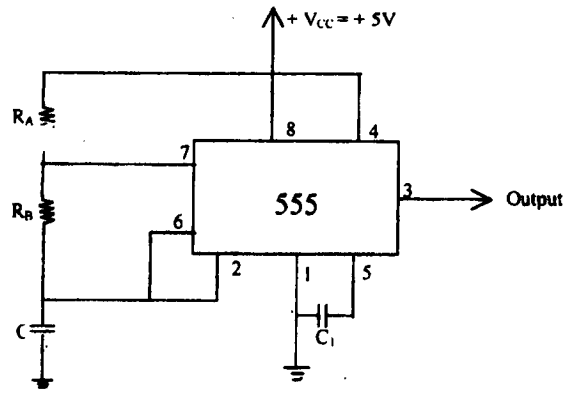


Fig.8.9(a) The 555 astable multi-vibrator circuit

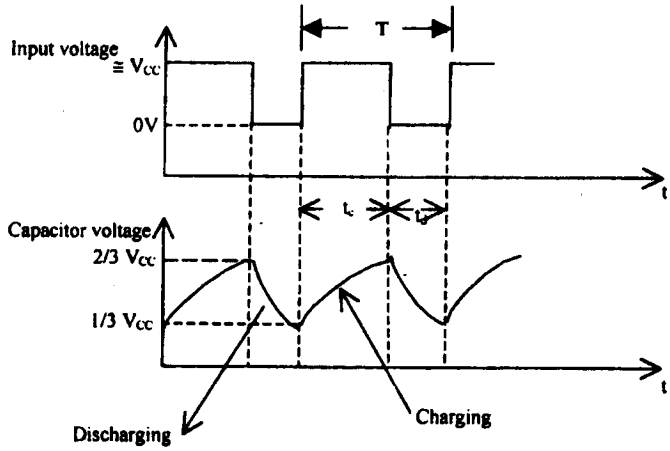


Fig 8.9(b) The 555 astable multi-vibrator output voltage wave form and voltage across the capacitor.

Similarly, the time during which the capacitor discharges from $\frac{2}{3}$ V_{cc} to $\frac{1}{3}$ V_{cc} is equal to the time, the output is low and is given by

$$t_d = 0.69\ R_B C \qquad \text{---------- (8.31)}$$

Thus the total time period of the output waveform is

$$T = t_c + t_d = 0.69\ (R_A + 2R_B)\ C \qquad \text{----------(8.32)}$$

This, in turn gives the frequency of oscillation as

$$f_0 = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \qquad \text{-------- (8.33)}$$

Eq.(8.33) indicates then the frequency f_0 is independent of the supply voltage V_{cc}.

Pin 7: Discharge. This pin is connected internally to the collector of transistor Q_1. When the output is high, Q_1 is off and acts as an open circuit to the external capacitor C connected across it. On the other hand, when the output is low, Q_1 is saturated and acts as a short circuit, shorting out the external capacitor C to ground

Pin 8: $+V_{cc}$. The supply voltage of +5V to +18V is applied to this pin with respect to ground (pin 1)

8.6.2 THE 555 AS AN ASTABLE MULTI-VIBRATOR

An astable multi-vibrator, often called a **Free running multi-vibrator**, is a rectangular wave generating circuit. The time during which output is either high or low is determined by the two resistors and a capacitor, which are externally connected to the timer 555.

ASTABLE OPERATION

Fig.8.9(a) shows the 555 timer connected as an astable multi-vibrator. Initially, when the output is high, capacitor C starts charging toward V_{cc} through R_A and R_B. However as soon as voltage across the capacitor equals $\frac{2}{3}V_{cc}$, comparator 1 triggers the flip-flop, and the output switches low [see fig 8.9(b)]. Now capacitor C starts discharging through R_B and transistor. When the voltage across C equals $\frac{1}{3}V_{cc}$, comparator 2's output triggers the flip-flop and the output goes high. Then the cycle repeats. The output voltage and capacitor voltage waveforms are shown in Fig. 8.9(b).

As shown in this figure, the capacitor C is periodically charged and discharged between $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$ respectively.

The time during which the capacitor charges from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$ is equal to the time the output is high and is given by

$$t_c = 0.69 (R_A + R_B)C \qquad \text{--------} \quad (8.30)$$

where R_A and R_B are is ohms and C is in Farads.

Before proceeding with the operations of 555 Timer as an astable multi-vibrator, it is important to examine its pin functions. The pin number is used in the following discussion refer to the 8 pin mini DIP and 8-pin metal can packages

Pin 1: Ground. All voltages are measured with respect to this terminal.

Pin 2: Trigger. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. The output is low if the voltage at this pin is greater that 2/3 V_{cc}. However, when a negative going pulse of amplitude larger that 1/3 V_{cc} applied to this pin, the comparator2 output goes low, which in turn switches the output of the timer high. The output remains high as long as the trigger terminal is held at a low voltage.

Pin 3: There are two ways a load can be connected to the output terminal: either between pin 3 and ground (pin 1) or between pin 3 and supply voltage $+V_{cc}$ (pin 8). When the output is low, the load current flows through the load connected between 3 and $+V_{cc}$ into the output terminal and is called the sink current. However, the current through the grounded load is zero when the output is low. For this reason, the load connected between 3 and $+V_{cc}$ is called normally **on load** , and that connected between pin 3 and ground normally off load and that connected between pin 3 and ground is called the normally **off load**.

Pin 4: Reset. The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to $+V_{cc}$ to avoid any possibility of false triggering.

Pin 5: Control voltage. An external voltage applied to this terminal changes the threshold as well as the trigger voltage. In other words, by imposing a voltage on this pin or by connecting a pot between this pin and ground, the pulse width of the waveform can be varied. When not used, the control pin should be bypassed to ground with a 0.01μF capacitor to prevent noise problems.

Pin 6: Threshold. This is the non-inverting input terminal of comparator 1, which monitors the voltage across the external capacitor. When the voltage at this point is $\geq$ threshold voltage $\frac{2}{3}V_{cc}$, the output of comparator 1 goes high, which in turn switches the output of the timer low.

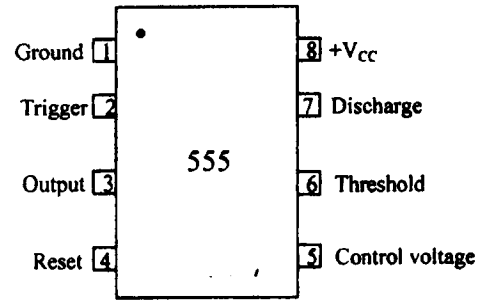


Fig.8.8(a) 555 timer connecting diagram

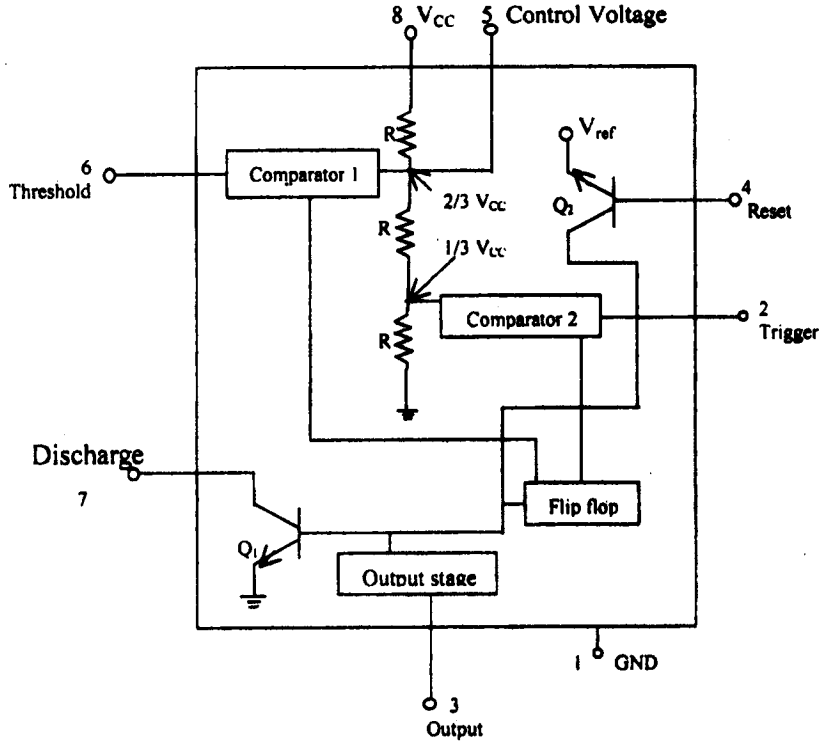


Fig.8.8(b) Block diagram

The important features of the 555 Timer are

(1) It operates on +5 to +15v supply voltage in both free running (astable) and one shot (mono stable) modes; **(2)** It has an adjustable duty cycle; timing is from micro seconds through hours; **(8)** It has high current output; it can source or sink 200 mA; **(4)** The output can drive TTL and has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature.

the left end of R. Because of the virtual ground, the input current is constant and is given by $I_{in} = \frac{V_{in}}{R}$.

This constant current flows into the capacitor and increases its charge given by $Q = CV$.

From which $V = \frac{Q}{C}$ .....(8.29)

This means the capacitor voltage V increases linearly with the polarity show in Fig 8.7a. Because of the phase inversion of the OP AMP, the output voltage is a negative ramp, as shown in Fig.8.7c. At the end of the pulse period, the input voltage returns to zero, and charging current stops. Because the capacitor holds its charge, the output remains constant at negative level.

To get a formula for the output voltage, divide both sides of Eq.(8.29) by T. Thus

$$\frac{V}{T} = \frac{Q/T}{C}$$

Since a constant current I is flowing into the capacitor $\frac{Q}{T} = I$ and hence

$$\frac{V}{T} = \frac{1}{C} \quad (OR) \quad V = \frac{IT}{C}$$

This is voltage across the capacitor with the polarity shown in Fig.8.7a. Because of the phase inversion, $V_{out} = -V$.

8.6 THE 555 TIMER

8.6.1 The 555 Timer and its pin configurations: Signetic corporation introduced this device as the SE / NE555 in early 1970 for the first time . It is one of the most versatile linear integrated circuit. The applications of 555 timer includes mono-stable and astable multi-vibrators, dc-dc converters, digital logic probes, waveform generators, analog frequency meters and tachometers, temperature measurement and control, infrared transmitters, burglar or toxic gas alarm, voltage regulators, electronic eyes and many others. The 555 is a monolithic timing circuit that can produce accurate and highly stable time delays or oscillation. In other words, the timer basically operates in one of the two modes: either as a mono stable multi-vibrator (one shot) or as an astable (free running) multi-vibrator. The device is available as an 8 pin metal can, as an 8-pin mini DIP or a 14-pin DIP. Fig.(8.8) shows that the pin connection diagram and the block diagram of the SE/NE 555 timer. The SE 555 is designed for the operating temperature range of –55 to +125^{0}c, while NE 555 operates over a temperature range of 0 to +70^{0}c.

Therefore, high slew rate op-amps should be used for the generation of relatively higher frequencies.

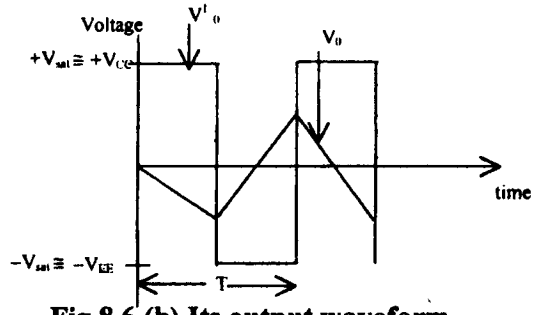


Fig 8.6 (b) Its output waveform.

RAMP GENERATOR

An integrator circuit performs the mathematical operation called integration. Its common application is to use a constant input voltage to produce a ramp of output voltage. (A voltage that changes linearly with time). With an OP AMP, we can build an integrator; a circuit that produces a ramp output from a rectangular input Fig.8.7a

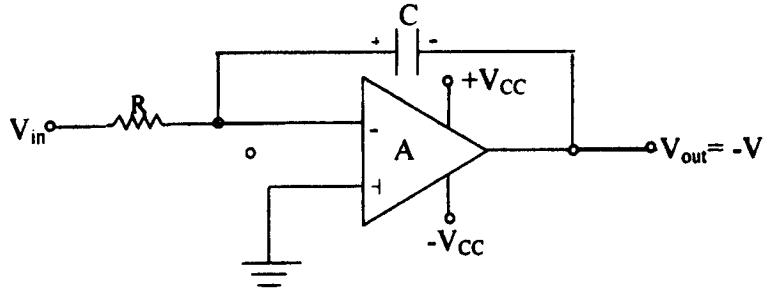


Fig 8.7 (a) Ramp generator

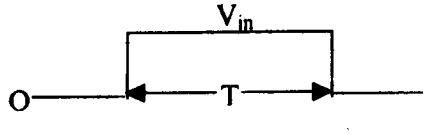


Fig 8.7(b)

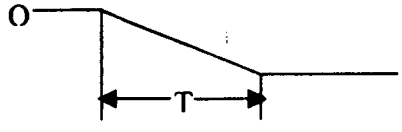


Fig 8.7(c)

shows an OP AMP integrator. Its input is a typical rectangular pulse shown in Fig8.7b. Here V_{in} represents a constant voltage during pulse time T and is applied to

$$f_0 = \frac{1}{2RC} \qquad \text{-------- (8.28),}$$

Eq.(8.28) shows that the smaller the RC time constant, the higher the output frequency f_0 and vice versa. As in the sine wave oscillator, the highest frequency square wave generated is also set by the slew rate of the op-amp. In practice, each inverting and non-inverting terminal needs a series resistor R_s to prevent excessive differential current flow because the input of the op-amp is subjected to large differential voltage. R_s should have a value of 100 KΩ or higher.

8.5.2 TRIANGULAR WAVE GENERATOR Recall that the output waveform of the integrator is triangular if its input is a square wave. It means that a triangular wave generator can be formed by simply connecting an integrator to the square wave generator of Fig. 8.5. The resultant circuit is shown in Fig.8.6(a). The circuit requires a dual op-amp, two capacitors and at least five resistors. The frequency of the square wave and triangular wave is the same. For fixed R_1, R_2 and C values, the frequency of the square wave, as well as triangular wave, depends on the resistance R. As R is increased or decreased, the frequency of the triangular wave will decrease or increase accordingly. Although the amplitude of the square wave is constant; ($\pm V_{sat}$), the amplitude of the triangular wave decreases with an increase in its frequency, and vice versa.

The input of integrator A_2 is a square wave, while its output is a triangular wave, however, the output of A_2 to be triangular wave requires that $5R_3C_2 > T/2$, where T is the time period of the square wave input. As a general rule, R_3C_2 should be equal to T. To obtain a stable triangular wave, it may also be necessary to shunt the capacitor C_2 with the resistor $R_4 = 10R_3$ and connect an offset voltage compensating network at the non-inverting terminal of A_2. As with any other oscillator, the frequency of the triangular wave generator is limited by slew rate of the op-amp.

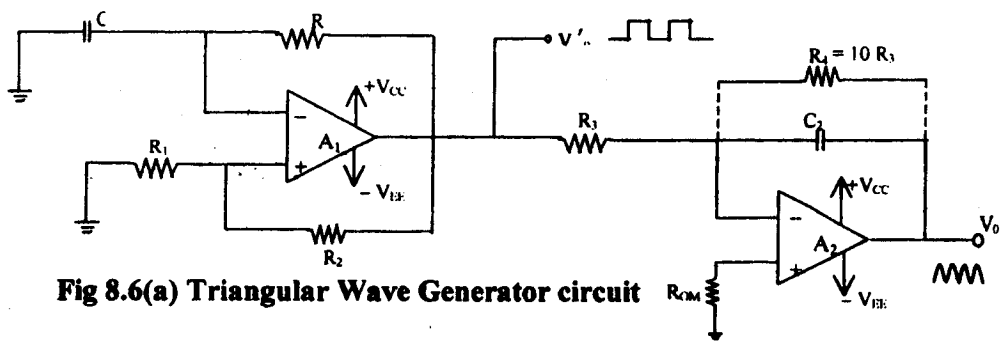


Fig 8.6(a) Triangular Wave Generator circuit

For example, suppose that the output offset voltage v_{001} is positive and that, therefore voltage v_1 is also positive. Since initially the capacitor C acts as a short circuit, the gain of the amplifier is very large (A).

Hence v_1 drives the output of the op-amp to its positive saturation + V_{sat} with the output voltage of the op-amp as $+V_{sat}$, the capacitor C_2 starts charging toward $+V_{sat}$ through the resistor, R. However, as soon as the voltage v_2 across the capacitor is slightly more positive than v_1, the output of op-amp is forced to switch to a negative saturation, $-V_{sat}$. With the op-amps output voltage as negative saturation, $-V_{sat}$ the voltage v_1 across R_1 is also negative,

$$\text{since } v_1 = \frac{R_1}{R_1 + R_2}(-V_{sat}) \qquad \text{---------- (8.25)}$$

Thus the net differential voltage $v_{id} = v_1 - v_2$ is negative, which holds the output of the op-amp in negative saturation. The output remains in negative saturation until the capacitor C discharges and then recharges to a negative voltage slightly higher than the $-v_1$ [see Fig 8.5(b)]. Now, as soon as the capacitor voltage v_2 becomes more negative than $-v_1$, the net differential voltage v_{id} becomes positive and hence drives the output of the op-amp back to its positive saturation $+V_{sat}$. This completes one cycle. With output at $+V_{sar}$, and voltage v_1, at the non-inverting input is

$$v_1 = \frac{R_1}{R_1 + R}(+v_{sat}) \qquad \text{---------(8.26)}$$

The time period T of the output waveform is given by

$$T = 2RC \ln\left(\frac{2R_1 + R_2}{R_2}\right) \qquad \text{--------- (8.27(a))}$$

$$\text{or } f_0 = \frac{1}{2RC \ln\left(\frac{2R_1 + R_2}{R_2}\right)} \qquad \text{--------- (8.27(b))}$$

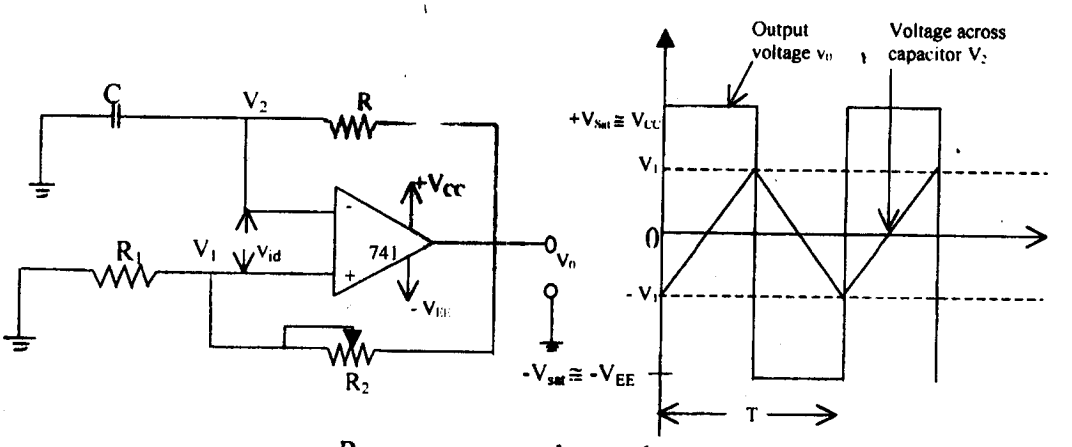
Eq.8.27(b) indicates that the frequency of the output f_0 is not only a function of the RC time constant but also of the relationship between R_1 and R_2. For example, if $R_2 = 1.16\ R_1$, Eq.8.27(b) becomes

Hence, for a stable operation of the oscillator: R_3 is selected slightly larger than $2R_4$ so that the maximum gain requirement is fulfilled.

8.5 SQUARE WAVE AND TRIANGULAR WAVE GENERATORS

8.5.1 Square Wave Generator

In contrast to sine wave oscillator, square wave outputs are generated when the op-amp is forced to operate in the saturated regions, that is, the output of the op-amp is forced to swing repetitively between positive saturation + V_{sat} ($\cong$ + V_{CC}) and negative saturation - V_{sat} ($\cong$ - V_{EE}), resulting in the square wave output. Such a circuit is shown in Fig.8.5. This square wave generator is also called a **free-running multi-vibrator.**



$$|v_1| = \frac{R_1}{R_1 + R_2}|V_{sat}|;\ f_0 = \frac{1}{T} = \frac{1}{2RC} \text{ if } R_2 = 1.16R_1$$

Fig 8.5(a) Square wave generator (b) Wave form of output voltage. v_0 and capacitor voltage v_2 of the square wave generator.

Assume that the voltage across the capacitor C is zero volts at the instant the dc supply voltages +V_{CC} and –V_{EE} are applied. This means that the voltage at the inverting terminal is zero initially. At the same instant, however, the voltage v_1 at the non-inverting terminal is very small finite value, that is a function of the output offset voltage V_{ooT} and the values of R_1 and R_2 resistors. Thus the differential input voltage v_{id} is equal to the voltage v_1 at the non-inverting terminal. Although very small, voltage $v_1$will start to drive the op-amp into saturation.

$$v_i = v_0 \frac{R \frac{1}{j\omega C}}{R \frac{1}{jC} + R^2 + 2R.\frac{1}{j\omega C} - \frac{1}{\omega^2 C^2}}$$

$$= v_0 \frac{1}{1 + j\omega RC + 2 - \frac{j}{\omega RC}} = v_0 \frac{1}{3 + j\left(\omega RC - \frac{1}{\omega RC}\right)} \quad \text{--------- (8.20)}$$

In order to have zero phase between v_i and v_0, the j-terms must be zero i.e.,

$$\omega RC - \frac{1}{\omega RC} = 0;$$

$$\omega^2 = \frac{1}{R^2C^2}$$

$$\omega = \frac{1}{RC}; \quad f = \frac{1}{2\pi RC} \quad \text{--------- (8.21)}$$

Substituting this frequency in equation (8.20)

$$v_i = \frac{1}{3} v_0 \quad \text{--------- (8.22)}$$

Eq.8.22 shows that there is a loss of voltage gain in the feedback network by a factor of 8. Therefore, the amplifier should have minimum voltage gain as 3 for oscillations.

The input voltage v_1 at the inverting point of the op-amp may be written as

$$v_i = \frac{v_0 R_4}{R_3 + R_4} \quad \text{--------- (8.23)}$$

Equating Eq.(8.22) and (8.23), we get

$$\frac{1}{3} = \frac{R_4}{R_3 + R_4}$$

$$R_3 = 2R_4 \quad \text{--------- (8.24)}$$

properly cut crystal shows the characteristic of a resonant circuit. The crystal oscillator possesses excellent frequency stability.

2. Radio frequencies: The frequency of electromagnetic radiation with in the range 1000kHz – 1000MHz.
3. Saw-tooth wave: A wave form in which the shape resembles the teeth of a saw. The voltage builds slowly and linearly up to a peak value (maximum) and when falls almost instantaneously to zero or valley (minimum) value in each cycle.
4. Potentiometer: A variable wire wound resistor with three leads, the value of resistor varies between extreme lead and wiper.
5. Wien bridge: This involves an RC bridge circuit in which a frequency adjusting network is constructed of a series combination of R and C connected from the output of the op-amp to the non-inverting input of the op-amp and of a parallel combination of R and C from the non inverting input of the op-amp to the ground connection.
6. Dual in line package: In the dual – in – line package (DIP) the chip is mounted inside a plastic or ceramic case.
7. Metal can type: The chip is encapsulated in a metal or plastic case. The metal can is best suited for power amplifiers because metal is a good heat conductor and consequently has better dissipation capability than the flat-pack or dual – in – line package.
8. Flip-Flop: The most important memory element is the Flip – Flop which is made up of an assembly of logic gates. It can store one bit of binary data (logic 1 or 0)

8.9 SELF-ASSESSMENT QUESTIONS

Long Answer Questions:

1) Describe the phase shift oscillator and obtain an expression for frequency of oscillations.
2) Derive an expression for the frequency of oscillation for Wien bridge oscillator. How is the minimum gain requirement fulfilled in this oscillator?
3) What are the important features or of the 555 Timer ?.
4) Explain the operation of 555 timer as an astable multi-vibrator.

Short answer Questions

1. Define an oscillator.
2) Why is the positive feedback required for oscillators?
3) What are the two conditions for oscillators?

4) How are oscillators classified?
5) Explain the frequency stability and its significance.
6) What are the two basic modes in which the 555 Timer operates?

8.10 TEXT AND REFERENCE BOOKS

(1) Operational Amplifiers and Linear Integrated Circuit Technology by Ramakanth A. Gaykwad Prentice Hall Inc.,
(2) Basic Electronics by DC Tayal, Himalaya Publish Co.,
(3) Foundations of Electronics
By D. Chattopadhyay, PC Rakshit, B. Saha, M.N. Purohit
Second Edition, Wiley Eastern Ltd,.
(4) Integrated Electronics by Millman & Halkias (MH)

OP AMP CIRCUITS AND IC VOLTAGE REGULATORS

OBJECTIVES OF THE LESSON

To learn about some more important applications of OP AMPs and Integrated Circuit fixed and variable D.C. voltage regulators

STRUCTURE OF THE LESSON

9.1 INTRODUCTION

In the previous lessons of this unit, we studied some applications of Op Amp. We learn some more in this unit. Many more are left uncovered due to lack of space. Although IC voltage regulators are not in the syllabus, these are included in practical paper. So these aspects are also included in this lesson. A course in Undergraduate course in analog electronics cannot be considered as complete without learning some more applications like Active filters, PLLs, VCOs etc. Unfortunately they are not included in the syllabus and the students have to learn modern topics like these and switching voltage regulators etc to face the competition.

9.2 THE COMPARATOR

An important application of the OP-AMP is comparator. OP-AMP are useful is comparing the magnitudes of two signals. If one signal is applied to the inverting input and the other to the non-inverting input, the output of the amplifier is zero only when the two signals are equal and the output is saturated either positively or negatively when the inputs are unequal.

Basically the circuit is shown in Fig9.1a its action is demonstrated by the transfer curve of Fig.9.1b

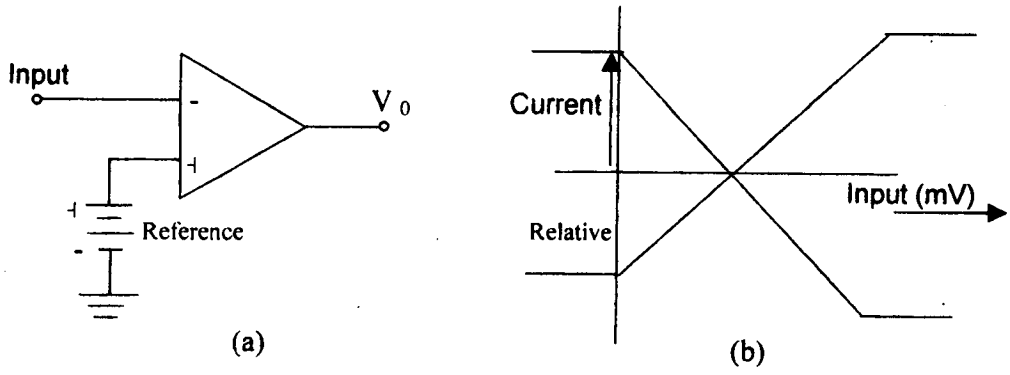


Fig. 9.1 a) Comparator and b) its transfer characteristic

When the input signal is slightly greater than the reference voltage, the output swings to saturation. When the input signal is slightly less than the reference voltage, the output swings to saturation on the other side and output voltage reverses. The amplifier is driven to saturation in each direction.

A faster operating circuit which keeps the circuit out of the saturation condition by use of directional feedback is the zero crossing detector (Fig.9.2). Depending on the input voltage polarity, the amplifier has large feedback through one diode or the other and remains in the linear operating region.

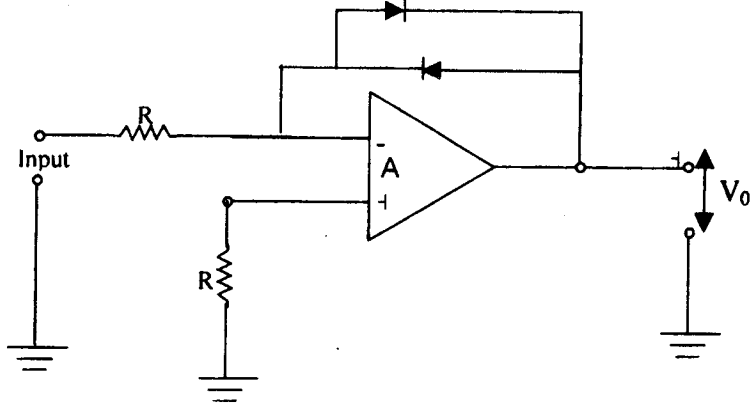


Fig.9.2 Comparator as zero crossing detector

If the input of an OP-AMP comparator is sine wave, the output is a square wave. If a zero-crossing detector is used, a symmetrical square wave results as shown in figure. The comparator may be used as timing marker generator from a sine wave, phase meter, amplitude distribution analyzer and pulse time modulation.

9.3 SCHMITT TRIGGER

By employing positive (regenerative) voltage-series feedback, as is done in figure and for the astable and monostable multivibrators, the gain may be increased greatly. Consequently the output excursion takes place in a

time interval during which the input is changing by much less than 2 mV theoretically, if the loop gain $-\beta A_V$ is adjusted to be unity, then the gain with feedback A_{Vf} becomes infinite. Such an idealized situation results in an abrupt (Zero rise time) transition between the extreme value of output voltage. If a loop gain in excess of unity is chosen, the output waveform continues to be virtually discontinuous at the comparison voltage. However, the circuit now exhibits a phenomenon called hysteresis, backlash, which is explained below.

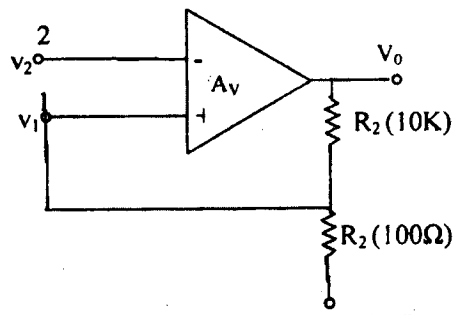


Fig 9.1 Schmitt trigger

The regenerative comparator of Fig.9.1 is commonly referred to as a "Schmitt trigger " (after the inventor of a vacuum-tube version of this circuit). The input voltage is applied to the inverting terminal 2 and the feedback voltage to the non-inverting terminal 1. The feedback factor is $\beta = R_2/(R_1 + R_2)$. For R_2=100Ω, R_1=100K, and A_V = -5,000, the loop gain is

$$-\beta A_V = 0.1 \times \frac{5{,}000}{10.1} = 49.5 >> 1$$

Assume that $v_i < v_1$, so that $v_0 = +V_0 (+5V)$. Then using superposition, we find from figure that

$$v_1 = \frac{R_1 V_R}{R_1 + R_2} + \frac{R_2 V_0}{R_1 + R_2} \equiv V_1 \qquad \ldots\ldots \quad (9.1)$$

If v_i is now increased, then v_0 remains constant at V_0, and $v_1 = V_1 = constant$ until $v_1 = V_1$. At this threshold, critical, or triggering voltage, the output regeneratively switches to $v_0 = -V_0$ and remains at this value as long as $v_i > V_1$. This transfer characteristic is indicated in Fig.9.2.

The voltage at the non-inverting terminal for $v_i > V_1$ is

$$v_1 = \frac{R_1 V_R}{R_1 + R_2} + \frac{R_2 V_0}{R_1 + R_2} \equiv V_2 \qquad \ldots\ldots \quad (9.2)$$

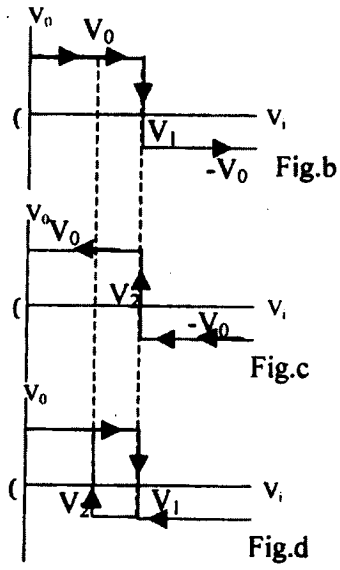


Fig.9.2 The transfer characteristic for For b) increasing v_i c) decreasing v_i d) the composite input-output curve.

For the parameter values given in figure and with $V_0 = 5V$,

$$V_1 = 0.99 + 0.05 = 1.04V$$

$$V_2 = 0.99 - 0.05 = 0.94V$$

Note that $V_2 < V_1$, and the difference between theses two values is called the hysteresis V_H.

$$V_H = V_1 - V_2 = \frac{2R_2V_0}{R_1 + R_2} = 0.10V \qquad \ldots\ldots \quad (9.3)$$

If we now decrease v_i, then the output remains at $-V_0$ until v_i equals the voltage at terminal 1 or until $v_i = V_2$. At this voltage a regenerative transition takes place and, as indicated in fig, the output returns to $+V_0$ almost instantaneously. The complete transfer function is indicated in figure. where the shaded portions may be traversed in either direction, but the solid segments can only be obtained if v_i varies as indicated by the arrows. Note that because of the hysteresis, the circuit triggers at a higher voltage for increasing than for decreasing signals.

We note above that transfer gain increases from 5,000 toward infinity as the loop gain increases from zero to unity, and that there is no hysteresis as long as $-\beta A_V \leq 1$. However, adjusting the gain precisely to unity is not feasible. The DIFF AMP parameters and, hence the gain A_V, are variable over the signal excursion. Hence, an adjustment which ensures that the maximum loop gain is unity would result in voltage

ranges where this amplification is less than unity, with a consequent loss in speed of response of the circuit. Furthermore, the circuit may not be stable enough to maintain a loop gain of precisely unity for a long period of time without frequent readjustment. In practice, therefore, a loop gain in excess of unity is chosen and a small amount of hysteresis is tolerated. In most cases, a small value of V_H is not a matter of concern. In other applications, a large backlash range will not allow the circuit to function properly. Thus, if the peak-to peak signal were smaller than V_H, then the Schmitt circuit, having responded at a threshold voltage by a transition in one direction, would never reset itself. In other words, once the output has jumped to say V_0, it would remain at this level and never return to - V_0.

The most important use made of the Schmitt trigger is to convert a very slowly varying input voltage into an output having an abrupt (almost discontinuous) waveform, occurring at a precise value of input voltage. This regenerative comparative comparator may be used in all the application listed in sec. For example, the use of the Schmitt trigger as a squaring circuit is illustrated in fig. The input signal is arbitrary except that it has a large enough excursion to carry the input beyond the limits of the hysteresis range V_H. The output is square wave as shown, the amplitude of which is independent of the peak-to peak value of the input waveform. The output has much faster leading and trailing edges than does the input.

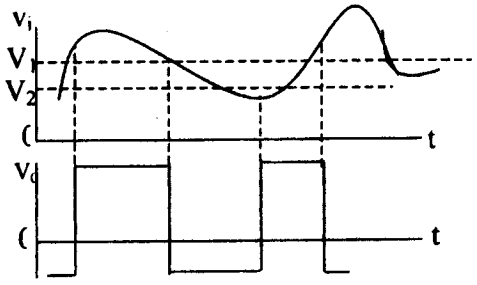


Fig.9.3 Response of the Schmitt trigger to an arbitrary input signal

9.4 OP-AMP AS VOLTAGE REGULATOR

In regulators, voltage v_o should be independent of input voltage variations and the load current variations. If V_{ref} is fixed then output voltage V_0 in circuit shown in Fig.9.4.

If V_{ref} is fixed and if $R_i = R_f$ then $V_0 = 2V_{ref}$. If $V_{ref} = 5$ volt then output $V_0 = 10V$ i.e., output fixed at 10V and variation in the unregulated power supplies +V and –V are absorbed in the OP-AMP and output is constant. Output can be varied by varying R_f,

R_i or V_{ref}. Regulator circuit with Zener diode is shown in Fig9.4b, V_{ref} has replaced by a regulated Zener diode V_Z. Zener diode should be operating only in breakdown region. The value of V_Z should be less than the output voltage.

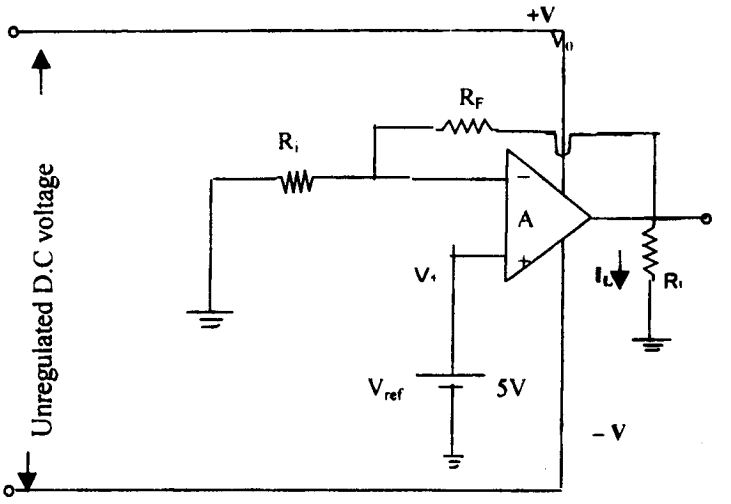


Fig 9.4(a) Op Amp voltage regulator

If V_Z = 5V then input to non-inverting terminal is 5V. Hence, output will be

$$V_0 = \left(1 + \frac{R_f}{R_i}\right) V_Z = 2V_Z = 10V \qquad \text{..... (9.4)}$$

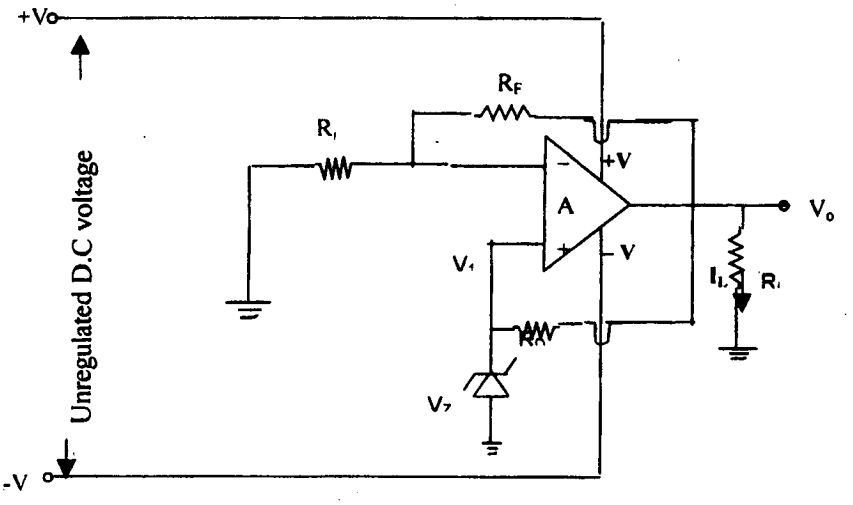


Fig.9.4(b) Op Amp – Zener voltage regulator

Thus Zener diode is properly over load giving a fixed voltage V_Z to the non-inverting terminal. Hence output is fixed at $2V_Z$, eliminating any variation in output due to supplies $(\pm V)$ and load currents I_L.

$$V_0 = \left(1 + \frac{R_f}{R_i}\right) V_{ref} \qquad (9.5)$$

Maximum current that can be supplied by an OP-AMP is only 5 mA. But regulation for higher I_L variation can be obtained by using a "Pass Transistor". It is a power transistor whose current rating is mA, for example transistor 2N3055

9.5 VOLTAGE REGULATORS

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load currents. Although voltage regulators can be designed using op-amps, it is quicker and easier to use IC (Integrated circuit) voltage regulators. Further more, IC voltage regulators are versatile and relatively inexpensive and are available with features such as a programmable output, current/voltage boosting, internal short circuit current limiting, thermal shutdown, and floating outputs for high voltage applications. IC voltage regulators are of the following types.

i) Fixed output voltage regulators: positive and / or negative output voltage

ii) Adjustable output voltage regulators: positive or negative output voltage.

iii) Switching regulators

iv) Special regulators:

Except for the switching regulators, all other types of regulators are called **Linear regulators**. The impedance of a linear regulator's active element may be continuously varied to supply a desired current to the load. On the other hand, in the switching regulator, a switch is turned on and off at a rate such that the regulator delivers the desired average current in periodic pulses to the load. Because the switching element dissipates negligible power in either on or off state, the switching regulator is more efficient than the linear regulator. In addition, most loads cannot accept the average current in periodic pulses. Therefore, most practical regulators are of the linear type.

Voltage regulators are commonly used for on-card regulator and laboratory type power supplies. Voltage regulators especially the switching type, are used as control circuits in pulse width modulator (PWM), push-pull bridges, and series type switch mode supplies. Almost all power supplies use some type of voltage regulator IC because, voltage regulators are simple to use, reliable, low cost and above all, available in variety of voltage and current ratings. A vast number of

voltage regulators are available, data sheets and application notes provided by the manufacturers contain information on the design and use of these devices.

9.5.1(d) Fixed voltage regulators: 78xx Series of positive voltage regulators with seven voltage options: The 7800 series consists of three terminal positive voltage regulators with seven voltage options are shown in Table 9.1

These ICs are designed as fixed voltage regulators with adequate heat sinking and can deliver output currents in excess of one ampere (1A). Although these devices do not require external components, such components can be used to obtain adjustable voltage and currents. These ICs also have internal thermal overload protection and internal short circuit current limiting.

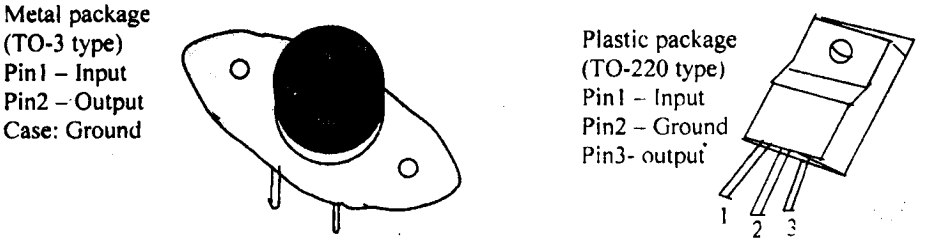


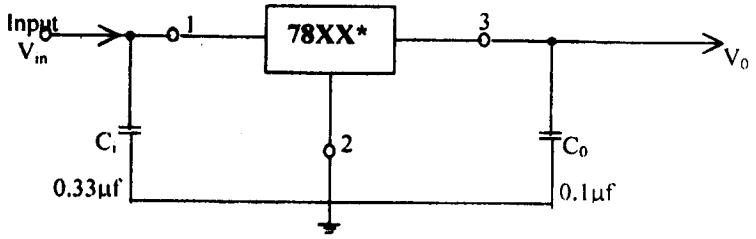
Fig.9.5 (a)The 7800 series regulators (b) Package types

Proper operation requires a common ground between input and output voltages. In addition, the difference between input and output voltages ($V_{in} - V_0$), called drop-out voltage, must be typically 2.0V even during the low point on the input ripple voltage. Further more, the capacitor C_i is required if the regulator is located an appreciable distance from the power supply filter. Even through C_0 is not needed, it may be used to improve the transient response of the regulator.

Device Type	Output Voltage(V)	Maximum input voltage(V)
7805	5.0	35
7806	6.0	35
7808	8.0	35
7812	12.0	35
7815	15.0	35
7818	18.0	35
7824	24.0	40

Table 9.1 The 7800 series regulators (a) voltage options

Typical performance parameter for voltage regulators is line regulation, load regulation, temperature stability and ripple rejection. Line or input regulation is defined as the change in the output voltage for a change in the input voltage and is usually expressed in milli volts or as a percentage of V_0. Temperature stability or average temperature coefficient of output voltage (T_CV_0) is the change in output voltage per unit change in temperature and is expressed in either milli volts/^{0}c or parts per million (ppm)/^{0}c.



9. 6 The 7800 series regulators (c) Standard application
*** XX - These two numbers in type number indicate output voltage**

Ripple rejection is the measure of a regulator's ability to reject ripple voltages. It is usually expressed in decibels. The smaller the values of line regulation, load regulation and temperature stability, the better the regulator.

The 7800 regulators can also be used as current sources. A typical connection diagram of the 7805c as a 0.5A current source is shown in Fig.9.7. The current supplied to the load is given by the equation

$$I_L = \frac{V_R}{R} + I_Q \qquad \text{---------- (9.6)}$$

Where I_Q = quiescent current (amperes)

= 4.3 mA typically for the 7805C

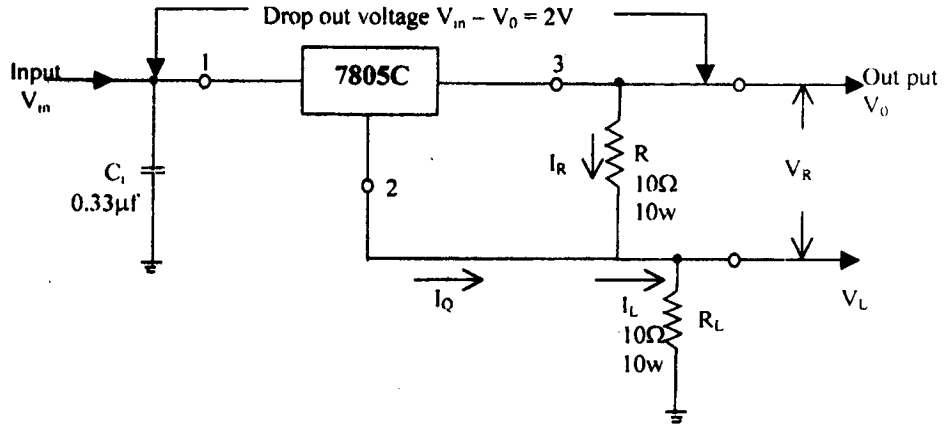


Fig 9.7. The 7805C as a 0.5A current source.

Referring to Fig.9.6, $V_R = V_{23} = 5V$ and $R = 10\Omega$;

Therefore, $I_C \cong 0.5$ A

The output voltage V_0 with respect to ground is

$$V_0 = V_R + V_L \qquad \text{--------- (9.7)}$$

where $V_L = I_L R_L$, the load resistance $R_L = 10\Omega$, hence, $V_L = 5V$, therefore $V_o = 10V$, since the dropout voltage for the 7805c is 2V, the minimum input voltage required is given by the equation

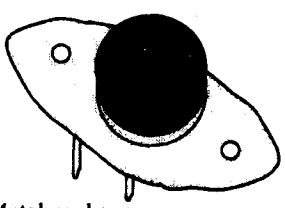
$V_{in} = V_0 +$ Dropout voltage ; $V_{in} = 10 + 2 = 12V$

9.5.1(b) Series of negative voltage regulator with mine voltage options

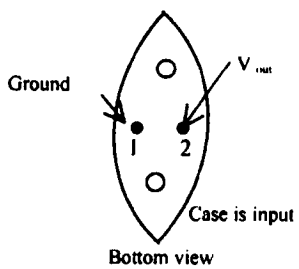
Device Type	Output Voltage (v)	Maximum input voltage (v)
7902	– 2.0	– 35
7905	– 5.0	– 35
7905.2	– 5.2	– 35
7906	– 6.0	– 35
7908	– 8.0	– 35
7912	– 12.0	– 35
7915	– 15.0	– 35
7918	– 18.0	– 35
7924	– 24.0	– 40

Table 9.2 The 7900 series voltage regulators (a) Voltage options

In short, a current source circuit using a voltage regulator can be designed for a desired value of load current (I_L) simply by selecting an appropriate value for R.

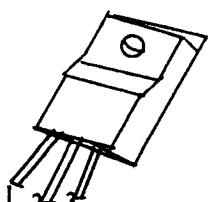


Metal package
(TO-3 type)



TO-3 steel metal can

Plastic package
(TO-3 type)
Pin: 1 Ground
2 Input
3 out put



(Heat sink surface connected to pin 2)

Fig 9.8 The 7900 series regulators (b) Package types

The **7900** series of **fixed output negative voltage regulators** are complements to the 7800 series devices. Further, these negative voltage regulators are available with the same seven voltage options as the 7800 devices and besides, two extra voltage options, - 2V and –5.2V, are also available in the negative 7900 series as shown in fig 9.8(a), the package types in which the 7900 series voltage regulators available are shown in Fig 9.8(b).

9.6 ADJUSTABLE VOLTAGE REGULATORS

The many manufactures that use fixed voltage regulators like the 7800 and 7900 series, in their line of products had to stock and hold an inventory quantities of each voltage in order to always have on hand a specific device for a particular system. Adjustable voltage regulators provided the answers to the excessive inventory and production costs because a single device satisfies many voltage requirements from 1.2 up to 57V. In addition, they have the following performance and relative advantages over the fixed types.

i) Improved system performance by having line and load regulators of a factor of 10 or better

ii) Improved over load protection allows greater output current over operating temperature range.

iii) Improved system reliability with each device being subjected to 100% thermal limit burn-in.

9:6(A) ADJUSTABLE POSITIVE VOLTAGE REGULATORS

The LM317 are a popular series adjustable three-terminal positive voltage regulators. The different grades of regulators in the series are available with output voltage of 1.2 to 57V and the output current from 0.1 to 1.5 A as shown in Table 9.3. The LM 317 series regulators are available in standard transistor packages that are easily mounted and handled Fig.9.9(a). The three terminals are V_{IN}, V_{OUT} and adjustment (ADJ). Fig.9.9(b) shows a typical connection diagram for the LM 317 regulator. From this diagram it is obvious that the LM 317 requires only two external resistors to set the output voltage. When configured as shown in Fig.9.9 (b), the LM 317 develops a nominal 1.25V, referred to as the reference voltage V_{REF} , between the output and adjustment terminal.

This reference voltage is impressed across resistor R_1 and, since the voltage is constant, the current I_1 is also constant for a given value of R_1. Because resistor R_1 sets current I_1, it is called the current set or program resistor. In addition to the current I_1, the current I_{ADJ} from the adjustment terminal also flows through the output set resistor R_2.

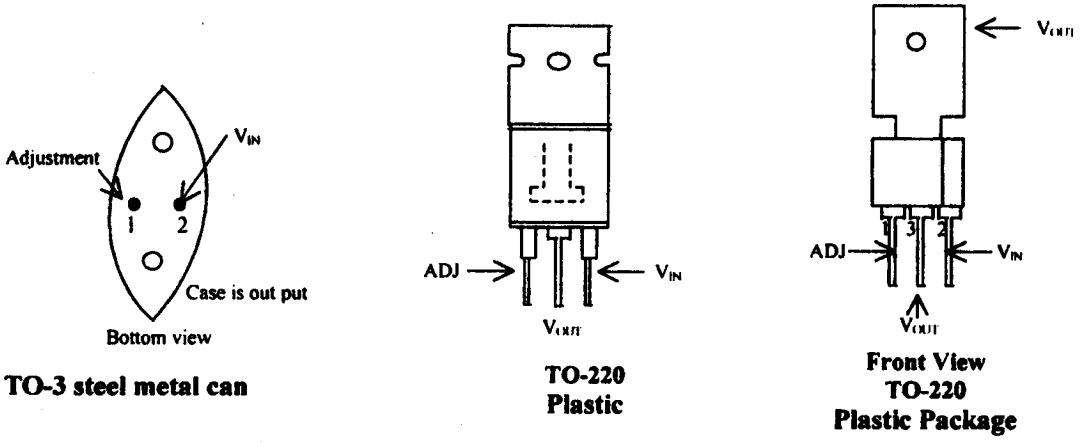
The LM 317 is designed such that I_{ADJ} is very small and constant with line and load changes. The maximum value of adjustment pin current I_{ADJ} is 100μA.

Device	Available V_0 (V)	Output Current (A)	V_{in} max (V)	Ripple rejection (dB)	Package
LM317	1.2 to 37	1.5	40	80	To-39
LM317 H	1.2 to 37	0.5	40	80	To-39
LM317 HV	1.2 to 57	1.5	60	80	To-3
LM317 HVH	1.2 to 37	0.5	40	80	To-39
LM317 L	1.2 to 37	0.10	40	65	To-92
LM317 M	1.2 to 37	0.50	40	80	To-202

Table 9.3 LM317 typical ratings.

Thus, referring to fig 9.9(b), the output voltage V_0 is

$$V_0 = R_1 I_1 + R_2 (I_1 + I_{ADJ}) \qquad \text{--------(9.8)}$$



TO-3 steel metal can | **TO-220 Plastic** | **Front View TO-220 Plastic Package**

Fig. 9.9(a) LM 317 standard package types.

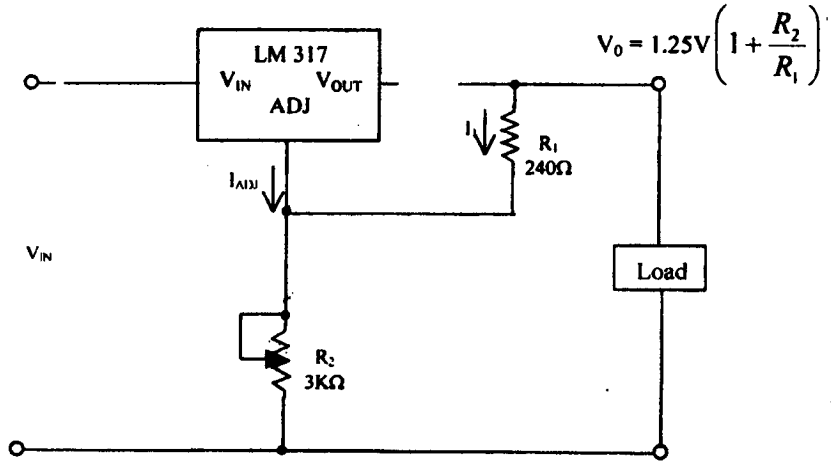


Fig 9.9 (b) LM 317A typical connection diagram.

where $I_1 = \frac{V_{REF}}{R_1}$; R_1 = Current (I_1) set resistor R_2 = output (V_0) set resistor

I_{ADJ} = adjustment pin current.

Substituting the value of I_1 in Eq.(9.8) and rearranging, we get

$$V_0 = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ} R_2 \text{ ---------- (9.9)}$$

Where V_{REF} = 1.25V = reference voltage between the output and adjustment terminals. However, the current I_{ADJ} is very small (100μA) and constant. Therefore, the voltage drop across R_2 due to I_{ADJ} is also very small and can be neglected. In short

$$V_0 = 1.25\left(1 + \frac{R_2}{R_1}\right) \text{ ---------- (9.10)}$$

Eq.(9.10) indicates that the output voltage V_0 is a function of R_2 for a given value of R_1 and can be varied by adjusting the value of R_2 . The current set resister R_1 is usually 240Ω, and to active good load regulation it should be tied directly to the output of the regulator rather than near the load.

9.7 SUMMARY

When large input signals are to be amplified for the operation of output device such as speakers and motors, the amplifier must be capable of handling large amount of power and its efficiency of converting input dc power to output ac power must be high. Such an amplifier is known as a power amplifier. Power amplifiers are classified on the basis of their operating point as class A, B, AB, C etc.

In class A amplifiers, there is always collector current regardless of the time in the cycle of the applied signals. As a result, power losses many be increased. Since the collector current flows only for one half of the input signal in class B amplifier and in order to get output power for full cycle, two class B amplifiers are used in a combination known as push-pull. Therefore, the power losses may be minimized and simultaneously the collector efficiency also increases in class B push-pull power amplifier:

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load currents. Monolithic voltage regulators are available on a variety of different output voltage ratings and also quicker and easier to use. The 7800 is a fixed positive voltage regulator series with seven voltage options while the 7900 is a fixed negative voltage regulator series with nine voltage options. Adjustable voltage

regulator such as the LM 317 is more popular because of its versatility, performance and reliability.

For adjustable negative voltage regulators see reference Text book.

9.8 KEY TERMINOLOGY

1. **Quiescent (Q) point**: The operating point in the absence of signal is called Quiescent point or simply the Q point of the device. The particular Q point at which the device will operate depends on the base current(I_B) and V_{CE}..
2. **Direct Coupling**: To amplify all the frequencies in the signal, signal source is coupled to the amplifier stage directly without using DC blocking capacitors and isolation transformers. In the same manner amplifier output is connected to the load. Direct coupling may be used to connect to the amplifier stage to the other. However precautions must be taken to provide level shifting so that satisfactory biases are established at various points in the circuit. This type of coupling is preferred in the fabrication of the integrated circuits(ICs).
3. **Push-Pull Configuration**: Two transistors amplifiers are said to be connected in push-pull configuration when the amplifiers are connected such that as current in one stage pushes forward, in the other, current pulls back. This configuration avoids the power losses in the transformer core and results in higher efficiency than a two transistor parallel coupled amplifier.
4. **Regulation**: Keeping the output voltage of the DC Power supply constant, irrespective of the variation of the supply voltage and load current is called regulation.
5. **Ripple**: After rectification of the AC signal using a full-wave rectifier to obtain a DC voltage we find that the output is not a pure DC, but contains a small amount of AC voltage which has to be removed by filtering or by incorporating the regulation circuit.

9.9 SELF-ASSESSMENT QUESTIONS

1. Describe the various classes of power amplifier in terms of these operating point.
2. Define efficiency of power amplifier and compare efficiencies in case of A, B and C classes of amplifiers.
3. Obtain an expression for the collector efficiency of transformer coupled class-A transistor power amplifier.
4. Describe a class-B push-pull power amplifier and obtain an expression for its efficiency. How the class-B push-pull amplifier is an advantageous over the class-A amplifier?

5. What do you mean by voltage regulator? List four different types of voltage regulators.
6. What are the advantages of adjustable voltage regulator over the fixed voltage regulators?

9.10 TEXT AND REFERENCE BOOKS

1. Operational Amplifiers and Linear Integrated Circuit Technology by Ramakanth A. Gaykwad Prentice Hall Inc.,
2. Basic Electronics by DC Tayal, Himalaya Publish Co.,
3. Semi Conductor Electronics by A K. Sharma
   New Age International Publishers
4. Foundations of Electronics
   By D. Chattopadhyay, PC Rakshit, B. Saha, M.N. Purohit
   Second Edition, Wiley Eastern Ltd.,

AMPLITUDE MODULATION AND DETECTION

OBJECTIVES OF THE LESSON

In this lesson, we study about the

(i) Processes of amplitude modulation

(ii) Types of amplitude modulation

(iii) Process of detection of AM waves

STRUCTURE OF THE LESSON

10.1 INTRODUCTION

For successful transmission and reception of intelligence (code, voice, music etc) by the use of radio waves, two processes are essential. They are (i) Modulation (ii) Demodulation or detection. To modulate means to regulate or adjust. Speech and music etc. are sent thousands of kilometers away by a radio transmitter. Similarly, a scene in front of a television camera is also sent many kilometers away to viewers. In such cases, the carrier is the high frequency radio wave. The intelligence i.e. video, sound and other data is impressed on the carrier wave and is carried along with it to the destination.

Modulation is the process of combining the low frequency signal with a very high frequency radio wave called **carrier wave** (c.w.). The resultant wave is called **modulated carrier wave**. This job is done at the transmitting station.

During modulation some characteristic of the carrier wave is varied in time with the modulating signal. Accordingly, there are three types of sine wave modulations known as Amplitude Modulation, Frequency Modulation and Phase Modulation.

The A.M. wave contains three frequency components, a carrier frequency (f_c), one component 'above' the carrier frequency ($f_c + f_s$) and the other component 'below' the carrier frequency ($f_c - f_s$) where 'f_c' and 'f_s' are the carrier and signal frequencies respectively. At the receiver the signal is extracted from the modulated carrier. This process is called A.M. detection or demodulation.

10.2 NEED FOR MODULATION

Sometimes, beginners question the necessity of modulation is using a carrier wave to carry the low frequency signal from one place to another. Why not transmit the signals directly and save lot of difficulty? Unfortunately, there are many hurdles in the process of such direct transmission of audio frequency signals. These are

(i) Voice, data and video signals have low frequencies. These waves have relatively short range.

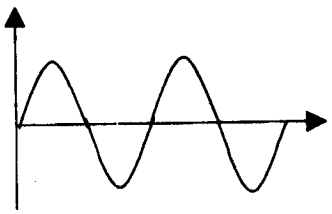
(ii) If everybody transmits these low frequency signals directly, mutual interference will render all of them ineffective.

(iii) Size of antennas required for their efficient radiation would be large, i.e., about 75Km!

Hence, the solution lies in modulation, which enables a low frequency signal to travel very large distances through space with the help of a high frequency carrier wave (f_c). These carrier waves need reasonably sized antennas and care is taken to select the carrier frequencies to avoid interference with other transmitters operating in the same area.

10.3 AMPLITUDE MODULATION

Definition: When the amplitude of high frequency carrier wave is changed in accordance with the instantaneous value of the amplitude of the signal, it is called Amplitude modulation. However, the frequency of the modulated wave remains the same i.e at carrier frequency. The following Fig.10.1 shows the principle of amplitude modulation. Fig 10.1(a) shows the audio electrical signal whereas Fig.10.1(b) shows a carrier wave. Fig.10.1(c) shows the amplitude modulated (AM) wave.



SIGNAL

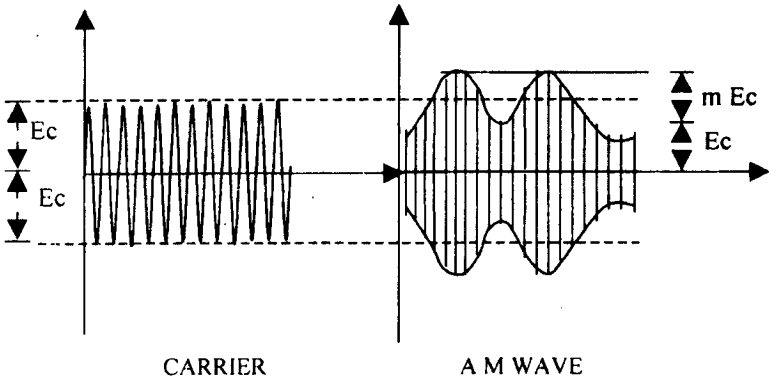


Fig 10.1 Amplitude Modulation

Note that the amplitudes of both positive and negative half cycles of carrier wave are changed in accordance with the signal. Amplitude modulation is done by, an electronic circuit called modulator.

Modulation factor

An important consideration in A.M. is to describe the depth of modulation, i.e the extent to which the amplitude of carrier wave is changed by the signal. This is described by a factor called Modulation index, which may be defined as under.

Definition of Modulation index/factor

The ratio of change of carrier wave amplitude due to modulation to the amplitude of un- modulated carrier wave is called the Modulation factor m.

10.4 Mathematical analysis of A.M. Wave:

A carrier wave may be represented by $e_c = E_c \cos \omega_c t$, where

e_c = instantaneous voltage of carrier

E_c = amplitude of carrier

$\omega_c = 2\Pi f_c$ = angular velocity of carrier of frequency 'f_c'.

The modulating signal can be represented by

$$e_s = E_s \cos \omega_s t \qquad (10.1)$$

where e_s is the instantaneous value of modulating signal. E_s is its amplitude.

$\omega_s = 2\Pi f_s$ = angular velocity of signal frequency 'f_s'.

In amplitude modulation, the amplitude E_c of the carrier wave is varied in accordance with the instantaneous value of the signal as shown in Fig.10.1.

The amplitude of modulated signal can be represented by

$$E = Ec + k_a E_m \cos \omega_s t \qquad (10.2)$$

where k_a is called Coefficient of modulation

The carrier wave amplitude is varied at signal frequency f_s. Therefore

$$e = E_c. (1+ m \cos \omega_s t) \cos \omega_c t. \quad (10.3)$$

where $m= k_aEs/Ec$ is called modulation index or modulation factor

The expression for A.M. wave can be expanded as

$$e = E_c . \cos \omega_c t + m . E_c . \cos \omega_s t . \cos \omega_c t.$$

$$= E_c . \cos \omega_c t + m . \frac{E_c}{2} . \{2 \cos \omega_s t . \cos \omega_c t\}$$

$$= E_c . \cos\omega_c t + m . \frac{E_c}{2} \{\cos (\omega_c+\omega_s)t + \cos (\omega_c-\omega_s)t\}$$

$$= E_c . \cos \omega_c t +. \frac{mE_c}{2} . \cos (\omega_c+\omega_s).t + \frac{mE_c}{2} . \cos (\omega_c -\omega_s) t. \quad (10.4)$$

The following points may be noted from the equation of Amplitude modulated wave.

The A.M. wave is equivalent to the summation of three sinusoidal waves: one having amplitude E_c and frequency 'f_c', the second having amplitude $\frac{mE_c}{2}$ and frequency $(f_c + f_s)$ and the third having amplitude $\frac{mE_c}{2}$ and frequency $(f_c - f_s)$.

The A.M. wave contains three frequencies. They are f_c, $f_c + f_s$ and (f_c-f_s). Thus, the process of amplitude modulation does not change the original carrier frequency but produces two new frequencies $(f_c + f_s)$ and $(f_c - f_s)$, which are called side band frequencies. The sum of carrier frequency and signal frequency i.e.,$(f_c +f_s)$ is called Upper Side Band (USB) frequency. The Lower Side Band (LSB) frequency is $(f_c - f_s)$ i.e., the difference between carrier and signal frequencies. The amplitudes of the side bands are equal and proportional to depth of modulation. It can be shown that the maximum power in each side band occurs when m = 1 and is equal to one fourth of carrier power.

Upper and Lower Sidebands

In the above discussion, it was assumed that the modulating signal was composed of one frequency component only. However, in a broadcasting station, the modulating signal is the human voice (or music), which contains waves with a frequency range of 20-4000 Hz. Each of these waves have its own LSF and USF. When combined together, they give rise to an Upper-side band (USB) and a Lower-side band (LSB) as shown in Fig.10.2.

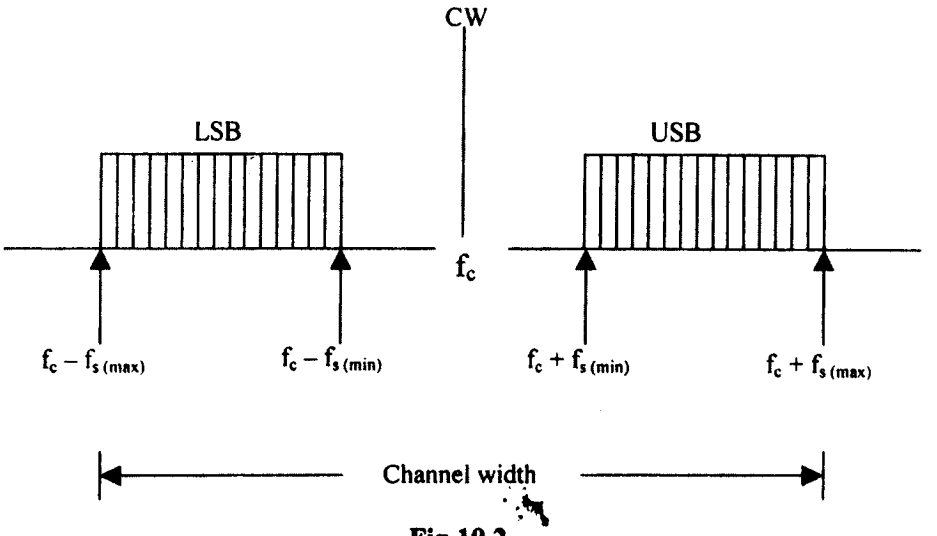


Fig.10.2

The USB, in fact, contains all sum components of the signal and carrier frequency whereas LSB contains their difference components. The channel width (or bandwidth) is given by the difference between extreme frequencies i.e., between maximum frequency of USB and minimum frequency of LSB. As seen

Channel width = 2 x maximum frequency of modulating signal = 2 x f_s(max).

Importance of modulation index

Modulation index, m is used to describe the depth of modulation. It tells about the extent to which the amplitude of the carrier wave has been changed by the signal. Hence, the ration of change of amplitude of carrier wave to the amplitude of normal carrier wave is calle4d the modulation index. m

The modulation index indeed is a number lying between 0 and 1. It is often expressed as a percentage and then called percentage modulation. Modulation index, m plays an important role in determining the strength and quality of signal transmitted. When the carrier wave is modulated to a small degree (for m<<1), the amount of carrier amplitude variation is small. As a result the audio signal becomes stronger and clear. But if m>1, the carrier wave is over modulated and distortion occurs during reception. Therefore, modulation indeed 'm' is an important consideration in amplitude modulation and that its value should always lie between 0 and 1

Power in an amplitude modulated wave

The power carried by a signal is proportional to the square of its amplitude. Equation of A.M. wave suggests that it has three components of amplitudes of with rms values

$\frac{E_C}{\sqrt{2}}, \frac{mE_C}{2\sqrt{2}}, and \quad \frac{mE_C}{2\sqrt{2}}$. The total power of the modulated carrier is given by

$$P_T \propto \left[\frac{E_c^2}{2} + \frac{m^2E_c^2}{8} + \frac{m^2E_c^2}{8}\right] \; or \; P_T \propto \frac{E_c^2}{2}\left(1 + \frac{m^2}{2}\right)$$

But $E_c^2/2$ represents the power of the carrier components

We may write $P_T = P_C(1 + \frac{m^2}{2})$

Power in the side bands = $P_T - P_C = P_C(m^2/2)$

Power in each side band = $P_C(m^2/4)$

RMS power in each sideband = $P_{C\,rms}(m^2/2)$

If R is the load resistance, I_m is the current when carrier is modulated and I_C the current when unmodulated, then

$$\frac{P_T}{P_C} = \frac{I_M^2R}{I_c^2R} = 1 + \frac{m^2}{2}$$

$$I_M^2 = I_c^2\left(1 + \frac{m^2}{2}\right)$$

$$\text{Or } m^2 = 2\left(\frac{I_M^2}{I_c^2} - 1\right)$$

Example: An audio signal given by 15 sin 2Π (2000 t) amplitude-modulates a sinusoidal carrier wave 60 sin 2Π (100,000) t. Assuming ka=1 determine a) modulation index, (b) percent modulation, (c) frequencies of signal and carrier, (d) frequency spectrum of the modulated wave.

Solution. Here carrier amplitude, A = 60 and modulating signal amplitude B = 15. Therefore

a) Modulation index, $m = \frac{B}{A} = \frac{15}{60} = 0.25$

b) b) Percent modulation, M = m x 100 = 0.25 x 100 = 25%

c) f_s = 2000 Hz --------by inspection of the given equation

f_q = 100,000 Hz --------by inspection of the given equation

d) The three frequencies present in the modulated carrier wave are

(i) 100,000 Hz = 100 kHz,(ii) 120,000 or 120 kHz (iii) 80,000 or 80kHz

Experimentally by measuring the maximum and minimum value of the modulated carrier amplitude one can determine the depth of modulation from the relation

$m = (E_{max} - E_{min}) / (E_{max} + E_{min})$

From this relation we see that , when $E_{max} = E_{min}$, $m = 0$ or there is no modulation and when

$E_{min} = 0$ there is 100 % modulation. In commercial radio broadcasting the depth of modulation is maintained around 40%.

10.5 GENERATION OF A.M. WAVE

Amplitude modulation is produced by combining the carrier and the signal frequencies using a non-linear device. Diodes are non-linear devices but they are not used as they do not offer any gain. Transistors behave as non-linear elements and offer gain as such they are suitable for this applications. Fig 10.3 shows a simple amplitude – modulated amplifier.

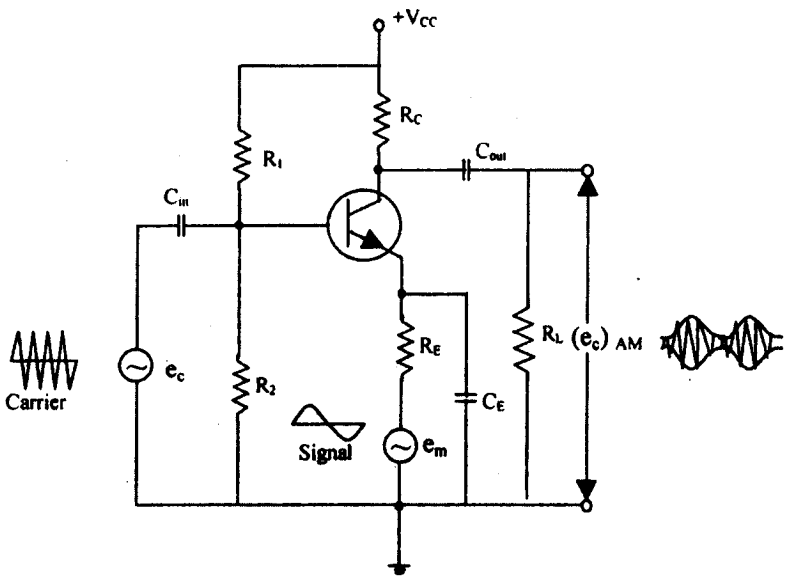


Fig.10.3 An amplitude-modulated amplifier.

The supply V_{CC} in combination with the resistors R_1, R_2, R_C & R_E sets the quiescent point for the transistor. The carrier e_C is the input to the CE amplifier. The circuit amplifies the carrier by a factor A_V where A_V is the voltage gain, so that the amplifier output is $A_V e_C$. The modulating signal e_m is applied in emitter circuit and hence forms a part of the biasing. It produces variation in emitter current at modulating frequency, which in turn produces variations in base emitter resistance and gain A_V. Thus, the amplitude of the carrier varies in accordance with the strength of the signal there by producing Amplitude modulated output across 'R_L'.

Forms of amplitude modulation:

We know now that one carrier and two side bands are produced in A.M. generation. It is not necessary to transmit all these signals to enable the receiver to reconstruct the original signal. Accordingly, we may attenuate or altogether remove the carrier or any one of the side bands with out affecting the communication process. The advantages are (i) Less transmitted power and (ii) Small bandwidth required.

The different suppressed component systems are: (a) DSB-SC (b) SSB-TC (C) SSB-SC,

(a)DSB-SC: It stands for double side band suppressed carrier system. Here carrier component is suppressed there by saving enormous amount of power.

(b)SSB-TC: It stands for single side band transmitted carrier system. In this case one sideband is suppressed but the other sideband and carrier are transmitted.

(c) SSB-SC: It stands for single side band suppressed carrier system. It suppresses one side band and the carrier and transmits only the remaining side bond.

Out of the above three systems, the SSB-SC (or simply SSB) is more preferable because of its advantage over other.

Generation of SSB-SC or SSB systems

The SSB-SC or simply SSB is generated mainly through the following three methods:

(1) Filter method.

(2) Phase cancellation (shift) method.

(3) The third method.

1. Filter method: In this method, DSB-SC signal is generated by, the balanced modulator. This signal is allowed to pass through side band filters, which are narrow band pass filters that only allow to pass the desired side band of frequencies. The filter may be a LC, mechanical or a crystal filter. All these filters have the disadvantage that their operating frequency is below the usual transmitting frequencies. Thus a balanced mixer and crystal oscillator are used to provide up conversion to the final transmitter frequency.

2. Phase shift method: In this method, two balanced modulators and two phase shifting networks are used. One of the balanced modulator receives the carrier voltage shifted by 90^0 and the modulating voltage signal while the other balanced modulator receives the carrier voltage and the modulating voltage shifted by 90^0. The output of both modulators consists of sidebands only. The signal is applied directly to the modulator M_1, therefore the modulator puts out two side bands, each one is shifted in phase by 90^0. The signal is shifted 90^0 before it is applied to the modulator, therefore,

the modulator also puts two side bands, but in this case the upper and lower side bands and shifted by $+90^0$ and -90^0 respectively. The two lower side bands, which are out of phase, when combined in the adder cancel each other. The upper side hands, which are in phase add directly in the adder. Thus SSB in which lower sideband is removed is produced. The block diagram of this method is shown in the Fig.10.4

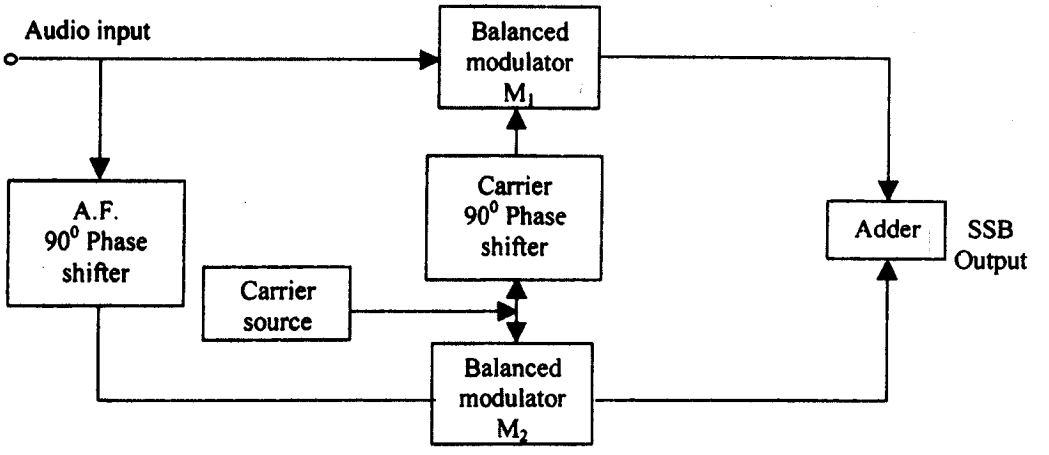


Fig 10.4 SSB – SC transmitter using phase shift.

The output of first balanced modulator M_1

$$v_1 = 2\, v_c .\, m_a \cos \omega_c t \,.\, \sin \omega_m t \,. \qquad \text{---------- (10.5)}$$

The output from the balanced modulator M_2

$$v_2 = 2\, v_c\, m_a \text{ co sin } \omega_c t \,.\, \cos \omega_m \,.\, t \qquad \text{---------- (10.6)}$$

The summing amplifier, the resultant output

$$v = v_1 + v_2 = 2\, v_c \,.\, m_a \sin (\omega_c + \omega_m)t \qquad \text{---------- (10.7)}$$

(By adding Eqs.(10.5) and (10.6))

Thus the output contains only upper side band, similarly, the output with lower side band can be obtained by passing the signal carrier directly to balanced modulator M_1 and each through 90^0 phase shifting networks to the modulator M_2.

The third method:-

This method has the ability to generate SSB at any frequency and the low audio frequencies. It neither refuses a filter circuit nor a wide band, audio phase shift network. The circuit is identical to that of the phase shift method, but the way in which voltages are fed to the two balanced modulators has been changed. Due to this reason, this method is called **Modified phase shift method** the block diagram of the method is shown in the following Fig.10.5.

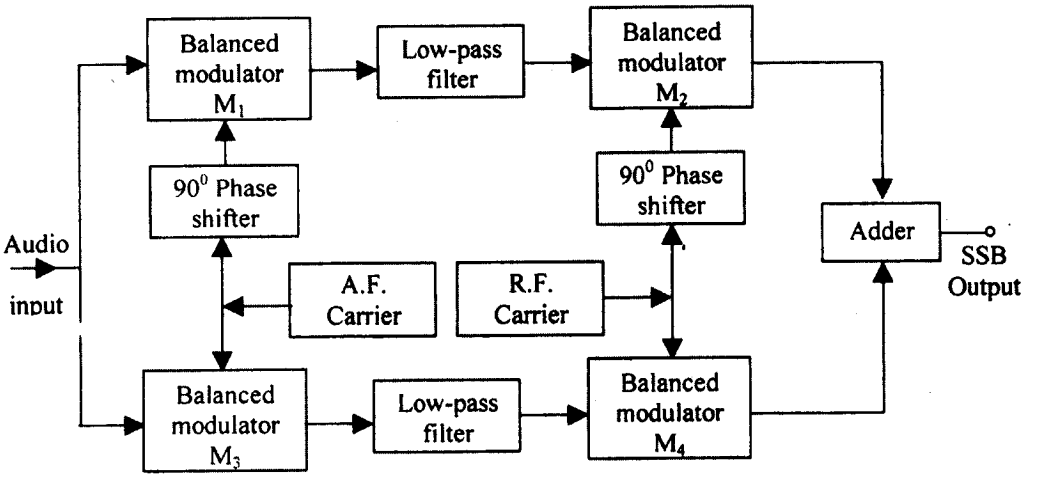


Fig 10.5 Third method for SSB generation.

10.6 DEMODULATION OF A.M. WAVES

Definition of Demodulation:

The process of recovering the audio signal from the modulated wave is known as demodulation or detection.

At the broadcasting station, modulation is done to transmit the audio signal over larger distances to a receiver. When the modulated wave is picked up by the radio receiver, it is necessary to recover the audio signal from it. This process is accomplished in the radio receiver and is called demodulation.

Necessity of Demodulation:

We know that an A.M. wave consists of carrier and side band frequencies. The audio signal is in side-band frequencies, which are radio frequencies. If the modulated wave after amplification is directly fed to the speaker, no sound will be heard because of the inertia of the diaphragm as it is not able to respond to such high frequencies.

Essentials of demodulation:

For a modulated wave to be audible, it is necessary to change the nature of modulated wave. This is done by a circuit called detector. A detector circuit performs the following two functions

It rectifies the modulated wave.

It separates the audio signal from the carrier.

The demodulation can be accomplished with the help of a diode detector.

A.M. Diode detector:

Diode detection is also known as envelope detection or linear detection.

In appearance it looks like an ordinary half wave rectifier circuit with capacitor input. As shown in the below fig--

It is called envelope detection because it recovers the A.F. signal envelope from the composite signal. Similarly, diode detector is called linear detector because its output is proportional to the voltage of the input signal.

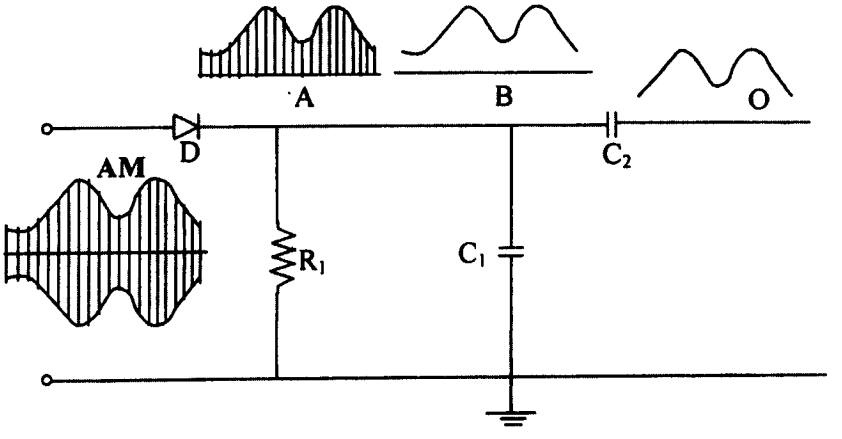


Fig.10.6 Simple detector of Amplitude Modulated Wave

Circuit Action:

This circuit involves the rectification of the signal, and filtering the r.f. and dc components. The signal is rectified by diode 'D'. The rectified wave is shown at A in the Fig.10.6 The combination $C_1 - R_1$ removes the high frequency component and provide the signal super posed over a dc component. The dc component is eliminated by capacitor 'C_2' to give the output.

10.7 SUMMARY

During modulation some characteristic of the carrier wave is varied in time with the modulating signal. Accordingly there are three types of sine wave modulations known as amplitude Modulation, Frequency Modulation and Phase Modulation. When the amplitude of high frequency carrier wave is changed in accordance with the instantaneous value of the amplitude of the signal, it is called amplitude modulation. The process of amplitude modulation does not change the original carrier frequency but produces two new frequencies ($f_c + f_s$) and ($f_c - f_s$), which are called side band frequencies.

Power contained in a modulated carrier = $P_T = P_C(1+\frac{m^2}{2})$ where P_C is the power of unmodulated carrier. The process of recovering the audio signal from the modulated wave is known as demodulation or detection.

10.8 KEY TERMINOLOGY

Modulation: Process of combining low frequency signal with a high frequency radio wave (carrier wave).

Balanced modulator: A modulation circuit which cancels but the product term does not cancel.

10.9 SELF – ASSESSMENT QUESTIONS

LONG ANSWER QUESTIONS

1. Draw the circuit diagram of amplitude modulator and explain its working.
2. Define modulation, define amplitude and frequency modulations and explains about them.
3. Explain how the Amplitude modulated waves are generated. Give the necessary diagrams.
4. With neat diagram and waveform, explain how the Amplitude modulated waves are detected.
5. Give the analysis of an AM wave. What are side bands? Explain Them.
6. Explain a method for the generation of SSB modulation.

SHORT ANSWER QUESTIONS

1. Discuss the need for modulation in radio and TV Transmissions.
2. What are sidebands produced in AM Wave. Explain them.
3. Distinguish between Amplitude and frequency modulation.
4. Write in detail about AM diode detector.
5. Explain now a SSB modulated system can be detected.

causing overloading. If the depth of modulation is decreased to 40%, determine

8. Draw the circuit diagram of a diode detector and discuss its working.
9. Explain the need for modulation.
10. Show that an AM wave contains a carrier and two side bands for every modulating frequency.

10.10 TEXT AND REFERENCE BOOKS

1. Integrated Electronics by Millman and Halkias
2. Electronic Communications by Kennedy
3. Principles of Digital Electronics by Malvino and Leach
4. Basic Electronics and Linear Circuits - Bhargava etc

REFERENCE BOOKS

1. A text lab manual in Electronics by ZBAR (Tata Mc graw Hill)
2. Electronics fundamentals by JD Ryder
3. Modern Electronics Communications by Gray and Miller
4. Digital Electronics by William H.Gothman
5. Op.Amp and linear integrated Circuits by Ramakant Gayakwad
6. Electronic Devices and Circuits by Samuel Seely.

FREQUENCY MODULATION AND DETECTION

OBJECTIVES OF THE LESSON

In this chapter, we study about the

(i) Processes of frequency modulation

(ii) Frequency modulation circuits

(iii) Process of detection of FM waves

STRUCTURE OF THE LESSON

INTRODUCTION

Amplitude modulated signals are influenced by noise. Most noise appears as additional amplitude modulation on the signal. The effect of noise is minimized in frequency modulation. Even though AM is preferred to establish radio stations, the need for number of stations limit the bandwidth allowed for transmitting AM signals The commercial broadcasting uses only 5KHz on either side so that the total bandwidth of AM is limited to 10KHz. This naturally removes the high frequency notes in voice or music. For high fidelity, the bandwidth has to be more and in FM the entire audio frequency region can be used for modulation. This will enable the listeners to appreciate the music much better than in AM. So, now a days, more FM stations are coming up. In broadcasting TV signals, both amplitude and frequency modulation are used. So, in this lesson we learn the details of production and detection of FM waves.

Definition: When the frequency of carrier wave is changed in accordance with the instantaneous value of signal, it is called **Frequency Modulation**.

In frequency modulation, only the frequency of the carrier wave is changed in accordance with the signal. However, the amplitude of the modulated wave remains the same i.e. carrier wave amplitude. The amount of change in frequency is determined by the amplitude of the modulating signal whereas rate of change is determined by the frequency of the modulating signal as shown in Fig.11.1.

In FM, information or intelligence is carried as variations in carrier frequency.

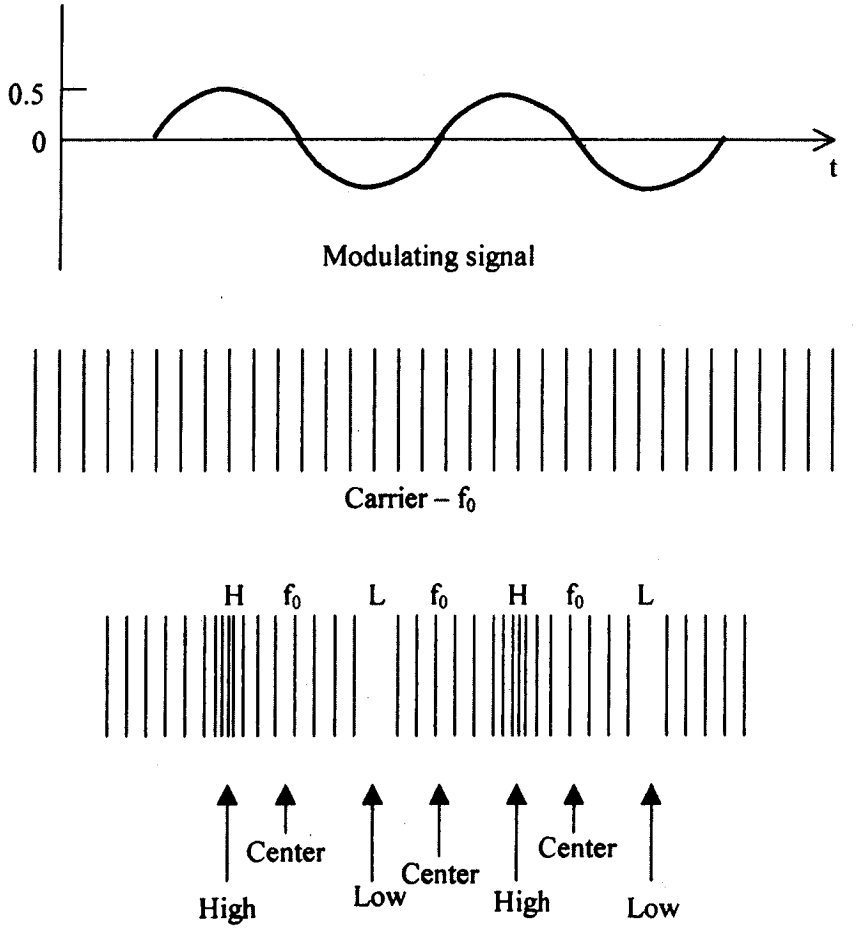


Fig 11.1

Mathematical expression for F.M. wave:

The unmodulated carrier is given by

$$e_c = E_C \cos 2\Pi f_c t \qquad \text{--------(11.1)}$$

The modulating signal frequency is given by

$$e_m = E_m \cos 2\Pi f_m t \qquad \text{--------(11.2)}$$

The modulated carrier frequency 'f' swings around the resting frequency f_0. Thus

$$F=f_C+kE_m \cos 2\Pi f_m t$$

$$f = f_C + \Delta f \cos 2\Pi f_m t \qquad \text{-------(11.3)}$$

Hence, equation for the frequency-modulated wave becomes

$$e = A \sin 2\Pi f t \qquad \text{-------(11.4)}$$

$$= A \sin \{2\Pi (f_0 + \Delta f .\cos 2\Pi f_m t) t\}$$

$$= A \sin \varphi t$$

$$\omega = \frac{d\varphi}{dt} \text{ or } \varphi = \int_0^t \omega dt$$

$$\therefore \quad e = A \sin \left(2\Pi f_0 t + \frac{\Delta f}{f_m} .\sin 2\Pi f_m t\right)$$

$$\therefore \quad f_{max} = f_C + kE_{m\,max}$$

$$\therefore \quad F_{min} = f_C - kE_{m\,max}$$

$$\therefore \quad \text{The modulation index } \beta = \frac{\Delta f}{f_m}$$

The equation for the frequency-modulated wave is given by

$$e = E_C \cos (2\Pi f_C t + \beta \sin 2\Pi f_m t)$$

$$e = E_C \cos(\omega_C t + m_f \sin \omega_m t) \quad \text{since } \omega = 2\Pi f$$

$$e = E_C \{\cos(\omega_0 t) \cos(m_f \cos\omega_m t) - \sin(\omega_C t) \sin(m_f \cos\omega_m t)\}$$

The $\cos(m_f \cos\omega_m t)$ and $\sin(m_f \cos\omega_m t)$ terms have to be expanded into infinite trigonometric series involving sine and cosine terms of harmonics of ω_m. When the relevant series are substituted in Eq.(11.4) , it can be shown that an FM wave comprises of an infinite number of side frequencies on both sides of the carrier frequency. The frequencies of these components are $f_c + f_m$, $f_c + 2f_m$, $f_c + 3f_m$, etc. The amplitudes of these components depend on the modulation index. The amplitudes are negligible when the separation between the carrier frequency and the side-band frequencies becomes sufficiently large. Therefore, in practice only a limited number of side frequency pairs are present. Also, as in AM the information is carried by side-frequency components. Hence the bandwidth needed for transmission or reception in case of FM is $2nf_m$ where n is the number of pairs of side frequencies. The total power in an FM wave remains constant and does not depend on the depth of modulation.

Thus, analysis of FM wave shows that unlike the AM wave, which has two side frequencies for each modulating frequency, it has an infinite number of side frequencies. However, it can be shown that even though the modulating frequency changes from 0.1 to 10kHz, or by a factor 100:1, the bandwidth occupied by the spectrum alters very little, from 140kHz to 170kHz

GENERATION OF F.M. WAVES

The methods used for FM generation can be grouped into two types. They are

(i) Direct method (ii) Indirect method

Direct method: In this method, the carrier frequency is directly modulated or varies in accordance with the input modulating signal such as (a) reactance modulator and (b) varactor diode.

Indirect method: The modulating signal is first integrated and then allowed to phase modulate a carrier. It is called indirect method because phase modulator is used for frequency modulation.

REACTANCE MODULATOR

In frequency modulation, the frequency deviation must be made proportional to the amplitude of the modulating signal. In the earlier methods, it was done by varying capacitance or inductance in the oscillator tuned circuits. A more modern technique is to insert a reactance circuit across the tuned oscillator circuit. In general series RC and RL circuits are used as reactance circuits. Phase technique can be used for the determination whether the particular circuit acts as capacitive or inductive. Fig.11.2 shows a typical reactance modulator.

Here RF oscillator is connected to produce carrier waves. The capacitance C is chosen so that its reactance at the oscillator frequency is much greater than R_2 in parallel with 'R_1'. Thus the current flowing through 'C' leads the voltage applied between C and ground by 90^0. The base current therefore leads the carrier voltage by 90^0. The collector current is in phase with the base current and therefore in phase with the current which passes through 'C'. The total current is leading the carrier voltage by 90^0. Thus the entire circuit appears as a capacitor.

The effective or equivalent capacitance of the reactance modulator is given by

$$C_{eq} = \frac{h_{fe} R_2 C}{h_{ie} + R_2} \qquad \text{---------- (11.5)}$$

The audio signal varies the operating point, which varies h_{fe} of the transistor, and thus the equivalent capacitance of the transistor reactor modulator according to the Eq.(11.5).

The effective capacitance C_{eq} is controlled by h_{fe}. Then the oscillator frequency across the tuned circuit

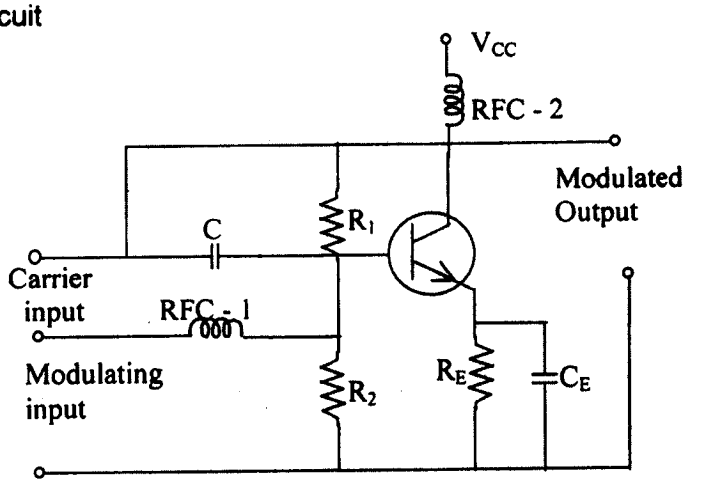


Fig 11.2 Transistor reactance FM Modulator

$$f = \frac{1}{2\pi\sqrt{L(C+Ceq)}} \qquad \text{---------- (11.6)}$$

where L = Inductance and C = capacitance

COMPARISON OF AM AND FM

TABLE 11.1

AMPLITUDE MODULATION	FREQUENCY MODULATION
The amplitude of AM signal varies depending on modulation index	The amplitude of FM signal is constant and independent of depth of modulation
Band width requirement is small compared to FM.	Bandwidth of FM is nearly 15 times that of AM
Transmitters are simple and less costly.	Transmitters are complex and expensive.
Area of reception is large.	Area of reception is small since it is limited to line of sight.
It is very noisy when compared to FM.	Noise can be easily minimized. Amplitude variations do not carry information and hence noise can be easily eliminated by using a limiter.
Most of the power contained in the AM carrier is not useful.	Full transmitted power is useful.

F.M. DETECTION

We know that an F.M. signal contains information in the form of frequency variation of the carrier signal. A simple method of converting frequency variations to voltage variations depends on the principle that reactance of the inductor or capacitor varies with the frequency. Thus the amplitude of current in the inductor or capacitor varies with the frequency of FM signal. As the frequency variations of FM signal depend on the amplitude of the AF signal, the current variations in the inductor or capacitor correspond to the AF signal. These amplitude variations in current, when made to flow through a resistor they will produce corresponding voltage variations across the resistor. There are various types of circuits used for FM demodulations. They are Phase discriminator or frequency discriminator, Ratio detector and Quadrature Detector

A circuit that gives an output voltage whose amplitude is proportional to the frequency of the input signal can be used to decode or detect FM signals. Such circuits are called **Frequency Discriminators.**

Now, let us discuss in detail about the functioning of Foster-Seeley discriminator.

FOSTER - SEELEY DISCRIMINATOR

The phase shift between Primary and Secondary voltages of a tuned transformer is a function of frequency and the Foster-Seeley discriminator utilizes this frequency phase dependence for the recovery of the modulating signal. The following Fig.113 shows the basic arrangement for the Foster-Seeley discriminator.

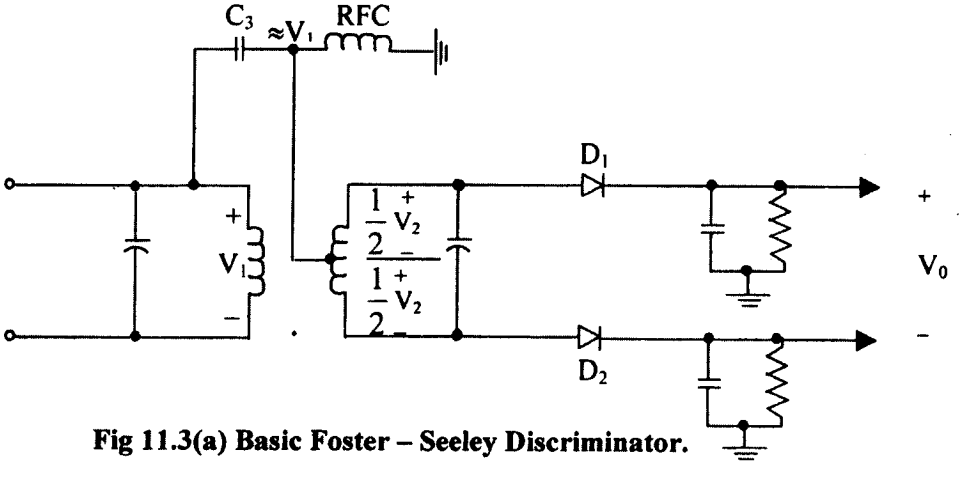


Fig 11.3(a) Basic Foster – Seeley Discriminator.

The primary voltage is tightly coupled through capacitor 'C_3' and the RFC to the center cap on the secondary. The coupling is tight enough that practically all the primary voltage appears between the centre top and ground.

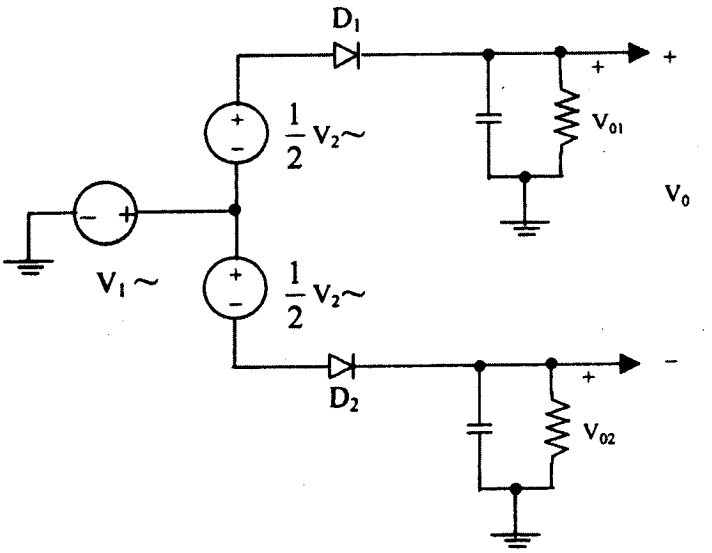


Fig 11.3(b) Voltage generator equivalent circuit

11.6 Electromagnetic spectrum

Elements of Electromagnetic theory

(a) Electromagnetic waves (EM –Waves) are generated by charged particles, e.g. electrons, in constant motion. The wave can propagate through free space, i.e., it does not need any medium for its propagation.

(b) A charged particle has one electric field (E – field).

(c) A change in the E – field generate a magnetic field (H – field)
A change in the H – field causes a further change in E – field.

(d) The E – and H – fields are perpendicular to each other and to the propagation direction.

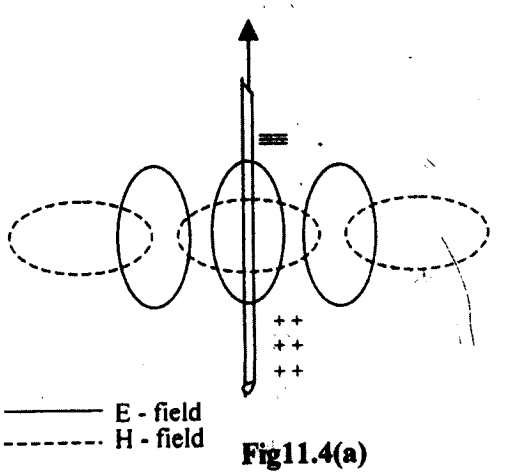


Fig11.4(a)

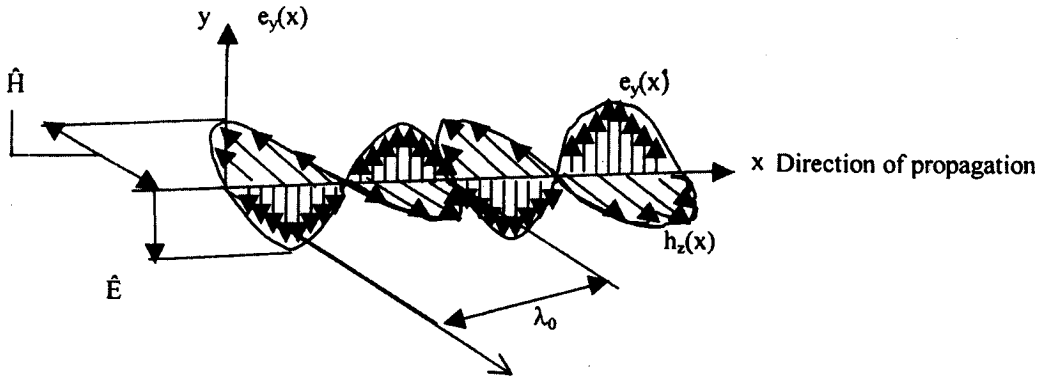


Fig 11.4(b)

Referring to Fig.11.4(b) the wavelength λ_0 is defined as the distance between two successive points in the propagation direction having the same phase. The EM-wave can also propagate in transmission lines, for instance in a co-axial cable or a wave-guide and is then associated with voltages and currents in the conductors. With suitable antenna arrangement, the wave will radiate into free space.

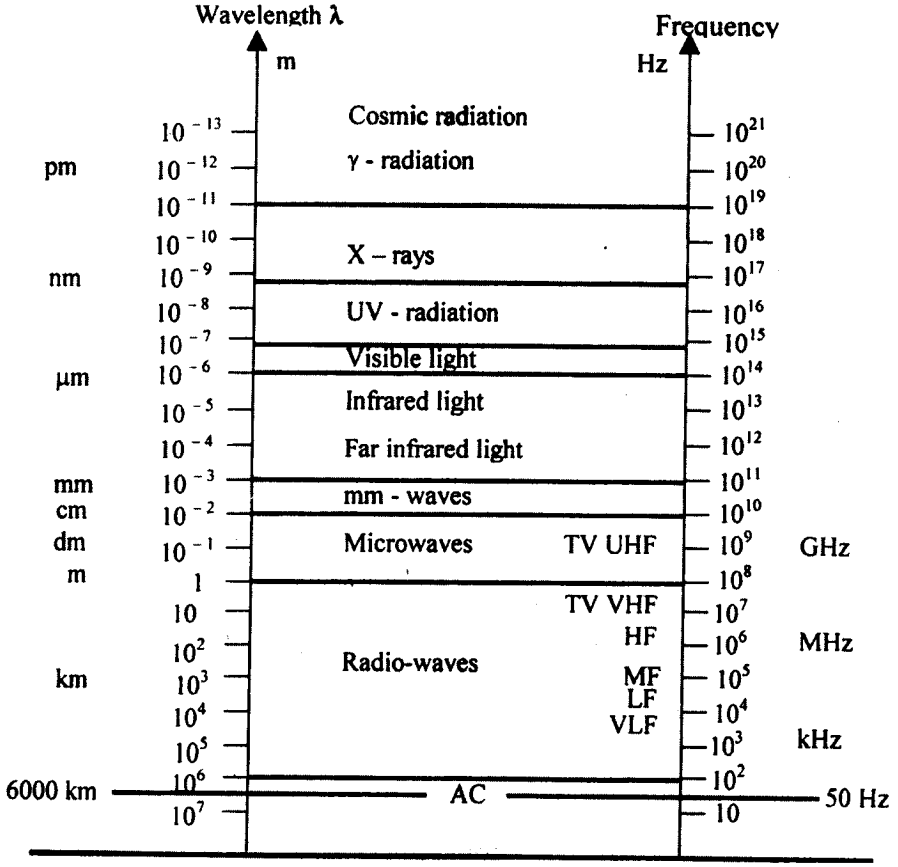


Table 11.2 Electromagnetic spectrum

Table 11.2 gives an idea about electromagnetic waves. Starting from very low frequency waves to γ-rays different types of waves come under this category. The waves below 1ookHz frequency behave more like electrical waves and need a conductor as a carrier. Above this frequency, and up to 300MHz, transmission lines with special properties are required. Up to this frequency we deal with voltages and currents to describe the signal motion. Above this frequency onwards, the signal behaves more like a wave and electric and magnetic fields are used to describe its propagation. The wavelength of these waves will be in centimeter region and are usually called microwaves. These require special transmission lines called wave guides. Above 300GHz the guided wave communication is not used and transmission through free space takes place. Recent trend in communication is to use visible light for communication and fibre optical guides are being used.

11.7 SUMMARY

1. In frequency modulation the frequency of the carrier wave is modulated as a function of the instantaneous value of the modulating signal. Un like amplitude modulation there will be infinite number of sideband in the spectrum of F.M wave. However, the bandwidth converges to 150kHz.
2. Several direct and indirect methods are available to produce FM waves.
3. F.M waves are detected by using Foster-Seeley discriminator circuit.

11.8 KEY TERMINOLOGY

Modulation: Process of combining low frequency signal with a high frequency radio wave (carrier wave).

Balanced modulator: A modulation circuit which cancels but the product term does not cancel.

Phase modulation: Just as amplitude and frequency are changed as a function of instantaneous value of modulating signal, phase can also be changed like that. The resulting modulation is called **Phase modulation**. At a given modulating frequency, the FM and PM waves look alike. The difference can be noticed only with change in modulating frequency. In a practical FM generator, both the types of modulations take place simultaneously and these two modulations put together are called **Angle Modulation.**

11.9 SELF – ASSESSMENT QUESTIONS

Long answer questions

1. Derive an expression for a Frequency modulated wave.

2. Discuss the principles involved in the production and detection of FM wave.
3. How can we detect an FM wave using Foster- Seeley discriminator? Explain with neat diagrams.

Short answer questions

1. Distinguish between Amplitude and frequency modulation.
2. Explain the working of reactance modulator
3. What are the advantages of frequency modulation?
4. Compare Frequency modulation and amplitude modulation

11.10 TEXT AND REFERENCE BOOKS

TEXT BOOKS

1. Integrated Electronics by Millman and Halkias
2. Electronic Communications by Kennedy
3. Basic Electronics and Linear Circuits - Bhargava etc

REFERENCE BOOKS

1. A text lab manual in Electronics by ZBAR (Tata Mc graw Hill)
2. Electronics fundamentals by JD Ryder
3. Modern Electronics Communications by Gray and Miller
4. Op. Amp and linear integrated Circuits by Ramakant Gayakwad
6. Electronic communications by Dennis Roddy and John Colllen (PHI).

RADIO BROADCASTING, RECEPTION AND MICROWAVES

OBJECTIVES OF THE LESSON

To identify the areas where Radio waves and Microwaves are applied, to understand the principles involved in radio broadcasting and reception , to understand the working of Super heterodyne receiver, to understand the properties of microwaves and to learn some applications.

STRUCTURE OF THE LESSON

12.1 INTRODUCTION

Radio communications use electromagnetic waves propagated through the earth's atmosphere or space to carry information over long distances without the use of wires. Radio waves with frequencies ranging from about 100 Hz to above 300GHz have been used for communications purposes. More recently, radiation in and near the visible range have also been used. Although the electric and magnetic fields exist simultaneously, in practice antennas are designed to work through one or other of these fields. To describe radio wave propagation, sinusoidal or co-sinusoidal variations will be assumed unless stated otherwise. In this lesson, we learn simple aspects of Radio wave and Microwave communications.

Table 12.1 Radio spectrum

Frequency band	Frequency range	Wave length range	Typical applications
Very Low Frequency (VLF)	10 – 30 kHz	30 –10km	Long – range direct communication
Low Frequency (LF)	30 – 300 kHz	10 – 1 km	Marine, navigational aids
Medium Frequency (MF)	300 kHz – 3 MHz	1 km-100m	Broadcasting, marine
High Frequency (HF)	3 – 30 MHz	100m –10m	All types of communication
Very High Frequency (VHF)	30–300 MHz	10 – 1m	TV, FM, radar, short –
Ultra – High Frequency (UHF)	300MHz –3 GHz	1m - 10cm	wave, air navigation
Super – High Frequency (SHF)	3 – 30 GHz	10 – 1cm	Radar, microwave relays, short distance communications Radar, radio relay, navigation satellite communication
Extremely High Frequency (EHF)	30 – 300GHz	1cm – 1mm	Experimental

12.2 RADIO WAVE PROPAGATION

Above 100 kHz, the radio waves prefer to travel without wires. In this process, they get scattered by buildings, hills and other obstacles. At higher frequencies, they travel more like a light rays. It means unless the receiving antenna must be in the line of sight of the transmitted ray. The earth's curvature affects the radio signal reception. For short wave communication, ionosphere is used as a reflector for radio waves. There are several ionic layers in the ionosphere and each has its cut-off frequency. The conditions in the ionosphere changes with day and night. It is called

Diurnal variation. Seasonal, cosmic ray incidence and sun spot activity also affect the propagation of radio waves through ionosphere. With the introduction of communication satellites, the present day TV, cellular and internet communication is taking place through satellite communication channels. Table 12.1 gives the use of various bands of radiofrequencies.

12.2.1 Propagation in electromagnetic waves in free space:-

Mode of propagation:- Consider first an average power P_T assumed to be radiated equally in all directions. This will spread out spherically as it moves away from the source. At distance 'd', the power density in the wave (power per unit area of wave front) will be

$$P_{di} = \frac{P_T}{4\pi d^2} \text{ watt / metre}^2 \qquad \text{---------- (12.1)}$$

This is so because $4\prod d^2$ is the surface area of the sphere of radius 'd', centered on the source.

P_{Di} = Isotropic Power density

It is known that all practical antennas have directional characteristics. The directivity gain is the ratio of actual power density along the main axis of radiation of the antenna to that which would be produced by an isotropic antenna at the same distance fed with the same input power.

Let G_T = Maximum directivity gain of the transmitting antenna

Then, the power density along the direction of maximum radiation will be,

$$P_D = P_{Di} \cdot G_T = \frac{P_T G_T}{4\pi d^2} \qquad \text{---------- (12.2)}$$

A receiving antenna can be positioned in such way that it collects, maximum power from the wave. When so positioned,

Let P_R = Power delivered by antenna to the load (receiver) under matched conditions.

$$\text{Then } P_R = P_D A_{eff} = \frac{P_T G_T}{4\pi d^2} \cdot A_{eff} \qquad \text{---------- (12.2.3)}$$

where A_{eff} = Affective area of the antenna

It can be shown that for any antenna;

$$\frac{A_{eff}}{G_R} = \frac{\lambda^2}{4\pi} \qquad \text{---------- (12.4)}$$

Here 'λ' is the wavelength of the wave being radiated.

Let G_R = Max. Directivity gain of the receiving antenna.

Then $\frac{P_R}{P_T} = G_T \cdot G_R \cdot \left(\frac{\lambda}{4\pi d}\right)^2$ ---------- (12.5)

This is the fundamental equation for free space transmission. Usually, it is expressed in terms of frequency 'f' in MHz, and distance 'd' in kilometers.

We know that $\lambda f = c$ ---------- (12.6)

Substituting Eq.(12.6) in Eq.(12.5), we get,

$$\frac{P_R}{P_T} = G_T \cdot G_R \frac{(0.57 \times 10^{-3})^2}{(df)^2}$$ ---------- (12.7)

By expressing power ratios in decibels, Eq.(12.7) becomes

$$\left(\frac{P_R}{P_T}\right)_{dB} = (G_T)_{dB} \cdot (G_R)_{dB} - (32.5 + 20 \log_{10} d + 20 \log_{10} f)$$ ---------- (12.8)

The third in parenthesis on RHS of Eq.(12.8) is the loss in dB, resulting from the spreading of the wave as its propagates outward from the source. It is the known as the **transmission path Loss L.**

Thus $L = (32.5 + 20 \log_{10} d + 20 \log_{10} f)$ dB ---------- (12.9)

Where 'd' is in Km and 'f' is in MHz

Then Eq.(12.8) becomes

$$\left(\frac{P_R}{P_T}\right)_{dB} = (G_T)_{dB} \cdot (G_R)_{dB} - (L)_{dB}$$ ---------- (12.10)

12.2.2 Factors involved in the propagating radio waves:-

There are a number of mechanisms by which radio waves may travel from a transmitting to a receiving antenna. The more important of these are designed by the terms.

(i) ground waves, (ii) Sky waves, and (iii) Space wave or tropospheric waves.

The ground wave (also sometimes called Surface wave) can exist when the transmitting and receiving antennas are close to the surface of the earth when

vertically polarized. This wave, supported at its lower edge by the presence of ground is of practical importance at broadcasting and lower frequencies.

The sky wave represents energy that reaches the receiving antenna as a result of a bending of the wave path introduced by ionization in the upper atmosphere. This ionized region is called the ionosphere. This begins about 80 Kms above the earth's surface and is useful for very long distance radio communication.

The space wave represents energy that travels from the transmitting to receiving antenna in the earth's Troposphere, Troposphere is the portion of the earth's atmosphere in the first ten miles adjacent to the earth's surface. A space wave consists of two components.

1. A ray that travels directly from transmitter to receiver and
2. A ray that reaches the receiver as a result of reflection from the surface of the earth.

Space wave energy may reach the receiver (i) as a result of reflection or refraction due to the variations in the electrical characteristics of the troposphere .and (ii) by diffraction around the curvature of the earth, hills etc.

Radio transmission at frequencies above about 30MHz is normally the range of space wave propagation.

Ex:- (a) Television , (b) F.M. (c) Radar use the frequencies in the rays g space wave propagation.

12.2.3 THE GROUND WAVE PROPAGATION

In ground wave propagation, the electromagnetic waves travel along the curved surface of the earth from transmitter to receiver. In fact, they depend on the earth for a portion of their transmitting medium.

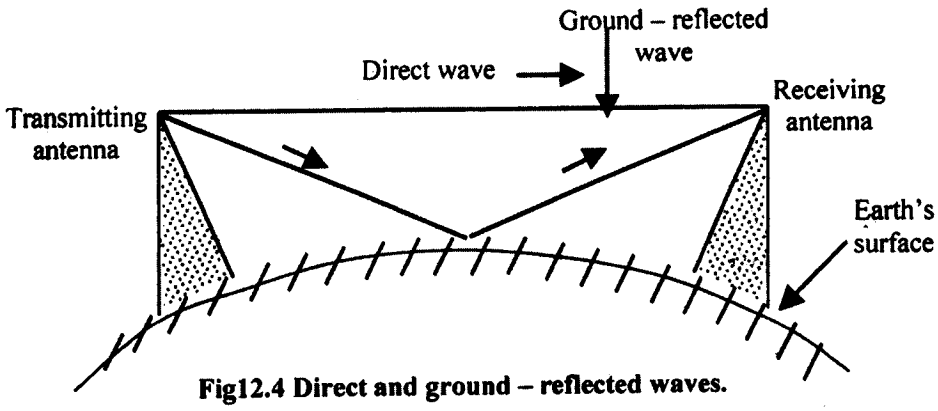


Fig12.4 Direct and ground – reflected waves.

These waves are influenced by the electrical characteristics of the ground, over which they travel. They are strongly absorbed by dry land. As the moisture and sea

water have greater conductivity, the ground waves are much less absorbed. The Table 12.1 shows the radio frequency spectrum.

The attenuation of ground waves depends on their direction of polarization also. These waves are always vertically polarized because the horizontal component of electric field is short circuited by the earth. But, the vertical component travels along the surface of the earth because of the electrical discontinuity between ground and atmosphere. As the wave travel along the ground, it induces charges in the ground. These charges travel along with the wave and have induced currents. As the earth has definite resistance the flow of induced current results in power loss, this causes absorption of energy from E.M. waves.

Ground waves get attenuated in another way also. As the wave travels over the ground, the wave front tilts, more and more towards the surface due to diffraction effects. This increases the horizontal component of electric field at the cost of vertical component. This causes greater attenuation.

The absorption of ground waves increases with frequency. Therefore, ground wave propagation is useful only at low frequencies.

Ground waves are useful in communication for the frequencies below 500KHz and over distances up to 1500 Kms. Amplitude modulated radio broadcasts in the medium frequency band are transmitted mainly via the ground wave. But at higher frequencies the ground waves are absorbed. So, these cannot be used beyond few Kilometers around the transmitter. Ground wave transmission makes the reception extremely reliable and not subject to the seasons atmospheric conditions.

12.2.4 SPACE OR TROPOSPHERIC WAVES

The space or tropospheric wave is that which travels from transmitting antenna to receiving antenna through the earth's troposphere. That is through the portion of the earth's atmosphere with in the first 15 Kms over the surface of the earth. The space wave is usually made up of two components. They are

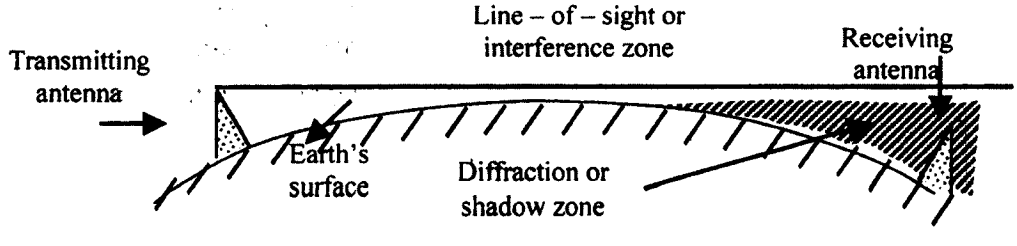


Fig 12.5 Interference and shadow zones.

a) The direct or line-of-sight wave from the transmitting to receiving antenna.

b) The ground reflected wave traveling from the transmitting to the receiving antenna after reflection from the ground. These two components are shown in the Fig.12.5

c) The phase of the ground reflected wave changes by 180^0 after reflection from the ground. The strength of the signal received at the receiving end depends on the phase relationship between the direct and reflected waves.

If the path length of the direct and reflected waves differ by $n\lambda$, where 'n' is an integer and 'λ' the wavelength, then the total path difference between the two waves becomes $(n + \frac{1}{2})\lambda$. Here, the additional path difference $\frac{\lambda}{2}$ is because of reflection. Therefore, the two waves reaching the receiving antenna will have opposite phases and will cancel each other. If the path lengths of the direct and reflected components differ by, half-integral multiple of λ the total path difference will become an integral multiple of 'λ'. Then the two waves arrive in phase and reinforce each other. Thus by varying the height of the receiving antenna, the path difference between the two waves can be changed. The signal strength can be increased or decreased. This phenomenon is referred to as ***selective fading.***

The space wave does not undergo continuous absorption by the surface of the earth. It can therefore cover large distances than the ground wave. The region beyond the line of sight is called **Diffraction zone** or **Shadow zone**. The signal in the shadow zone is also increased due to a phenomenon known as ***duct propagation.***

The region outside the shadow zone where the line of sight propagation is possible is called the ***interference zone.*** In this region the two waves interfere to give the resultant field.

12.2.5 RADIO HORIZON

The maximum distance over which the space wave can be transmitted is called the ***effective horizon*** *or* ***radio horizon.*** It is greater than the optical horizon. Optical horizon is the straight-line distance between the two points. The radio horizon of an antenna depends on its height above the ground. It is given by, an empirical relation,

$d_t = 4\sqrt{h_t}$ where

d_t = Radio horizon of the transmitting antenna of height h_t.

Similarly, $d_r = 4\sqrt{h_r}$ where

d_r = Radio horizon of the receiving antenna of height 'h_r'

Therefore the maximum limiting distance between the two antennas = $d = d_t + d_r$

$= 4 (\sqrt{h_t} + \sqrt{h_r})$.

12.2.6 SKY WAVES

A sky wave is that which arrives at a receiving antenna after reflection from the ionized layers of the earth's upper atmosphere known as ionosphere.

The short wave communication around the world takes place by the sky waves, via successive reflections at the earth's surface and the ionosphere. The transmission by this mode of propagation depends on the properties of ionosphere. It is subject to fading with seasons, day and night and atmospheric conditions. It is the primary means of propagation over a wide range of frequencies extending up to about 30MHz.

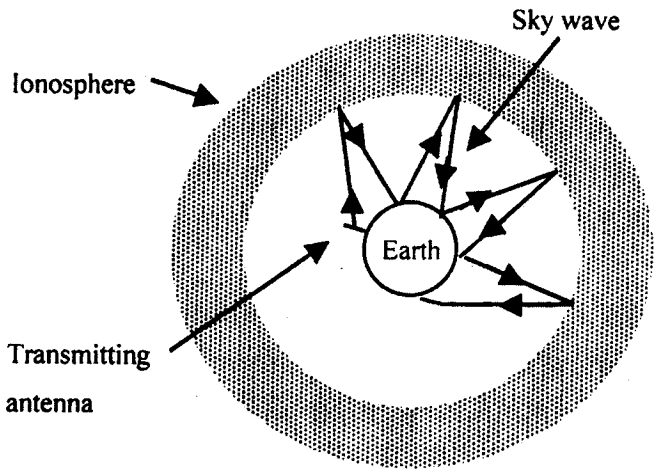


Fig.12.6 Around the world communication by means of sky waves.

TERMS RELATED TO SKY WAVE COMMUNICATION

I) SKIP DISTANCE

Let a radio wave with a frequency higher than the critical frequency of layer be incident on it at various angles. The situation is illustrated in the Fig.12.7

It is found from the figure that as the angle of incidence decreases, the distance between transmitting and receiving points on the earth's surface diminishes and then increases. Compared to the other rays, ray 2 moves through a longer horizontal distance in the layer. For the ray to be received on the earth's surface, there is a minimum distance between the transmitting and receiving points for a given frequency. This minimum distance is known as **skip distance.**

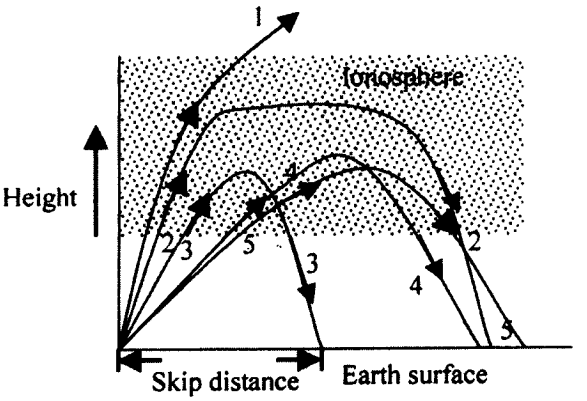


Fig.12.7 Ray trajectories in the ionosphere for different angels of incidence

In the above figure, ray 3 is received at skip distance. Skip distance for a given frequency increases with increasing height of the layer. The skip distance is minimum at noon and increases at other times.

II) MAXIMUM USABLE FREQUENCY

The frequency of radio wave for which a given distance on the earth's surface is equal to the skip distance is called as **Maximum Usable Frequency (MUF).** The MUF has ***diurnal*** variation. It is maximum at noon and falls on either side of the noon hour. For sky wave communication between two points the optimum frequency of the wave is taken to be about 85% of the MUF.

III) SINGLE AND MULTI HOP TRANSMISSIONS

If a radio wave launched by a transmitter arrives at the receiver after its reflection from the ionosphere the transmission is referred to as a single hop transmission and the path of the wave is called ***single hop path.***

Transmission using multiple reflections at the ionosphere is referred to as multi-hop transmission.

IV) FADING

The fluctuation of the received signal existing over short period of the order of a minute or less is called as ***fading.*** Fading is an undesirable phenomenon in any communication system. It is one of the problems of radio wave communication using ionosphere reflection.

12.3 PRINCIPLES OF RADIO BROADCASTING AND RECEPTION:

Radio communication is a very popular way of communicating information. The radio waves are electromagnetic and are produced due to the escape of electrical energy into free space. They have a frequency range of few Hertz to 10^9 Hertz. They travel with the velocity of light and consist of electric and magnetic fields

at right angles to each other. In a simple form of basic elements of radio communication are shown in Fig.12.8a.

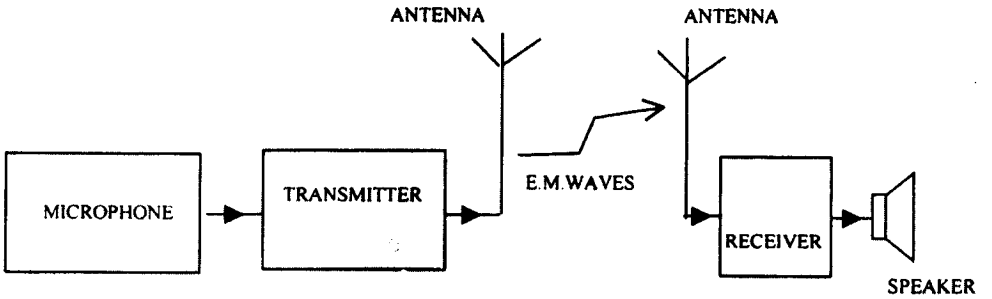


Fig.12.8a Wireless Communication system

Speech or music, usually called ***audio information*** that is mechanical in nature and a microphone converts into electrical form. These electrical signals are weak. So these are subjected to amplification and modulation process before being transmitted. The high power modulated carrier generated by the transmitter is radiated into space by means of a transmitting antenna. The transmitted radio waves travel through free space and reach a receiving antenna. A receiving antenna receives these signals and feeds them to a chain of amplifiers as the received signals will be very very weak. After sufficient amplification, the modulated wave is detected to extract audio information from it. The detected audio signal is again fed to a series of voltage and power amplifiers before giving it to a speaker. Speaker is a transducer that converts electrical energy into sound energy thereby reproducing the transmitted information. By tuning the receiving system to the frequency of the transmitting system we can hear the transmitted audio. With minor modifications, the same process is used for receiving video signals also.

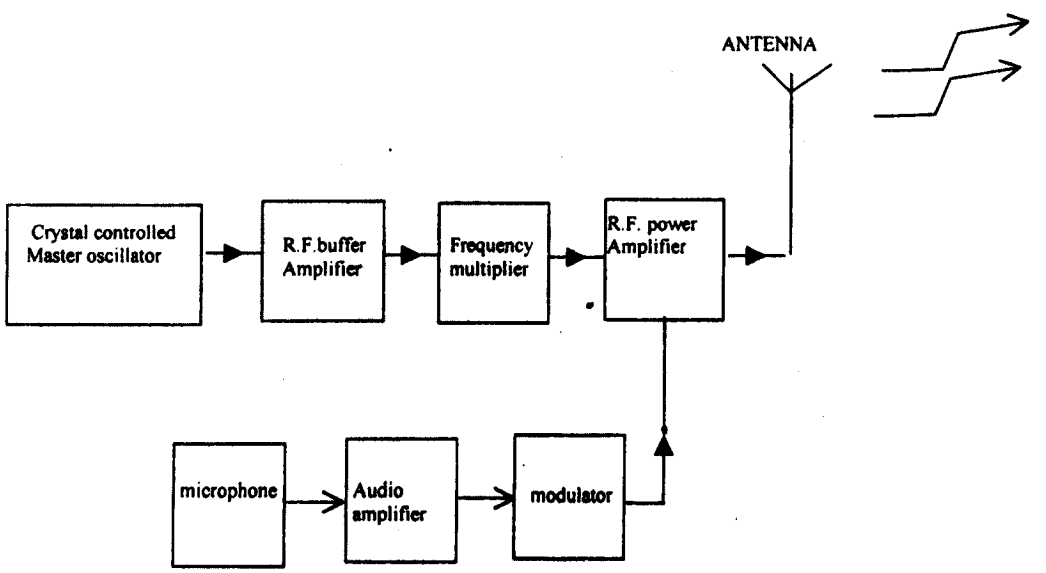


Fig.12.8b Radio frequency transmitter

Transmitter: The block diagram of an AM transmitter is shown in Fig 12.8b. The individual blocks are described as follows:

1) Crystal controlled master oscillator: It operates the transmitter at the desired frequency. Since the power output of this oscillator is small it subjected to amplification.
2) R.F. Buffer amplifier: It isolates the master oscillator from the succeeding stages so that loading effect does not take place.
3) Frequency multiplier. It is used to multiply the crystal oscillator frequency to the required value.

The other items are already known to us and so are not discussed here.

Receiver:

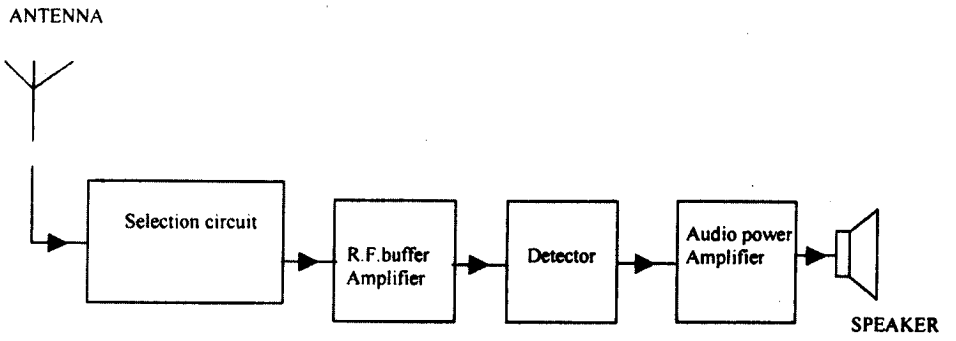


Fig 12.8c Receiver

The individual blocks are described below:

1) **Selection circuit:**

   It is a series resonant circuit. By varying the capacitance of the circuit, desired carrier is selected and the other carriers that may be coming from the antenna are rejected.

The other units were already discussed by us and so are not discussed here.

12.4 Super heterodyne receiver:

The shortcomings of a radio receiver were overcome by the invention of super heterodyne receiver.

Principle of super - heterodyning: In this type of radio receiver the selected radio frequency is converted to a fixed lower value called intermediate frequency (IF). This is achieved by a special electronic circuit called mixer circuit. There is a local oscillator in the radio receiver itself. This oscillator produces high frequency waves. The selected radio frequency is mixed with the high frequency wave by the mixer circuit. In this process, beats are produced and the mixer produces a frequency equal to the difference between local oscillator and radio wave frequency. The circuit is so designed that oscillator always produces a frequency 455KHz above the

selected & R.F. Therefore the mixer always produces an IF of 455KHz regardless of the station to which the receiver is tuned. The production of mixed IF is the salient feature of a super heterodyne circuit. At this fixed IF, the amplifier circuit operates with a maximum stability, selectivity and sensitivity. As the conversion of incoming RF to IF is achieved by heterodyning or beating the local oscillator against R.F., therefore this circuit is called super heterodyne circuit.

Stages of super heterodyne receiver

The following Fig.12.9 shows the block diagram of a super hetero dyne receiver. It consists of 5 stages. There are 1) RF amplifier stage 2) Mixer stage 3) IF amplifier stage 4) Detector stage 5)AF amplifier stage

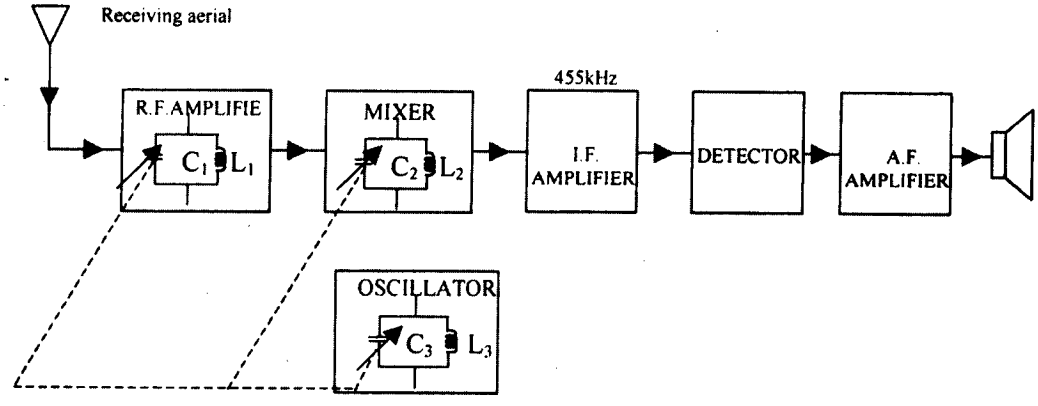


Fig 12.9

RF amplifier stage: This stage uses a tuned parallel circuit L_1 C_1 with a variable capacitor 'C_1'. The radio waves from various broadcasting stations are intercepted by the receiving aerial and are coupled to this stage. This stage selects the desired radio wave and raises the strength of the wave to the desired level.

Mixer stage: The amplified output of RF amplifier is fed to the mixer stage. Hence it is combined with the output of local oscillator. The two frequencies beat together and produce an intermediate frequency (IF).

IF = Oscillator frequency – Radio frequency.

= 455 KHz (always)

IF amplifier stage: The output of mixer is always 455 KHz and is fed to fixed tuned IF amplifiers. These amplifiers are tuned to one frequency and give nice amplification.

Detector stage: The output from the last IF amplifier stage is coupled to the input of the detector stage. Here, the audio signal is extracted from the input.

AM amplifier stage: The audio signal output of the detector stage is fed to multistage audio amplifier. Here, the signal is amplified until it is sufficiently strong to

drive the speaker. The speaker converts the audio signal into sound waves corresponding to the original sound of the broadcasting station.

Advantages of super heterodyne circuit

The super heterodyne principle has the following advantages.

High RF Amplification, Improved selectivity and low cost.

12.5 MICROWAVES

Microwaves are a part of the electromagnetic spectrum, i.e., radio waves, in the frequency band between 300MHz and 30 GHz

Referring to Table 12.1, the frequency of microwaves is placed in between radio frequencies and light wave frequencies. From this, we can conclude that terms and theories from both these fields are used to describe microwaves. Further, the wavelength is in the same magnitude as the physical dimensions of the components. This compares with alternating currents, where a wavelength is 6000Km

Properties of microwaves:

1, Microwaves exhibit all the properties of optical waves like reflection, refraction, diffraction, and polarization.

2. Since microwaves have very small wave length, these waves are not reflected by the ionosphere. There are some bands of frequencies. Microwaves whose frequencies fall in this region propagate into space with out attenuation. These bands are called microwave windows.

3. Microwaves are absorbed by some molecules by resonance phenomena.

4. Microwaves produce thermal effects like any other form of energy.

12.6 APPLICATIONS OF MICROWAVES

There are a number of areas where microwave techniques are used for practical applications. Some of them are

i) In aviations surveillance and navigation, microwave radars systems are being used. In meteorology, radars are used in weather forecasting. Shipyards and airports use radar for navigation and to pilot traffic.

ii) Telecommunications use microwaves to convey telephone and TV signals between continents via satellites and modern communications systems use microwave links.

iii) Microwave radiation is used for heating materials in industrial applications and in food processing.

iv) Radio astronomy reveals existence of distant galaxies with microwaves and space-vehicles land and dock using microwave navigational aids.

v) Microwaves are used in measuring moisture contents in food, paper etc.

vi) Automatic door openers and bugler alarms often use microwaves.

vii) Microwaves are also used for speed control, short distance measurement, short distance directed communications e.g, in dirty and smoky areas.

viii) Microwaves have also scientific and medical applications.

12.7 SUMMARY

There are three modes of propagation for the radio waves.

1) Ground wave or surface wave, 2) Tropospheric wave or space wave, 3) sky wave. The choice of mode of propagation depends on the frequency of radio waves. Ground wave travels along the surface of the earth. So it can follow the earth curvature. It is vertically polarized. The attenuation of ground wave increases with frequency.

2) Space wave propagates through the earth's troposphere and consists of two components. 1) Direct or line of sight wave and the ground reflected wave. The strength of a signal at a point depends on the interference of the two components.

A sky wave is that which arrives at a receiving antenna after reflection from the ionosphere. It is used for short wave communication.

12.8 KEY TERMINOLOGY

Microwave region: That portion of the electromagnetic spectrum lying between the far infrared and conventional RF portion. Commonly regarded as extending from 1,000 megacycles to 300,000 megacycles.

Cut-off frequency: The lowest frequency at which loss-less waveguide will propagate energy in some particular mode without attenuation.

Attenuation: Decrease in magnitude of current, voltage, or power of a signal in transmission between points.

Attenuation constant: For a traveling plane wave of a given frequency, the rate of exponential decrease of the amplitude of a field component in the direction of propagation. Expressed in Neperes or db per unit length.

1) Vidicon 2) Orthicon 3) interlaced scanning 4) raster 5) Troposphere 6) Ionosphere 7) Sky wave 8) Ground wave 9) Skip distance 10) Radio horizon

12.9 SELF ASSESSMENT QUESTIONS

Long answer questions

1. Give the block diagram of a super heterodyne receiver and explain the function of each block.
2. . Explain the principle of super heterodyne reception.
3. Explain the principle of radio transmission and reception.

4. Draw the block diagram of a super heterodyne receiver and explain the function of each block.
5. Name the various regions in the electromagnetic spectrum and mention the use of various frequency regions.
6. Describe the AM detector section in a super heterodyne receiver.

Short answer questions

1. Explain the principle of super heterodyne reception.
2. Mention the properties of microwaves
3. Mention the applications of microwaves.
4. Draw the block diagram of radio transmitter.
5. Discuss the effect of earth curvature on space wave propagation.
6. What is meant by fading
7. Describe Automatic volume control in a super heterodyne receiver.

12.10 TEXT AND REFERENCE BOOKS

1. Microwave Engineering – Rajeswari Chatterjee
   Affiliated East – West Press Pvt. Ltd. – New Delhi.
2. Microwave Principles – Herbert. J. Reich
   Affiliated East – West Press Pvt. Ltd. – New Delhi.
3. Microwave Propagation and Techniques – D.C. Sarkar – S. Chand & Company Ltd.
4. Foundation for Microwave Engineering – Collin, R.E., Mc Graw – Hill, New York.

UNIT IV LESSON 13

NUMBER SYSTEMS

OBJECTIVES OF THE LESSON: To learn about various binary related number systems.

STRUCTURE OF THE LESSON

13.1 INTRODUCTION

A computer understands information composed of only zeros and ones. Therefore, instructions and data are processed by the computer in the from of zeros and ones. We are familiar with decimal number system in which digits are 0,1,2,3,4,5,6,7,8, and 9. The decimal number system is convenient for the programmer. The computer uses binary digits for its operation. In the binary system there are only two digits 0 and 1. The programmer feeds instructions and data in alphabets and decimal digits. But, for the operation of the computer these are converted to binary bits. This lesson deals with the conversion of binary numbers to

decimal numbers and vice versa. It also deals with hexadecimal and octal systems. Computer circuitry is usually designed to process hexadecimal and octal numbers.

13.2 DECIMAL NUMBER SYSTEM

We use decimal number system in everyday work. There are ten digits 0 to 9. The base of the decimal number system is 10. The following example will explain the base and value of the digit of a decimal number.

Example:

$$6784 = 6000+700+80+4$$
$$= 6 \times 10^3 + 7 \times 10^2 + 8 \times 10^1 + 4 \times 10^0$$

The value of each digit depends on its position in the number as described below :

The value of the 1st digit of the number from the right side

$$= 1^{st} \text{ digit} \times 10^0$$

The value of the 2_{nd} digit of the number from the right side

$$= 2_{nd} \text{ digit} \times 10^1$$

The value of the 3_{rd} digit of the number from the right side

$$= 3_{rd} \text{ digit}$$

The value of the 4^{th} digit of the number from the right side

$$= 4^{th} \text{ digit} \times 10^0$$

The value of the n^{th} digit of the number from the right side

$$= n^{th} \text{ digit} \times 10^{n-1} = n^{th} \text{ digit} \times (\text{base})^{n-1}.$$

13.3 BINARY NUMBER SYSTEM

It the binary number systems there are only two digits 0 and 1. The binary digits are called **bits**. The base of the binary number system is 2. In the decimal system, there is no difficulty in representing numbers up to 9. For ten there is no symbol or digit and hence 10 is written. Again, after 99 we have to write 100. Similarly, in binary system zero is represented by 0 and one by 1. After this, there is no digit for two. Therefore, two is written as 10 and three as 11. For four, we have to write 100. In this way, we proceed further. Thus we see that a binary number becomes very long and cumbersome. The following example will illustrate the base and weight of each digit in binary number.

Example:

$$1110 = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$$
$$= 8 + 4 + 2 + 0 = 14 \text{(decimal number)}$$

The weight of each bit of a number depends on its position as described below :

The value of the 1st bit of the number from the right side

$$= 1^{st} \text{ bit} \times 2^0$$

The value of the 2_{nd} bit of the number from the right side

$= 2_{nd}$ bit x 2^1

The value of the 3_{rd} bit of the number from the right side

$=3_{rd}$ bit x 2^2

The value of the 4^{th} bit of the number from the right side

$=4^{th}$ bit x10^3

The value of the n^{th} bit of the number from the right side

$= n^{th}$ bit x 2^{n-1}= n^{th} digit x $(base)^{n-1}$.

Thus we see that rules for decimal and binary numbers are exactly same. The value of a digit in number depends on the base and its relative position in the number. Table shows the binary representation of decimal numbers

Decimal number	Binary number	Decimal number	Binary number
0	0	9	1001
1	1	10	1010
2	10	11	1011
3	11	12	1100
4	100	13	1101
5	101	14	1110
6	110	15	1111
7	111	16	10000
8	1000		

13.3.1 CONVERSION OF BINARY NUMBER TO DECIMAL NUMBER

For the evaluation of a binary number we must know the relative position of each bit. For this purpose we count the position of binary bits from the right side as shown below:

Binary number = 1 1 1 0 1

Bit position = 5 4 3 2 1

The value of the $n^{th} = n^{th}$ bit x 2^{n-1}

The values of all bits are added to give the value of the binary number.

11101(binary number) = 1 x2^4 + 1 x 2^3 + 1 x 2^2 + 0 x 2^1+ 1 x 2^0

= 16 + 8 + 4 + 0 + 1 = 213(decimal number)

In the decimal number system the 1^{st} place from the right side is for 1, 2_{nd} for 10s, 3_{rd} for 100s, 4^{th} for 1000s, and so on. Similarly, in the binary number system the 1^{st} place is for 1, 2_{nd} for 2, 3_{rd} for 4, 4^{th} for 8, 5^{th} for 16 and so on. Binary numbers are

long, cumbersome and difficult to understand for us, but for computers they are simple. 0 and 1 are represented in terms of OFF (0) and ON (1) or pulse and no pulse (0) or LOW (0) and HIGH (1).

CONVERSION OF DECIMAL NUMBER TO BINARY NUMBER

We have seen that a binary number weight of bits from the right side are 1,2,4,8,16 and so on. This concept can be utilized for the conversion of a decimal number to binary number. A procedure is to be developed to examine which multiples of 2 are present in the decimal number. For example, 12 (decimal number) has one 8 and one 4. It has no 2 and 1. In other words, it has zero 2 and zero 1. Its binary equivalent is 1100. Based on this concept for decimal to binary conversion, the decimal number is divided by 2 successively. At each stage, the quotient and remainder are noted down. The quotient of one stage is divided by 2 at the next stage. The procedure is repeated till the quotient becomes zero. If the remainder of the 1st stage is R_1, remainder of the 2nd stage is R_2, and so on, the binary number is given by

Binary Number = $R_i R_{i-1} R_{i-2} \ldots\ldots\ldots\ldots R_3, R_2, R_1$

Where R_i = remainder of the i_{th} stage.

The following examples will illustrate the conversion of decimal numbers to binary numbers:

Example 1: Find the binary equivalent of the decimal number 39.

	Quotient	Remainder	Remark
Divide 39 by 2	19	1(LSB)	There is one 1
Divide 19 by 2 (It is equivalent to division by 4)	9	1	There is one 2
Divide 9 by 2 (It is equivalent to division by 8)	4	1	There is one 4
Divide 4 by 2 (It is equivalent to division by 16)	2	0	There is zero 8
Divide 2 by 2 (It is equivalent to division by 16)	1	0	There is zero 16
Divide 1 by 2	0	1(MSB)	There is one 32

(It is equivalent to division by 32)

The binary number is 100111.

The last remainder is MSB and 1st remainder LSB.

Check : The decimal equivalent of the above binary number is given by

$100111 = 1 \times 2^5 + 0 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$

$= 32 + 0 + 0 + 4 + 2 + 1 = 39$ (decimal)

Example 2: Convert the decimal number 25 to its binary equivalent.

The division and remainder can be written in a simpler form as shown below:

2	25	remainder
2	12	1(LSB)
2	6	0
2	3	0
2	1	1
	0	1(MSB)

The Binary number = 11001.

Check : $11001 = 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$

$= 16 + 8 + 0 + 0 + 1 = 25$ (decimal).

The equivalent binary number is 11001. If there is a mixed number, for instance 25.7, first convert 25 into binary equivalent as above, and then proceed as follows to convert 0.7 into its binary equivalent:

Product	Fraction		Carry
$0.7 \times 2 = 1.4$	$= 0.4$	and a carry of	1
$0.4 \times 2 = 0.8$	$= 0.8$	" "	0
$0.8 \times 2 = 1.6$	$= 0.6$	"	1
$0.6 \times 2 = 1.2$	$= 0.2$	" "	1
$0.2 \times 2 = 0.4$	$= 0.4$	" "	0
$0.4 \times 2 = 0.8$	$=0.8$	" "	0
$0.8 \times 2 = 1.6$	$=0.6$	" "	1
$0.6 \times 2 = 1.2$	$=0.2$	" "	1

The equivalent binary number is 11001. 10110011. If necessary this process can be continued further where greater accuracy is desired.

Example 3: Conversion of 1010.101_2 into decimal

Binary Number is	1	0	1	0	.	1	0	1
Place values	2^3	2^2	2^1	2^0		2^{-1}	2^{-2}	2^{-3}

Hence decimal equivalent of the given binary number is

$1x2^3 + 0x2^2 + 1x2^1 + 0x2^0 + 1x2^{-1} + 0x2^{-2} + 1x2^{-3}$

$= 8 + 0 + 2 + 0 + 0.5 + 0 + 0.125$

$= 10.625_{10}$.

13.3.2 BINARY ADDITION AND SUBTRACTION (1s and 2s COMPLIMENTS METHODS):

Table.2 shows the rules for binary addition. When 1 is added to 1, the sum is 10 (binary) = 2(decimal).

Table.2 Binary Addition Table

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	10

Example 1:

1	1	0	1	(13 decimal)
+0	0	0	1	(+1 decimal)
1	1	1	0	(14 decimal)

When 1 is added to 1, there is a carry = 1. This carry is added to the sum of the adjacent bits.

Example 2:

0	0	1	1	(3 decimal)
+0	1	1	1	(+7 decimal)
1	0	1	0	(10 decimal)

BINARY SUBTRACTION

The following examples will illustrate binary subtraction:

Table 2 Binary Subtraction Table

Minuend A	Subtrahend B	Difference D	Borrow B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The following examples will illustrate binary subtraction:

Example 1:

Borrow ↓

1	1	0	1	(13 decimal)
-0	0	1	1	(-3 decimal)
1	0	1	0	(10 decimal)

When 1 is subtracted from 0, there is a borrow from the adjacent bit.

Example 2:

1	1	0	1	(13 decimal)
-0	1	1	0	(-6 decimal)
0	1	1	1	(7 decimal)

Conversion of a decimal number to Hexa decimal

For converting a decimal number into its equivalent Hexa number, the following steps are followed.

- The integer part of the decimal number is progressively divided by 16 and the remainders after each division are noted until the quotient becomes zero.
- The remainders are written in the reverse order.
- For the conversion of fractional part, the fraction is progressively multiplied by 16 and the carry is recorded until the fractional part of the multiplication becomes zero.
- Now the carries are noted in the forward order.

Ex: Conversion of 685.15_{10} into Binary,

Integer part of given number is 685

16	685
16	42 ----D
16	2 ---- A
16	0 -----2

↑

Hence the Hexa equivalent to the integer part of the given decimal number is $2AD_{16}$

Fractional part of given number is 0.15.

Fraction	Fraction X 16	Carry
0.15	2.40	2
0.40	6.40	6
0.40	6.40	6

Hence Hexa equivalent to the fraction part of given decimal number is 0.266_{16}

$\therefore$ Hexa equivalent of given decimal number is $(2AD.266\text{---})_{16}$.

1'S COMPLEMENT TO A BINARY NUMBER

1's complement to a binary number can be obtained by complementing all its bits (i.e) replacing 0's by 1's vice versa.

Ex: - 1's complement of 1010110_2 is ----

Binary Number is	1	0	1	0	1	1	0
1' s complement is	0	1	0	1	0	0	1

2'S COMPLEMENT TO A BINARY NUMBER

2's complement to a binary number can be obtained by adding 1 to the 1's complement of the binary number.

Ex: 2's complement of 1010111_2 is ----

Binary Number is	1	0	1	0	1	1	1
1' s complement is	0	1	0	1	0	0	0

2's complement to the given binary = 1's complement + 1

$= (0101000)_2 + 1$

$= 0101001_2$

2'S COMPLIMENT METHOD OF SUBTRACTION

The following steps are followed for subtraction for binary numbers using 2's complement method.

- Compute 2's complement to the minued.
- Add this 2's complement to the minued.
- If carry exists, remove it and the remaining sum gives the result. In this case the result is positive.

❖ If there is no carry, again compute 2's complement to the sum in step2 and put a negative sign. In this case result is negative.

Ex: Subtract 101101_2 from 1110010_2.

1's complement of subtrahend ——— 1 0 1 0 0 1 0
+1

2's complement of subtrahend ——— 1 0 1 0 0 1 1
Minued ——— 1 1 1 0 0 1 0 (Add)

Sum ——— 1 1 0 0 0 1 0 1
Ignoring the carry result is 1000101_2
$\therefore (1110010)_2 - (101101)_2 = 1000101_2$

Ex: Subtract 1111_2 from 1000_2.

1's complement of subtrahend ——— 0 0 0 0
+1

2's complement of subtrahend ——— 0 0 0 1
Minued ——— 1 0 0 0 (Add)

Sum ——— 1 0 0 1

Since carry doesn't exist,
1's complement of sum ——— 0 1 1 0
+1

2's complement of sum ——— 0 1 1 1

$\therefore (1000)_2 - (1111)_2 = -111_2$.

13.4 HEXADECIMAL NUMBER SYSTEM

The hexadecimal number system is widely used with computers and other digital systems. The base of is 16. The digits from 0 to 9 are same as those of the decimal number system 16. In the hexadecimal system 10 is represented by A, 11 by B, 12 by C, 13 by D, 14 by E, and 15 by F. The decimal number 16 is represented by 10 in the hexadecimal system; 17 by 11 ; 18 by 12; 32 by 20; 33 by 21 and so on.

A hexadecimal digit is represented by four binary bits. For example, 6 is represented by 0110, B is represented by 1011 and F is represented by1111. If there are two or more than two digits in a hexadecimal number, each hexadecimal digit is represented by four binary bits. For example, 98 is represented by 1001 1000; 5C by 01011100; 3AFB by 0011 1010 1111 1011.

Decimal Number	Hexa Decimal Number	Binary equivalent of Hexa Decimal Number
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010

The hexadecimal system utilizes the full capacity of four binary bits. The BCD system does not utilize the full capacity of four binary bits which represent a decimal digit. In the hexadecimal system an 8-bit word can represent up to 11111111 or 255 (decimal) whereas in BCD only up to 10011001 or 99 (decimal). Thus the hardware cost in the hexadecimal system is reduced. The BCD system has the advantage of simplicity in getting the output in the decimal system.

Example: Convert 110111100010 to Hexadecimal

Decimal Number	Hexa Decimal Number	Binary equivalent of Hexa Decimal Number
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111
16	10	0001 0000
17	11	0001 0001
20	14	0001 0100
21	15	0001 0101
32	20	0010 0000
100	64	0110 0100

We rewrite the number as 1101 1110 0010. We separated the number into three four-bit groups keeping their positional value as it is. Now we replace each group its hexadecimal equivalent following the conversion given in Table. The resulting hexadecimal number is $DE2_H$

13.4.1 Conversion of a hexadecimal number to decimal:

The decimal equivalent of a Hexa number can be obtained as a sum of various Hexa digits multiplied by their respective place values.

EXAMPLE 1: - Conversion of $15BC.251_8$ into decimal

Hexa Number is 1	1	5	B	C	2	5	
Place values	16^3	16^2	16^1	16^0	16^{-1}	16^{-2}	16^{-3}

Hence decimal equivalent of the given Hexa number is

$1X16^3 + 5X16^2 + BX16^1 + CX16^0 + 2X16^{-1} + 5X16^{-2} + 1X16^{-3}$

$= 40136 + 1280 + 176 + 12 + 0.125 + 0.01135 + 0.00024$

$= 5564.14474_{10}$.

EXAMPLE 2

Convert the hexadecimal number 5A9 to its decimal equivalent.

9 is the 1st digit from right; its weight is 9×16^0

A is the 2nd digit from right; its weight is 13×16^1

5 is the 3rd digit from right; its weight is 5×16^2

$5A9 \text{ (hex)} = 5 \times 16^2 + A \times 16^1 + 9 \times 16^0$

$= 5 \times 256 + 10 \times 16 + 9$

$= 1280 + 160 + 9 = 1449$ (decimal).

EXAMPLE 3

Convert the hexadecimal number 5A9 to its binary equivalent.

We replace the individual hexadecimal number by its binary equivalent and place them in their respective positions.

Binary equivalent of 9 is 1001

Binary equivalent of A is 1010

Binary equivalent of 5 is 0101

The binary equivalent of 5A9 is 0101 1010 1001

$= 1280 + 160 + 9 = 1449$ (decimal).

EXAMPLE 4

Convert the hexadecimal number 12_H to its binary equivalent.

We replace the individual hexadecimal number by its binary equivalent and place them in their respective positions.

Binary equivalent of 2 is 0010

Binary equivalent of 1 is 0001

The binary equivalent of 12_H is 0001 0010

Verification:

Decimal equivalent of 12_H is $1 \times 16 + 2 = 18$ (decimal)

Decimal equivalent of 00010010 is (ignoring the three leading zeros)

$1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = 16+0+0+2+0 = 18$

13.5 OCTAL NUMBER SYSTEM

The base of the octal number system is 8. The digits are 0 to 7 same as those for the decimal number system. The number 8 of the decimal number system is represented by 10, 9 by 11 and so on. Table shows the octal representation of decimal number.

Decimal number	Octal number	Decimal number	Octal number
0	0	9	11
1	1	10	12
2	2	11	13
3	3	12	14
4	4	13	15
5	5	14	16
6	6	15	17
7	7	16	20
8	10		

13.5.1 Conversion of Octal number to Decimal number

The following examples illustrate the conversion of octal number to decimal number:

Example1: convert the octal number 23 to equivalent decimal number.

$$23 \text{ (octal)} = 2 \times 8^1 + 3 \times 8^0$$

$$= 2 \times 8 + 3 \times 1$$

$$= 16+3 = 19 \text{ (decimal)}.$$

Example2: convert the octal number 645 to equivalent decimal number.

$$645 \text{ (octal)} = 6 \times 8^2 + 4 \times 8^1 + 5 \times 8^0$$

$$= 6 \times 64 + 4 \times 8 + 5 \times 1$$

$$= 384 + 32 + 5 = 421 \text{(decimal)}.$$

Conversion of a decimal number to Octal:

Binary equivalent of 2 is 0010

Binary equivalent of 1 is 0001

The binary equivalent of 12_H is 0001 0010

Verification:

Decimal equivalent of 12_H is $1 \times 16 + 2 = 18$ (decimal)

Decimal equivalent of 00010010 is (ignoring the three leading zeros)

$1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = 16+0+0+2+0 = 18$

13.5 OCTAL NUMBER SYSTEM

The base of the octal number system is 8. The digits are 0 to 7 same as those for the decimal number system. The number 8 of the decimal number system is represented by 10, 9 by 11 and so on. Table shows the octal representation of decimal number.

Decimal number	Octal number	Decimal number	Octal number
0	0	9	11
1	1	10	12
2	2	11	13
3	3	12	14
4	4	13	15
5	5	14	16
6	6	15	17
7	7	16	20
8	10		

13.5.1 Conversion of Octal number to Decimal number

The following examples illustrate the conversion of octal number to decimal number:

Example1: convert the octal number 23 to equivalent decimal number.

$$23 \text{ (octal)} = 2 \times 8^1 + 3 \times 8^0$$
$$= 2 \times 8 + 3 \times 1$$
$$= 16+3 = 19 \text{ (decimal)}.$$

Example2: convert the octal number 645 to equivalent decimal number.

$$645 \text{ (octal)} = 6 \times 8^2 + 4 \times 8^1 + 5 \times 8^0$$
$$= 6 \times 64 + 4 \times 8 + 5 \times 1$$
$$= 384 + 32 + 5 = 421 \text{(decimal)}.$$

Conversion of a decimal number to Octal:

For the conversion of a decimal number to an octal number, the technique of successive division by 8 can be used. The following examples will illustrate the technique.

Example1: Convert 61(decimal) to its equivalent octal number.

8 | 61		remainder
8 | 7		5 (least significant digit)
0		7 (most significant digit)

The Octal Number = 75

13.5.2 Conversion of a decimal number to Octal

The decimal equivalent of an octal can be obtained as a sum of various octa digits multiplied by their respective place values.

Ex1: - Conversion of 1567.251_8 into decimal

Octal Number is	1	5	6	7	.	2	5	1
Place values	8^3	8^2	8^1	8^0		8^{-1}	8^{-2}	8^{-3}

Hence decimal equivalent of the given Octal is

$1X8^3 + 5X8^2 + 6X8^1 + 7X8^0 + 2X8^{-1} + 5X8^{-2} + 1X8^{-3}$

$= 512 + 320 + 48 + 7 + 0.25 + 0.078125 + 0.001135$

$= 887.3302_{10}$.

13.6 BCD (Binary Coded Decimal): A nibble is a string of 4 bits. Binary-coded – decimal (BCD) numbers express each decimal digit as a nibble. For instance, decimal 2,945 converts to BCD number as follows:

2	9	4	5
0010	1001	0100	0101

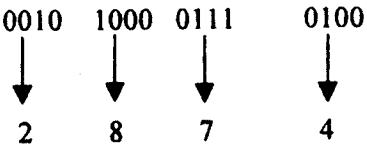
As you see, each decimal digit is coded as nibble.

Here's another example: 9.863_{10} converts like this:

9	8	6	3
1001	1000	0110	0011

Therefore, 1001 1000 0110 0011 is the BCD equivalent of $9,863_{10}$.

The reverse conversion is similar. For instance, 0010 1000 0111 0100converts as follows:



It is called the 8-4-2-1 code because the weight in the four bit group, reading from left to right are 8,4,2,and 1, same as that for binary numbers.

BCD codes very convenient and useful code for input and output operations un digital circuits.

In this code, each decimal digit is represented as a four bit binary number. In BCD arithmetic binary addition rules apply to individual digits. When ever the digit value becomes greater than 9, a carry is forwarded to the next digit just as in decimal addition. To facilitate this, 8085 has Decimal Adjust Accumulator instruction.. A single BCD digit appears as 05, 06 etc. These are called unpacked BCD. Usually in a 8 bit register two BCD digits can be packed as in 68.

BCD (Binary coded Decimal) A code used to represent decimal numbers.

Weighed codes: The BCD code is sometimes referred to as 8421 code because the weights of the digital positions from left to right are 8,4,2 and 1.. There are many other weighed codes such as the 7421, 6311, 5421, and so on.

13.7 BINARY CODES

A number system containing the only digits 1 and 0 is called binary number system. A pattern of numbers can be used as a code which has a special meaning. An organization may use straight binary with 8 bits or the 256 binary words to represent 256 different codes. Another organization may use these 256 words to represent entirely different purpose. 8085 and 6502 processors use 01 instruction code, but, it will be understood by them differently. If several organizations use the se binary words for similar purpose, it may be possible that they end up with same assignment of code. It may lead to copy write problems, losing secret information etc. To avoid this several types of binary codes were developed. Here a binary code is manipulated in a particular way to generate another binary number. It is used to codify information. The transmission of information takes place using this coded information. Reverse process defined will restore the original information to the genuine user. This will protect secrecy of information. For Engineering and Scientific application common understanding is necessary and for such purposes standard codes were developed. We now consider some standard codes. Like BCD, ASCII, GRAY, EBCDIC, Excess 3 etc.

We have already gone through the BCD (Binary coded decimal) and we consider the other codes now.

13.7.1 THE ASCII CODE

To get information into and out of a computer, we need to use numbers, letters, and other symbols. This implies some kind of alphanumeric code for the input unit of a computer. At one time, every manufacturer had a different code, which led to all kinds of confusion. Eventually, industry settled on an input-output code known as the "American Standard Code for Information Interchange (abbreviated ASCII). This code allows manufactures to standardize input hardware such as keyboards, printers, video displays, and so on.

$X_3X_2X_1X_0$	$X_6X_5X_4$					
	010	011	100	101	110	111
0000	SP	0	@	P		p
0001	!	1	A	Q	a	q
0010	"	2	B	R	b	r
0011	#	3	C	S	c	s
0100	$	4	D	T	d	t
0101	%	5	E	U	e	u
0110	&	6	F	V	f	v
0111	'	7	G	W	g	w
1000	(	8	H	X	h	x
1001	)	9	I	Y	i	y
1010	*	:	J	Z	j	z
1011	+	;	K		k	
1100	,	<	L		l	
1101	-	=	M		m	
1110	.	>	N		n	
1111	/	>	O		o	

The ASCII (pronounced ask'-ee) code is a 7-bit code whose format (arrangement) is

$$X_6\ X_5\ X_4\ X_3\ X_2\ X_1\ X_0$$

Where each X is a 1. For instance, the letter A is coded as

1000001

Sometimes, a spaces is inserted for easier reading

100 0001

Table shows the ASCII code. Read the table the same as a graph. For instance, the letter A has an X_6 X_5 X_4 of 100 and an X_3 X_2 X_1 X_0 of 0001. Therefore, its ASCII code is

100 0001(A)

Table includes the ASCII code for lowercase letters. The letter a is coded as

110 0001 (a)

More examples are

110 0010 (b)
110 0011 (c)
110 0100 (d)

And so on.

Also look at the punctuation and mathematical symbols. Some examples are

110 0100 ($)
010 1011 (+)
011 1011 (=)

In table SP stands for space (blank). Hitting the space bar of an ASCII keyboard Sends this into a computer:

010 0000 (space)

ASCII: (American Standard Code for Information Interchange): A binary code used for communication purpose. Special 6 bit, seven bit and eight bit codes are developed. As it is used to represent numbers and characters and typewriter symbols It is called a Character code. This code allows manufacturers to standardize computer hardware such as keyboards, printers, and video displays.

EBCDIC: (Extended binary coded Decimal Interchange Code). It is the standard binary code for large computers. As it is used to represent numbers and characters and typewriter symbols It is called a Character code

Excess-3 code is an important 4-bit code sometimes used with binary-coded decimal numbers.. To convert decimal numbers in to excess-3 code add 3 to each decimal digit, and then convert the sum to a BCD number code.

13.7.2 GRAY CODE

This code is often used in digital systems because only one bit in the code group changes when going from one number to the next. For example, in going from 7 to 8 binary number changes from 0111 to 1000 (all the four bits change values) while Gray code changes from 0100 to 1100 (only the first bit from left changes from 0 to 1, the other three bits remain the same). Similarly, 1100 represents 8 and 1101

represents 9 in Gray code. These two consecutive numbers also differ only in one bit (fourth from left)

It is not suited for arithmetic operation but is often employed for A/D converters and location of angles on a rotating shaft.

In order to convert binary numbers to Gray code numbers, following procedure is adopted.

- The first Gray digit is the same as the first (msb) binary digit.
- The next Gray digit is the sum of first two bits in mod-2 addition* i.e., the carry, if any ignored.
- This process of mod-2 addition is represented by adding second bit to third and so on until entire Gray -code number is obtained.

The Gray code: Each Gray code number differs from the preceding number by a single bit. It was developed for Engineering application.

To convert a Gray code in to Binary the following procedure is adopted.

We see how a binary code can be converted to Gray code and vice versa.

Consider the 8 bit binary number. We convert it to Gray code. D7 bit of binary number is copied to D7 bit of Gray Code.. The D6 bit is exclusive ORed with D7 bit and is taken as D6 bit of Gray code. The D5 bit is likewise Ex-ORed with its previous bit(D6) and is taken as D5 bit of Gray code. This procedure is repeated for the other bits of binary number to form corresponding Gray code.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Ex1: Binary	1	0	0	1	1	1	0	1
Gray	D_7	$D_7 \oplus D_6$	$D_6 \oplus D_5$	$D_5 \oplus D_4$	$D_4 \oplus D_3$	$D_3 \oplus D_2$	$D_2 \oplus D_1$	$D_1 \oplus D_0$
	1	1	0	1	0	0	1	1
Ex 2	0	0	1	1	0	0	1	1
Gray	0	0	1	0	1	0	1	0
Ex3	0	1	0	1	1	0	1	1
Gray	0	1	1	1	0	1	1	0

GRAY TO BINARY

Gray	G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0
Binary	D_7	$D_7 \oplus G_6$	$D_6 \oplus G_5$	$D_5 \oplus G_4$	$D_4 \oplus G_3$	$D_3 \oplus G_2$	$D_2 \oplus G_1$	$D_1 \oplus G_0$
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Gray	0	0	1	0	1	0	1	0
Binary	0	0	1	1	0	0	1	1

Besides these to detect errors in transmission error detecting codes, error correcting codes like Hamming code are also in use.

Computers deal only with binary numbers. However, we appreciate if the display is in decimal form. Therefore it is necessary to convert binary results in to their BCD form. The conversion of Binary to BCD is done by dividing the number by the power of 10. The division is done by subtraction method.

Example: Assume the given binary number is 1111 1111. = FFH = 255D. To represent this number in BCD 12 bits or three BCD digits are required as BCD2,BCD1,BCD0

i.e 255D = 00010 0101 0101

BCD3 BCD2 BCD1

Eg:	Quotient
255	
-100 = 155	1
-100 = 55	1
	1+1 = 2

The conversion is performed as follows BCD3 =

13.8 Taking care in number representation: In the problems we are given usually decimal numbers unless specified explicitly. Microprocessor assembly language program accepts Hexadecimal or Hex numbers. While representing numbers like 213 40 etc, we must be careful as they may belong to decimal as well as hexadecimal systems. In hexadecimal form, 29 is not equal to decimal 29. Its equivalent is 41. So good practice is to put a suffix. Some people put 10 as subscript after Least significant digit to indicate that they consider it as a decimal number. Some people prefer D after LSD to represent decimal numbers as in 14_{10} or 14_D. In the case of Hex numbers, 16 is used as subscript. Some others put H as suffix or subscript after LSD, as in 14_{16} or 14H

13.13 SUMMARY

We are familiar with decimal number system in which digits are 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9. The base of the decimal number system is 10. The decimal number system is convenient for the programmer. The computer uses binary digits for its operation. In the binary system there are only two digits 0 and 1. The base of the binary number system is 2. The programmer feeds instructions and data in alphabets and decimal digits. But, for the operation of the computer these are converted to binary bits.

1's complement to a binary number can be obtained by complementing all its bits (i.e) replacing 0's by 1's vice versa. 2's complement to a binary number can be obtained by adding 1 to the 1's complement of the binary number. The hexadecimal number system is widely used with computers and other digital systems. The base of is 16. The digits from 0 to 9 are same as those of the decimal number system 16.

In the hexadecimal system 10 is represented by A, 11 by B, 12 by C, 13 by D, 14 by E, and 15 by F. The decimal number 16 is represented by 10 in the hexadecimal system; 17 by 11 ; 18 by 12; 32 by 20; 33 by 21 and so on. The base of the octal number system is 8. The digits are 0 to 7 same as those for the decimal number system. The number 8 of the decimal number system is represented by 10. Binary-coded –decimal (BCD) numbers express each decimal digit as a nibble.

It is called the 8-4-2-1 code because the weight in the four bit group, reading from left to right are 8,4,2,and 1, same as that for binary numbers.

BCD codes very convenient and useful code for input and output operations un digital circuits. For Engineering and Scientific application common understanding is necessary and for such purposes standard codes like BCD, ASCII, GRAY, EBCDIC, Excess 3 etc were developed.

Some people put 10 as subscript after Least significant digit to indicate that they consider it as a decimal number. Some people prefer D after LSD to represent decimal numbers as in 14_{10} or 14D. In the case of Hex numbers 16 is used as subscript. Some others put H as suffix or subscript after LSD

13.10 KEY WORD TERMINOILOGY

GRAY code: It is an unweighed code. It is not suitec for arithmetic operations but is useful for peripheral equipment and A/D converters.

Parity bit: In order to check for errors in the transmission of binary information, one of the methods used is to attach an extra bit called parity bit. Two kinds of parity exist – even parity and odd parity. Even parity means attaching an extra bit to yield an even number of 1's. Parity checks will detect all one bit errors but not two-bit errors.

13.11 SELF ASSESSMENT QUESTIONS

Long Answer Questions:

1. Discuss in detail about Binary, Decimal, Hexadecimal and Octal number system.
2. Explain BCD and Gray codes with examples.
3. What are binary, decimal, hexadecimal and octal numbers? Explain with examples the conversion
   - (i) Binary number to decimal number.
   - (ii) Decimal to hexadecimal.
   - (iii) Octal number to binary.
4. Explain about the binary number system?
5. Discuss about decimal to binary conversion?

6. Explain about binary to decimal conversion?
7. Explain about the hexadecimal number system?
8. Explain about the octal number system?
9. Mention the ASCII code.
10. What is 2's complement of a Binary number? Illustration of Binary numbers using 2's complement method. What is the advantage of this method?

Short Answer Questions:

1. Give various number systems used in digital electronics.
2. What is a binary number system? How does it differ from decimal number system.
3. Write first 18 binary numbers starting with zeros.
4. Convert 12.06725 into a binary number.
5. Explain BCD and Gray codes with examples.
6. Mention the ASCII code
7. Convert decimal number 37 into binary, hexadecimal and octal codes.
8. Convert decimal number 41into binary, hexadecimal and octal codes.
9. Write about Gray code.
10. Convert the following binary numbers to gray code numbers.

TEXT AND REFERENCE BOOKS

TEXT BOOKS

1. Integrated Electronics by Millman and Halkias
2. Electronic Communications by Kennedy
3. Principles of Digital Electronics by Malvino and Leach
4. Basic Electronics and Linear Circuits - Bhargava etc

REFERENCE BOOKS

1. A text lab manual in Electronics by ZBAR (Tata Mc Graw Hill)
2. Electronics fundamentals by JD Ryder
3. Modern Electronics Communications by Gray and Miller
4. Digital Electronics by William H.Gothman
5. Op.Amp and linear integrated Circuits by Ramakant Gayakwad
6. Electronic Devices and Circuits by Samuel Seely.

DIGITAL ELECTRONICS - BASIC LOGIC GATES

OBJECTIVES OF THE LESSON

To understand what digital electronics is, to learn Boolean algebra , to understand various basic logic gates, to understand De Morgan's theorems and to know about universal logic gates.

STRUCTURE OF THE LESSON

14.1 INTRODUCTION

The term **digital** refers to any process that is accomplished using discrete units, e.g. fingers, toes, digits etc. Each of these can be used as a unit or group of units to express a whole number. On the other-hand, analog numbers are represented as directly measurable quantities such as volts, distances, and rotations etc. Thus, in analog method, a number can be represented as an angle (in degrees) rotation of the needle on a meter. This method has been used widely in electronics to represent intensity, frequency, and time etc. The two factors namely accuracy and economy made the people to prefer digital readout devices. As examples we can quote: Digital multi-meters, Digital frequency counters, Screw gauges, Vernier calipers with digital readout facility.

Though there are many number systems, in digital electronics, binary system is used extensively. Good amount of accuracy and reliability that can be achieved with digital electronics. Because of this reason, conventional electronic circuits are being replaced with digital circuits. Already we see present day communication is based on digital techniques. Digital electronics is also extensively used in computers.

In computers information and data are processed in terms of only zeros and ones (0 and 1) which are called binary digits. In binary system those are only two digits 0 and

1. The **Bi**nary digits are called Bits. The programmer feeds instructions and data in a form that looks like English. For example ADD for addition, SUB for subtraction etc. Later computer converts these instructions and data into binary digits before processing. Processing of data in computers is performed by digital circuits. Because the data in computers is in the form of 0's and 1's, a special logic is developed by George Boole to perform the arithmetic and logic operations. Hence the algebra developed for binary systems is known as Boolean algebra.

In a digital system, we will consider inputs and outputs, as either 0's or 1's. In order to express the input and output relationship, an algebra known as switching algebra is useful. Shannon developed this for use in telecommunication switching circuits. It is based on a more general algebra that was developed earlier by Boole. This algebra uses a limited number of operators to connect variables together to form expressions. Further, it is also easy to build electronic circuits to implement these operators. Boolean Algebra is the algebra of binary variables. Any system, which has only two states, can be expressed in terms of Boolean logic. For example a statement can be either true or false, if it is true we can represent it as logic 1 and if is false we represent it by 0. This is called positive logic.

Existence of positive voltage at a point may be taken as logic 1. Zero voltage can be represented as logic zero. A glowing bulb, a current flow, a happening of an incident can be represented by logic 1 or TRUE state. The complementary actions can be represented by a 0 or FALSE state. In fact we may represent actions that were represented by 1 by logic 0 also. It all depends on one's choice. The electronic circuits used to perform Boolean operations are called gates. The gate is a circuit with one or more input signals but only one output signal. These gates are constructed by using diodes and transistors (known as DTL logic) or using transistors only (known as TTL) Technical standards were evolved in electronics depending on the implementation of integrated circuits using various semiconductor technologies viz DTL,TTL,ECL etc. The most important and popular semiconductor logic is Transistor-Transistor Logic (TTL), in which a +5V DC is taken as logic 1 and zero volts is taken as logic 0 .

This chapter introduces the fundamentals of Boolean operations, corresponding logic circuits and gates and integrated circuits related to these circuits are discussed.

14.2 Boolean Algebra :

The fundamental operations in Boolean algebra are OR, AND and NOT, with symbols + (plus),. (dot) and bubble or bar over Boolean variable respectively.

In real life applications, one combines several logic gates and the combined effect determines a system behavior depending on the states of individual logic variables. This is usually expressed in terms of a truth table. In truth table, various inputs are listed and various combinations are workedout to determine the system behavior. As a simple example, see the OR gate truth table given in table 14.3a. Here A and B are the input variables. These two variables can have 2^2=4 combinations of 1s and 0s. As per the Boolean equation y = A + B (A+B to be red as A or B), output is true for 3 input combinations and false for one combination.

The following are the laws of Boolean algebra and complicated laws can be proved using simple Boolean laws. These laws can be verified by writing truth tables for L.H.S and R.H.S expressions.

1. $A + 0 = A$
2. $A + 1 = 1$
3. $A + A = A$
4. $A + \overline{A} = 1$

} Laws of 'OR'

5. $A \cdot 0 = 0$
6. $A \cdot 1 = A$
7. $A \cdot A = A$
8. $A \cdot \overline{A} = 0$

} Laws of 'AND'

9. $\overline{0} = 1$
10. $\overline{1} = 0$
11. of A = 0 then $\overline{A} = 1$
12. of A = 1 then $\overline{A} = 0$
13. $\overline{\overline{A}} = A$

} Laws of complementation (NOT Laws)

14. $A + B = B + A$
15. $A \cdot B = B \cdot A$

} Commutative Laws

16. $A + (B + C) = (A + B) + C$
17. $A \cdot (B \cdot C) = (A \cdot B) \cdot C$

} Associative Laws

18. $A \cdot (B + C) = (A + B) \cdot C$
19. $A + B \cdot C = (A + B) \cdot (A + C)$

} Distributive Laws

20. $A + \overline{A}B = A + B$
21. $A + AB = A$
22. $A(A + B) = A$
23. $A(\overline{A} + B) = AB$
24. $AB + \overline{A}B = A$
25. $(A + B)(A + \overline{B}) = A$
26. $AB + \overline{A}C = (A + C)(\overline{A} + B)$
27. $(A + B)(\overline{A} + C) = AC + \overline{A}B$
28. $AB + \overline{A}C + BC = AB + \overline{A}C$
29. $(A + B)(\overline{A} + C).(B + C) = (A + B)(\overline{A} + C)$
30. $\overline{A + B + C + \text{--}} = \overline{A}.\overline{B}.\overline{C}.\text{---}$ } De Morgan's Laws
31. $\overline{A.B.C.\text{--}} = \overline{A} + \overline{B} + \overline{C} + \text{---}$ }

14.3 BASIC LOGIC GATES

Basically, a logic gate is a circuit with one or more logic input signals (each input is either 0 or 1), but with only one output signal (logically related to inputs). Logic circuits are analyzed with the help of Boolean laws.

The basic logic gates are: OR, AND and NOT

14.3.1 OR Gate:

An OR gate has two or more input signals but only one output signal. If one or more input signals are high, the output signal is high.

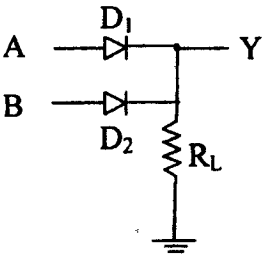
Boolean expression for two input OR gate is

$$Y = A + B$$

(read as Y equals A OR B).

The circuit to implement the OR function, logic symbol and its truth table(which depicts the output condition to given input is shown in Fig.14.1.

Any one or both of the inputs A, B are high (+5V) makes the corresponding diode to forward bias and the current flows through load resistor R_L to have an output at Y. An OR gate can have any number of inputs 1 to n. For example two input OR-gates can be used to form a 3 input OR gate as shown in Fig.14.2



Circuit of OR gate

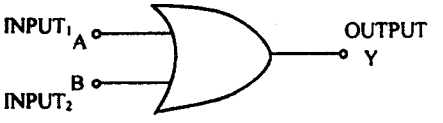


Fig 14.1 Logic Symbol of OR gate

TURTH TABLE

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Truth table

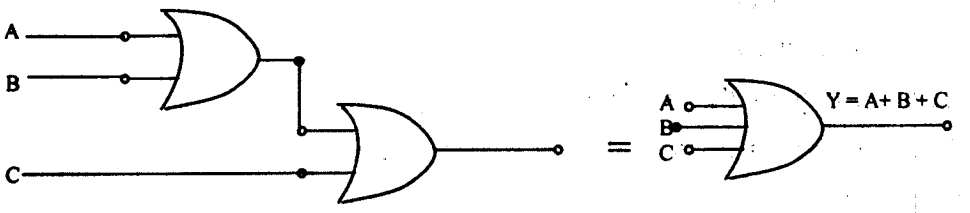


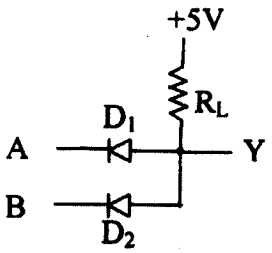
Fig.14.2: Two two - input OR gates connected to form a 3 input OR gate.

The OR gate circuit of Fig 14.1 constructed by using diodes and resistors . But the same OR gate can also be constructed by using transistors only (TTL circuit). The logic gates are available in the form of integrated circuits(ICs) to offer advantages in terms of size, cost and power. The IC 7432 is a quad (four), two input OR gate using TTL logic and 74LS32 and 74HS32 are the low power and high speed versions of the same OR gate.

14.3.2 AND gate:

The AND gate has two or more inputs but has only one output. If all the inputs are simultaneously high, the output is high. Boolean expression for two input AND gate is Y = A . B (read as Y equals A AND B). The circuit to implement AND function, corresponding logic diagram and its truth table is shown in Fig.14.3.

When any one or both of the inputs in above circuit are low, the diode of that input becomes forward biased, so the level of voltage at output point Y is at 0V i.e low state.



Circuit of AND gate

TURTH TABLE

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

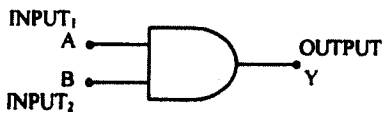


Fig.14.3 Logic Symbol of AND gate

On the other hand, if both A and B are high, both diodes are now in reverse biased having same voltages at both ends. So 5V now appears at Y, i.e high state.

As in the case of OR gate, the two input AND gates can be used to construct three input or n-input AND gate. Construction of 3-input AND gate by using two 2-input AND gates is shown in Fig.14.4.

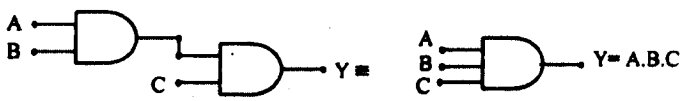


Fig 14.4

IC 7408 / 74LS08 is a Quad two input AND gate whereas IC 7411 is a triple 3 input AND gate IC.

14.3.3 NOT gate: (Inverter gate):

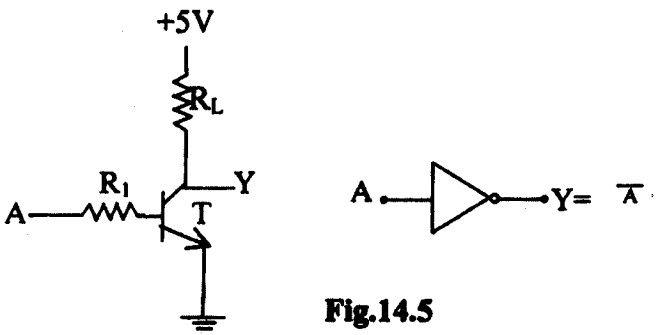


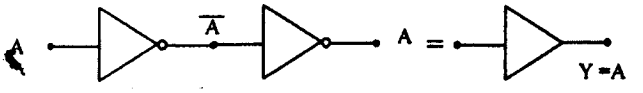
Fig.14.5

TRUTH TABLE

Input A	Output Y
0	1
1	0

The inverter is a gate with only one input and one output. The output state is always the opposite of the input state. It is also called as NOT gate. Boolean expression for this gate is $Y = \overline{A}$ (read as Y equals complement of A or Y equals NOT of A). The circuit, logic symbol and its truth table is shown in Fig.14.5.

In the above circuit, the transistor is working either in the conduction or cut-off state. When a high state (+5V) is presented in input make the transistor to conduct and to produce 0V or low state at output. On the other hand, a low state at input A produces a high state at output Y by cut-off the transistor T. Input given to two NOT gates connected in cascade results in the original Boolean variable as shown in Fig.14.6. This is called as a **buffer.**



TRUTH TABLE

Input A	Output Y
0	0
1	1

Fig.14.6 Two NOT gates connected to form a buffer, logic symbol of buffer and truth table

Electronically buffers are very useful as they do not alter the nature of original signal but provide boosting of signal amplitude and power to standard levels. This prevents logic failure due to fall in signal strength. Tri-state buffers are also available whose output can be 0 or 1 or tri-state. In the tri-state condition the signal path is disconnected. These tri-state buffers are used in advanced logic circuits like Microprocessors and memories.

14.3.4 NOR gate:

Fig 14.7

TRUTH TABLE

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

The basic logic circuits are used to construct some more gates to perform more Boolean functions. For example, consider the NOR gate which has two or more inputs but only one output. All the inputs must be low to get a high output. Boolean expression for two input NOR gate is

$Y = \overline{A + B}$.

(read as Y equals not of A OR B).

The NOR gate can be constructed by connecting an OR gate with NOT gate as shown in Fig 14.7

The NOR gate may have more than two inputs. Regardless of how many inputs a NOR gate has, it is still logically equivalent to one OR gate followed by an inverter. For instance, the equation for 3-input NOR gate is $Y= \overline{A+B+C}$. The 7402 is a quad 2-input NOR gate where as 7427 is a triple 3-input NOR gate.

14.3.5 NAND gate:

A NAND gate has two or more inputs but only one output. All the input are the simultaneously high to get a low output. Boolean expression for two – input NAND gate is

$Y = \overline{A.B}$ (read as Y equals Not of A AND B).

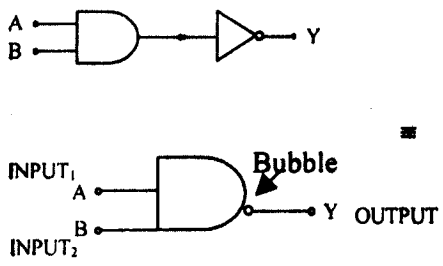


Fig 14.8 Logic Symbol of NAND gate

TRUTH TABLE

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

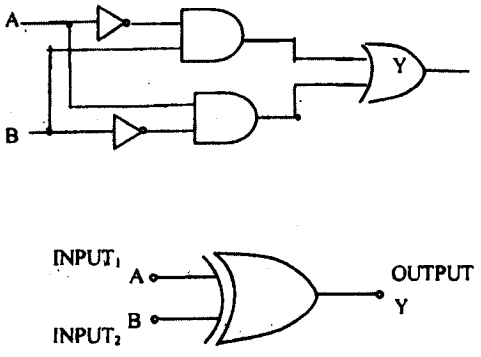
The Boolean equations for 3-input and 4-input NAND gates are $Y = \overline{ABC}$ and $Y = \overline{ABCD}$ respectively.

The IC 7400 have 4 Nos of 2- input NAND gates, whereas 7410 have three numbers of 3-input NAND gates.

14.3.6 EX – OR gate:

An OR gate recognizes words with one or more 1s, whereas the exclusive – OR gate recognizes only words that have an odd number of 1s. Boolean expression for two – input

EX-OR gate is $Y = A\bar{B} + \bar{A}B = A \oplus B$. (read as Y equals A EX-OR B). The logic diagram, symbol and its truth table is shown in Fig 14.9.



TRUTH TABLE

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Fig 14.9 Logic Symbol of EX-OR gate

When h inputs A & B in the above circuit are both high and or low, the AND gates have low output and give the final output as zero. But when any one of the input (A or B) is high, the corresponding AND gate output is high. So the final output is one as shown in truth table. IC 7486 is the IC version of EX – OR gate.

Transistor OR Gate:

Figure14.10 shows a transistor OR gate. It consists of three transistors Q_1, Q_2 and Q_3 supplied from supply V_{CC} = 5 VOLT

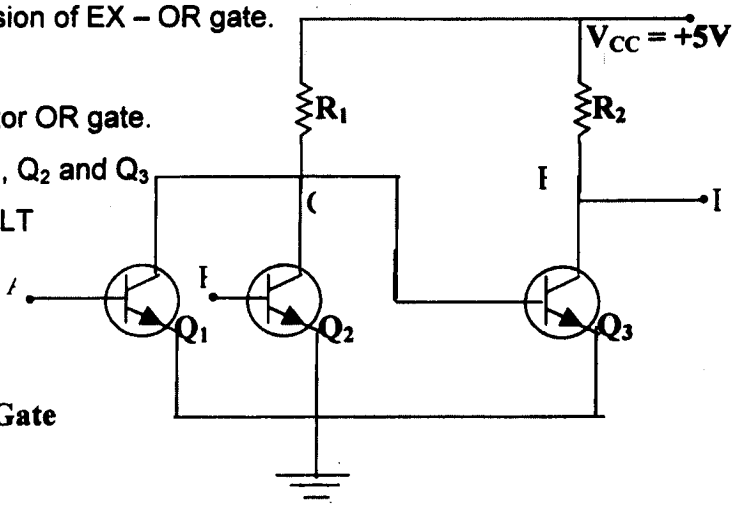


Fig 14.10: Transistor OR-Gate

(i) If A = 5V i.e., +5V is applied to A, Q_1 is forward biased and hence conducts. When Q_1 is saturated, entire V_{CC} = 5V drops across R_1 and hence C goes to ground i.e., its potential = 0V. Consequently Q_3 is cut off and D goes to V_{CC} = 5V.

(ii) (ii) If B = 5V i.e., Q_2 is forward biased and hence conducts. It causes C to go to ground i.e., C = 0V. Thus there is no forward bias on the base of Q_3. Hence Q_3 is cut off and D again goes to V_{CC} = 5V.

(iii) If A = 0V, B = 0V i.e., both A and B are grounded. Then Q_1 and Q_2 are both cut -off. Consequently, Q_3 becomes forward biased and conducts. As a result, entire V_{CC} drops across R_2. It drives E and hence D to ground i.e., output = 0V.

Transistor AND Gate:

Fig.14.11 shows a transistor AND circuit, consisting of three transistors Q_1, Q_2 and Q_3 supplied from a common supply V_{CC} = 5 V.

When A = B = +5V, then both transistors Q_1 and Q_2 conduct. Consequently, supply voltage of +5V drops across R_1. It drives point C and hence base of transistor Q_3 to ground or 0 volt. Consequently, transistor Q_3 is cut off and D goes to supply voltage +5V. Thus there is an output at C only when there is input at A and B.

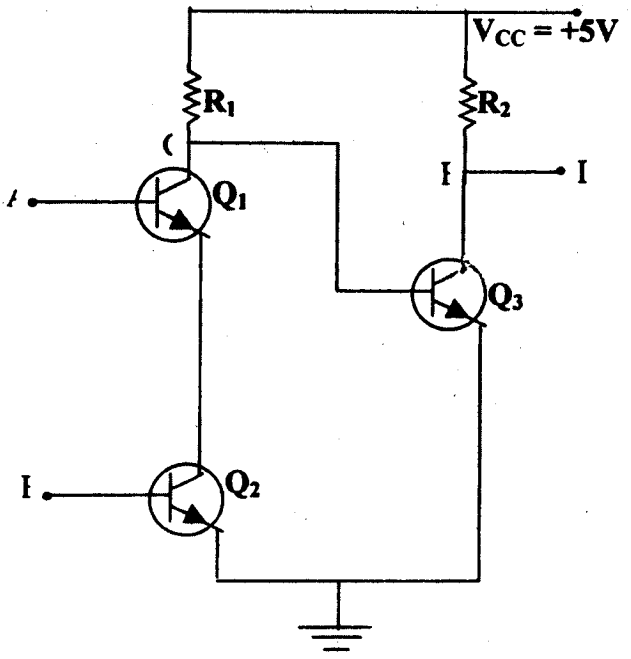


Fig.14.11 Transistor AND - Gate

If either A = 0V or B = 0V Q_1 or Q_2 will be cut off and the will be no drop across R_1. Then point C will be at +5V. As a result Q_3 will conduct dropping entire V_{CC} across R_S. It drives E and hence D to ground i.e., 0 volt

14.4 DE MORGAN'S THEOREMS

The Boolean algebra developed by George Boole was further extended by De Morgan by his famous theorems that can be used in the simplification of logic circuits.

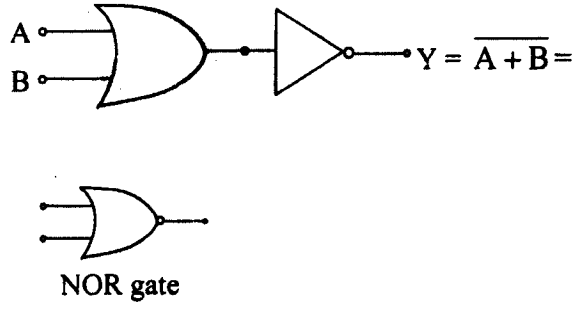
14.4.1 De Morgan's First Theorem

$$\overline{A+B} = \overline{A}.\overline{B}$$

Statement: Complement of sum equals the product of the complements.

Proof: The theorem can be proved by taking expressions and writing the truth tables on both sides. And finally we equate LHS to RHS.

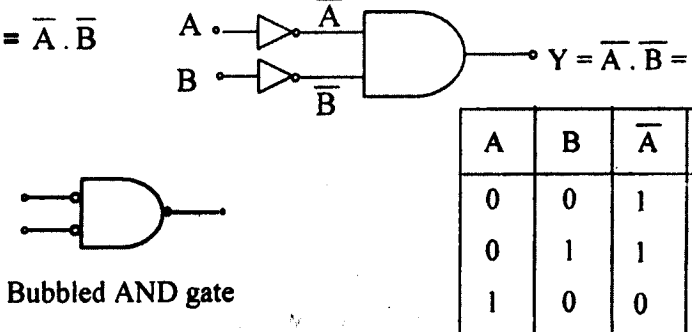
Consider L.H.S i.e $\overline{A+B}$. It indicates a 2-input OR gate followed by a NOT gate that is a NOR gate as shown in Fig14.12. Fig 14.12 also shows its truth table. Similarly take the R.H.S of the theorem which is equal to $\overline{A}.\overline{B}$. This equation indicates that the two inputs A and B are inverted before they reach the AND gate as shown in Fig.14.13. Therefore we have the truth table as in Fig 14.13 for this circuit. Therefore the comparison of the truth table of Fig.14.12 with the truth table of Fig14.13 reveals that these two are equivalent; and the circuits of Fig.14.12 and Fig. 14.13 are equivalent. Hence the theorem is proved.



A	B	A+B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Fig 14.12

R.H.S = $\overline{A}.\overline{B}$



A	B	$\overline{A}$	$\overline{B}$	$\overline{A}.\overline{B}$
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	0

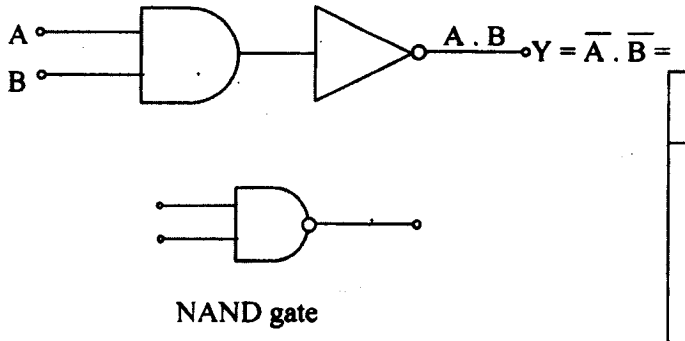
Fig 14.13

14.4.2 De Morgan's Second Theorem

$\overline{A.B}$ = $\overline{A}$ + $\overline{B}$

Statement: Complement of product equals the sum of the complements.

Proof: Left hand side of the theorem shown is a 2-input AND gate followed by a NOT gate i.e. a NAND gate having the circuit and truth table as shown in Fig 14.14.



A	B	A . B	$\overline{A . B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Fig 14.14

The right hand side of the equation shows an OR gate with two inverted inputs. The circuit and truth table is shown in Fig.14.15

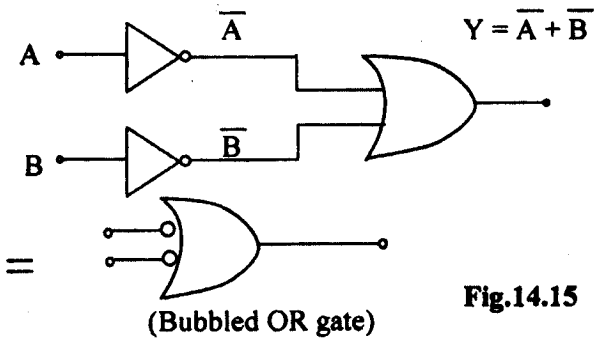


Fig.14.15

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}$ + $\overline{B}$
0	0	1	1	1
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0

Comparison of these two truth tables reveals that they too are identical and equal. Therefore the theorem is proved.

14.5 UNIVERSAL LOGIC GATES

The logic gates NAND and NOR are called Universal Building Blocks or Universal Logic Gates because using either NAND or NOR gates we can construct other logic gates (AND, OR, NOT, EX-OR) as well as we can implement Boolean functions.

14.5.1 FORMATION OF OTHER LOGIC GATES USING ONLY NAND GATES

(i) NOT gate: From the truth table of the NAND gate given in Fig 14.16, we know that the same inputs of the NAND gives its complement output viz if A = B = 0 we have an

output of 1 and if A = B = 1, the output is 0. Hence the circuit of Fig 14.16 acts as NOT gate.

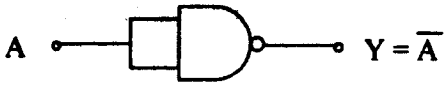


Fig 14.16

ii) AND gate: The Boolean expression for NAND is Y= $\overline{A.B}$. So, the first NAND gate output in the Fig 14.17 is $\overline{A.B}$ and second NAND gate simply a NOT gate. Now the circuit is simply an AND gate circuit.

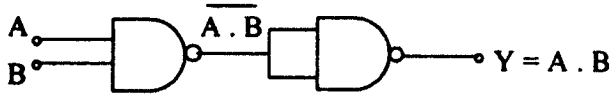


Fig 14.17

(iii) OR gate: Two NOT gates of Fig 14.16 gives output of $\overline{A}$ and $\overline{B}$, which are the inputs of second NAND gate. Hence, second NAND gives an output of $\overline{\overline{A}.\overline{B}}$. According to second De Morg.. 's theorem it can be written as $\overline{\overline{A}} + \overline{\overline{B}}$ which can also be written as A+B($\overline{\overline{A}}$ =A and $\overline{\overline{B}}$ = B). Refer fig 14.18. It is the output of an OR gate.

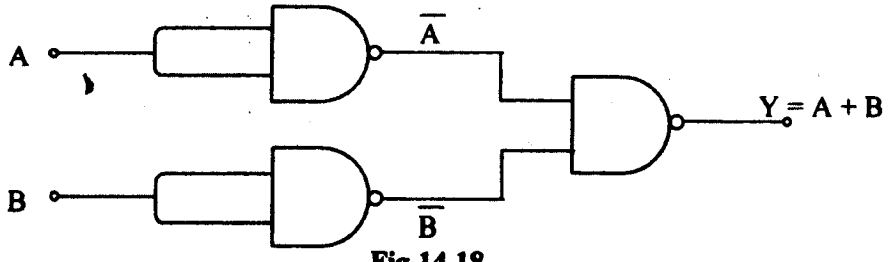


Fig 14.18

(Iv) NOR gate:

Addition of another NOT gate to the circuit for OR gate of Fig 14.18 as shown in Fig 14.19 gives the operation of a NOR-gate.

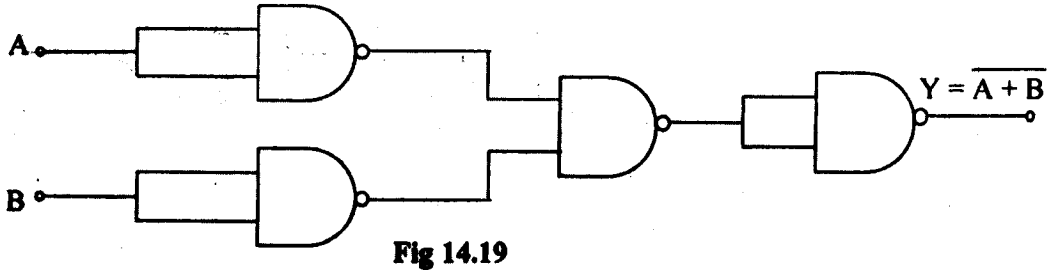


Fig 14.19

(iv) EX – OR gate: We can form an Ex-OR logic gate using only NAND gates As the Boolean expression can be represented in more than one way, more types of circuit implementations are possible. In Fig 14.20 we see an Ex-OR gate using minimum number of NAND gates.

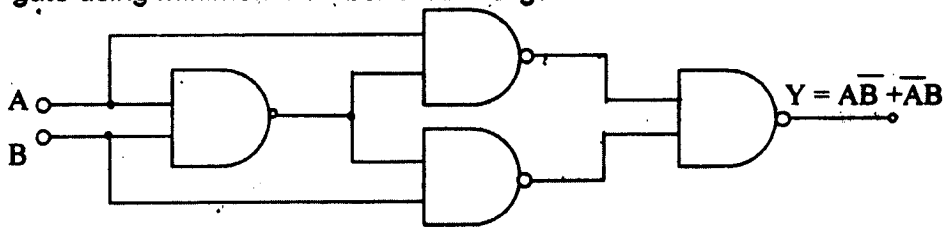


Fig 14.20

14.5.2 FORMATION OF OTHER LOGIC GATES USING ONLY NOR GATES

(i) NOT gate :

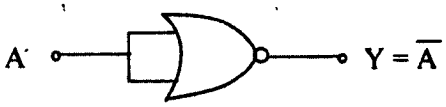


Fig.14.21

(ii) OR gate:

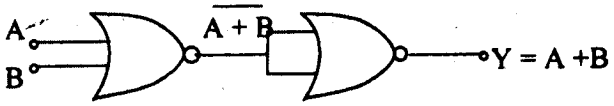


Fig.14.22

(iii) AND gate:

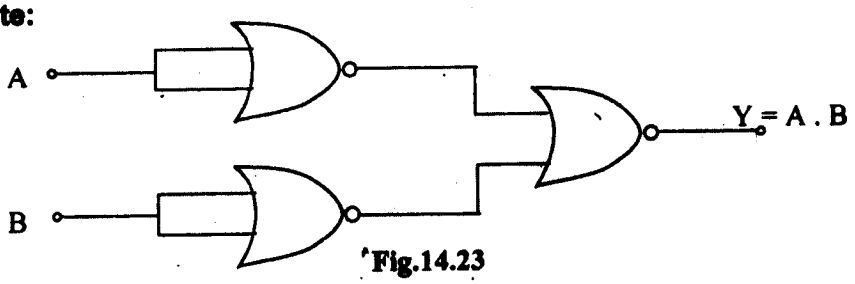


Fig.14.23

(iii) NAND gate:

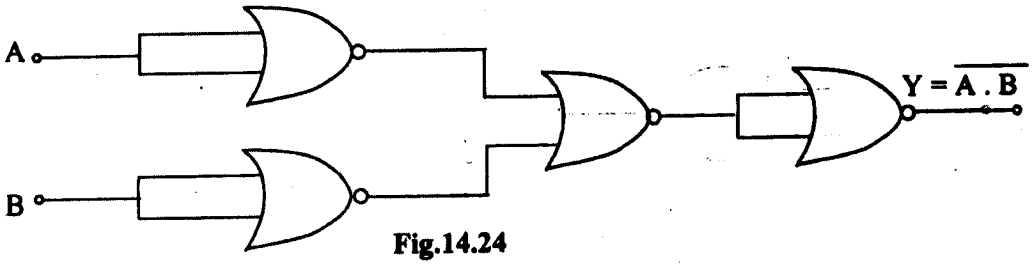


Fig.14.24

(v) EX - OR gate:

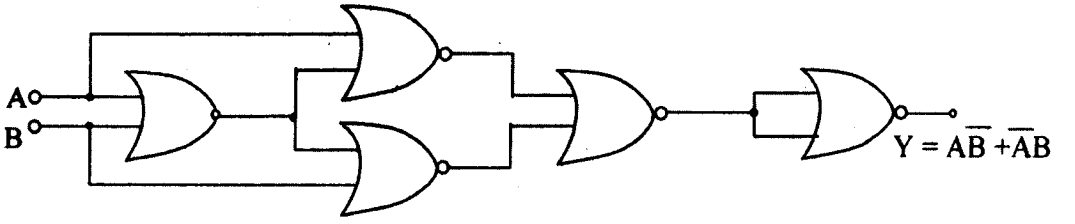


Fig.14.25

Of the several technologies available, Transistor–Transistor Logic is widely used where logic 1 is represented by +5V DC. And Logic zero by 0V DC. Circuits using other types of logic are provided with TTL logic compatibility to facilitate easy interfacing of logic circuits.

When a logic gate is connected to another logic gate, depending on the logic status it is supposed to supply or take currents. Supplying current is called sourcing and taking the current is called sinking. Capability of a circuit depends on how much current a circuit can sink and source.

This is expre ;ed in terms of how many logic gates can be connected to it (fan-in) and how many circuits can be driven by it (fan-out). For standard TTL fan – out is 10.

Logic circuits are supposed to change their states from 0 to 1 or 1 to 0 instantaneously, but, electronic circuits have inherent delays and because of it, there will be some definite rise time, fall time and propagation delay as a signal passes from input to output. Further there will be signal attenuation and induction effects and noise, which affect signal amplitude. For a standard TTL circuit if a logic 1 signal amplitude falls below 2.4V DC it cannot be recognized as Logic1. Like wise, if logic 0 signal amplitude is greater than 0.4V DC it cannot be identified as logic 0. This results in failure of logic circuits. Crossing the fan-in and fan-out limits also changes logic voltages. So, logic circuits are to be buffered to bring back, the signal levels to TTL levels before they fall down. A signal in its transmission path may develop glitches, slopes and other types of distortion. Schmitt trigger circuit is used to produce rectangular wave shape regardless of the input waveform.

14.6 SUMMARY

Digital electronics mainly deals with binary number system. Binary number system has a base of 2. It has two numerals 0 and 1. Any big number can be expressed in the form of 0s and 1s. In a digital system, logic 1 means high positive signal value, logic 0 means low positive signal value in a positive logic system. But in a negative logic

system, zero value represents logic 1 and a negative value represents logic '0'. Digital electronics mainly depends on Boolean algebra and logic gates. Using the gates, one can construct bit circuits that can perform complex operations. These gates possess, in general, 2 or more inputs and only one output. NOT, OR and AND are the basic logics and circuits used to implement higher logic. However semiconductor technology prefers NAND and NOR logic gates. Using only NAND or NOR gates, other logic gates can be constructed. Because of this reason, NAND and NOR are called **Universal logic gates.**

De Morgan's first theorem says that a NOR gate and bubbled input AND gate are equivalent. Similarly De Morgan's second theorem says that a NAND gate and bubbled input OR gate are equivalent. If Boolean expressions are given, one can construct logic circuits. On the other hand if logic circuits are given, one can write the Boolean expressions.

Logic gates can be fabricated using various Semiconductor technologies like TTL, NMOS, and CMOS etc. Each technology has its own advantages.

14.7 KEY TERMINOLOGY

(i) Gate: An electronic circuit with one or more inputs but with only one output.

(ii) Logic Gate: As the gates simulate mental processes, these are often called Logic Gates.

(iii) Universal Gate: The gate with which other logic circuits / gates can be constructed (Ex NAND, NOR)

(iv) Boolean Algebra: The modern algebra that uses the set of numbers 0 and 1.

(v) Complement: The output of an inverter gate.

(vi) Truth table: A table that shows all input and output possibilities for a logic circuit.

(vii) Word: A string of bits that represent a coded instruction or data.

(viii) Fan – in: The maximum number of inputs that can be applied to a logic gate.

(ix) Fan – out: The number of gates that can be driven by a logic gate.

14.8 SELF – ASSESSMENT QUESTIONS

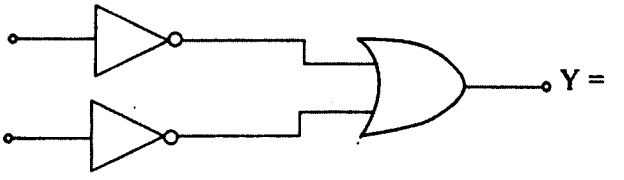
Long answer questions:

1. Explain the basic laws of Boolean algebra
2. Simplify $Y = (A + B)(A + \bar{B})(\bar{A} + \bar{B})$ by using Boolean algebra
3. Prove that $\overline{A + B + C + D} = \bar{A}\bar{B}\bar{C}\bar{D}$

Short answer questions:

1. Prove the De Morgan's Theorems.

2. Draw the truth table of 3 – input, EX – OR gate.
3. Draw the truth table of 4 – input NOR gate.
4. What is the Boolean equation of the figure given below?



5. Draw the logic circuits of the Boolean expressions given below.

(i) $Y = A \cdot B + B \cdot C + \overline{A \cdot C}$

(ii) $Y = A \cdot B \cdot C + \overline{A \cdot B} + \overline{B \cdot C}$

(iii) $Y = \overline{(A + C + B)} \cdot \overline{(ACB)}$

6. Apply De Morgan's Laws to the following expressions.

$\overline{(A+B)}\overline{B}$, $\overline{(A+B)}.\overline{C}$, $\overline{\overline{A \cdot B} + \overline{C \cdot D}}$

14.9 TEXT AND REFERENCE BOOKS

TEXT BOOKS

1. Integrated Electronics by Millman and Halkias
2. Principles of Digital Electronics by Malvino and Leach
3. Basic Electronics and Linear Circuits - Bhargava etc

REFERENCE BOOKS

1. Electronics fundamentals by JD Ryder (PHI)

2. Digital Electronics by William H.Gothman

3. Principles of Digital Electronics – Malvino & Leach (Tata - McGraw Hill Publishers)
4. Digital Computer Electronics – Albert Paul Malvino. (Tata - McGraw Hill publishers)

UNITIV LESSON– 15

COMBINATIONAL LOGIC CIRCUITS

OBJECTIVES OF THE LESSON

To learn about 1) various logic families 2) binary addition 3) the working of various combinational logic circuits like adders, decoders, de-multiplexers, data selectors, multiplexers.

STRUCTURE OF THE LESSON

15.1 INTRODUCTION

Basic logic gates are the building blocks of logic systems like digital computers. In digital computer performs arithmetical operations using binary number system. Further any arithmetic operations like subtraction, multiplication and division can be expressed in the terms of binary addition. In this lesson we learn basic concepts of binary additions using logic gates. Various logic gates are combined to generate a complex logical operation and if these circuits are made to work independent of time, such circuits are called simply combinational logic circuits. If these logic circuits are made to work with time as a parameter these circuits are called sequential logic circuits. General logic

circuits may be combinational and sequential logic circuits. In this lesson learn about some combinational logic circuits.

Binary codes are used to spec , instructions, addresses and coded data. One binary digit (bit) can stand for two codes 0 or 1. with two bits we can have four codes namely 00, 01, 10, 11. Similarly with n bits we can form 2^n codes. Circuits that generate these codes are called encoders. It becomes necessary not only to code information but also to decode the codes whenever necessary. Circuits which decode are called decoders.

Information coming on several channels may have to be rooted on a single channel. This is called multiplexing and circuits which do this are called multiplexers. Multiplexed information coming on a single channel has to be separated and sent and varies channels and this is called de-multiplexing. In this lesson we learn about these combinational logic circuits also.

15.2 LOGIC FAMILIES

A number of logic families are designed for different operating conditions.. Important logic families are

1) Resistance Transistor logic (RTL)

2) Diode Transistor logic (DTL)

3) Transistor- transistor logic (TTL)

4) Metal oxide semiconductor logic (MOS)

Resistance Transistor Logic (RTL): It is one of the early logic families developed. It offers high performance but has low noise margins.

Diode Transistor Logic (DTL): It had better noise margins and larger fan-out but was slow.

Transistor- Transistor Logic (TTL): It provides greater operating speed than DTL and has a good fan-in and fan – out and is easy to interface with other digital circuitry.

Metal Oxide Semiconductor logic (MOS): Instead of bipolar junction transistors, if we use MOSFETS to form logic circuits, we get MOS logic family. There are several varieties of sub families in it. Important of them are PMOS, NMOS, CMOS. CMOS has the lowest power dissipation and high fan-out. They can be fabricated into high packing density for a given chip area. i. e large number of circuits can be placed on a single chip.

15.3 TTL LOGIC: The basic circuit of the TTL family is a NAND gate. Fig 15.1 shows aa modified version known as totem-pole circuit because the three output components Q_3,Q_4 and D are stacked one on top of the other in manner of a totem pole. This

arrangement of totem-pole configuration increases the operating speed and output current capability of the circuit. The function of the diode D in this circuit is to prevent both Q_3 and Q_4 are ON at the same time. If both Q_3 and Q_4 are ON simultaneously, supply circuit then sends a large current to ground which may cause a spike voltage drop on the V_{CC} line and a large noise in the output. It may also cause large power consumption.

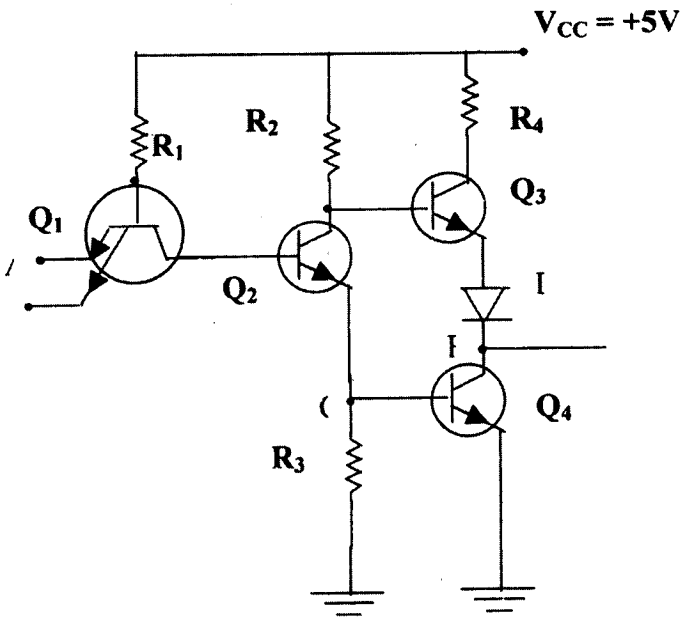


Fig.15.1 TTL NAND gate

Circuit operation:

Case 1: When input is high

When inputs are high (logic 1) , transistor Q_1 is OFF, Q_2 is ON , Q_3 is OFF and Q_4 is ON and therefore, output becomes low (logic 0)

Case 2 When input is low

In this case, any of the two inputs or both are low (logic 0), then the emitter-base junction of Q1 is forward biased anf hence Q_1 is turned ON. Then the potential of its collector (point A) falls. It turns Q_2 OFF. Then emitter of Q_2 and hence base of Q_4 are grounded. Thus Q_4 is also turned OFF. But point B is at V_{CC}, hence it turns Q_3 ON. The potential of point E = V_C - potential drop across (R_3+Q_3+D) ≈ V_{CC} because the potential drop across R4, Q3 and D is not too much.

15.4 CMOS NOR circuit: Fig.15.2 shows a CMOS NOR circuit. It has two N-channel MOSFETS Q_1 and Q_2 and two p-channel MOSFETS Q_3 and Q_4 . A and B are two inputs which switch between +V_{DD} (logic 1) and

Ground (logic 0).

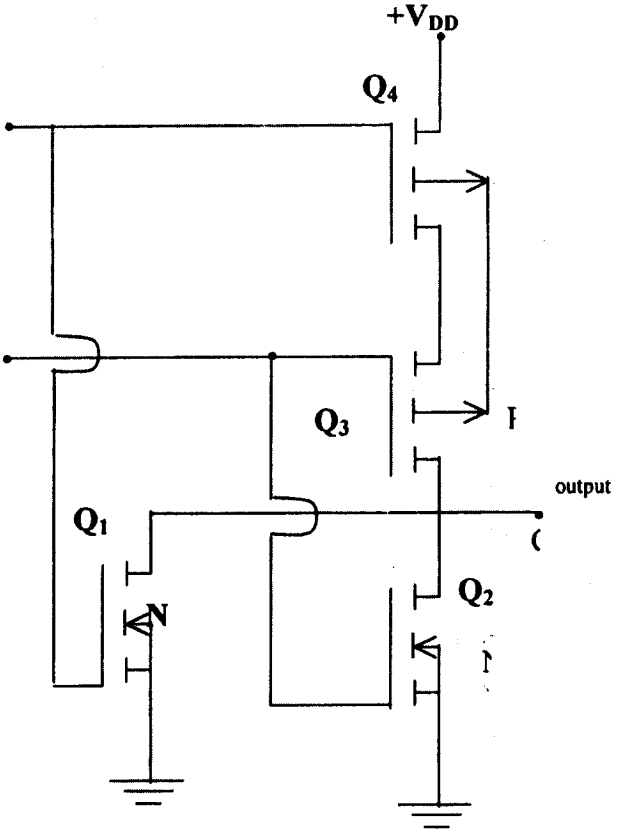


Fig.15.2 CMOS NOR gate

Circuit operation

If inputs A and B have positive voltage, A = B = logic 1, then Q_1 and Q_2 will be ON so that they will act as closed switches but Q_3 and Q_4 will be OFF. So that they will act as open switches. Therefore, output C is logic 0.

When A = B = 1 , C=0

If either of the inputs A and B has positive voltage i.e., either A or B is at logic1, then associated N-channel MOSFET (Q_1 or Q_2) will be OFF. Consequently, either Q_3 or Q_4 will act as open switch. and the output C will be at logic 0.

When A = 1 B = 0, C = 0

A = 0 B = 1, C = 0

If both the inputs are at logic 0, then Q_1 and Q_2 will be OFF but Q_3 and Q_4 will be ON. Since the voltage across an open equals the applied voltage, C will be at logic 1.

15.5 BINARY ADDITION

When we perform binary addition and subtraction, the following rules must be followed.

Binary addition	Binary subtraction
0 + 0 = 0 → (1)	0 – 0 = 0 borrow 0
0 + 1 = 1 → (2)	0 – 1 = 1 borrow 1
1 + 0 = 1 → (3)	1 – 0 = 1 borrow 0
1 + 1 = 15 → (4)	1 – 1 = 0 borrow 0
1 + 1 + 1 = 11 → (5)	

In binary addition, the first three operations produce a sum with only one digit, but when both augend and added bits are equal to 1, the binary sum consists of two digits. The higher significant bit of this result is called a carry.

15.6 HALF ADDER

A combinational circuit that performs the addition of two – bits is called a Half – adder. The Half – adder has two binary inputs and two binary outputs.

This is 2 – bit adder. This circuit is called half – adder because it cannot accept a carry – in from previous additions. The inputs to the circuits are the addend and augend bits. The outputs produced by it are sum (s) and carry (c). The half adder can be constructed by using one AND gate and an EX – OR gate. Fig 15.3(a) shows logic circuit that adds 2 bits namely A and B.

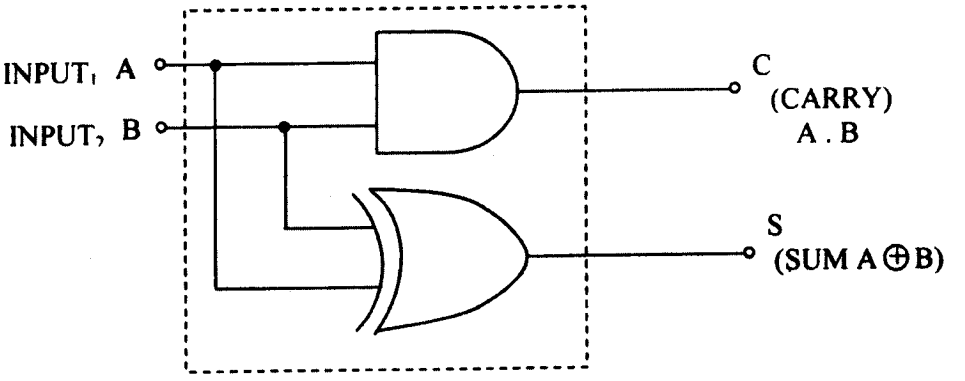


Fig.15.3(a) Half-Adder Logic circuit

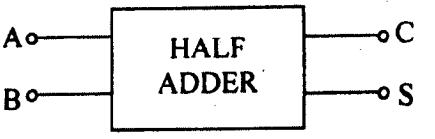


Fig.15.3 (b) Half – adder Logic symbol

Half – adder Truth table

A	B	Carry C	Sum S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Fig 15.3 (c)

15.7 FULL ADDER

A full adder is combinational circuit that forms the arithmetic sum of three input bits. The two significant bits to be added are denoted as A and B, where as the third input C represents the carry from the previous lower significant position. The full adder can be constructed from two half adders and one OR gate as shown in Fig.5.4(a). And its symbol is shown in Fig.15.4(b).

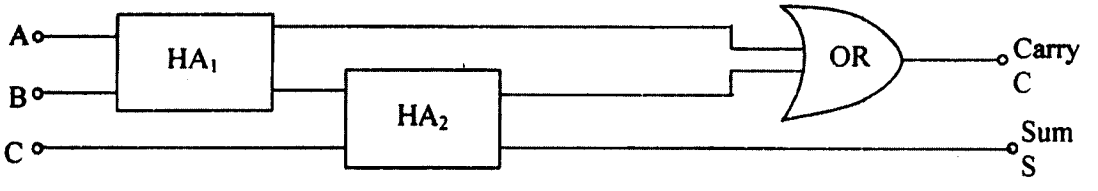


Fig.15.4(b): Full – adder Logic Symbol

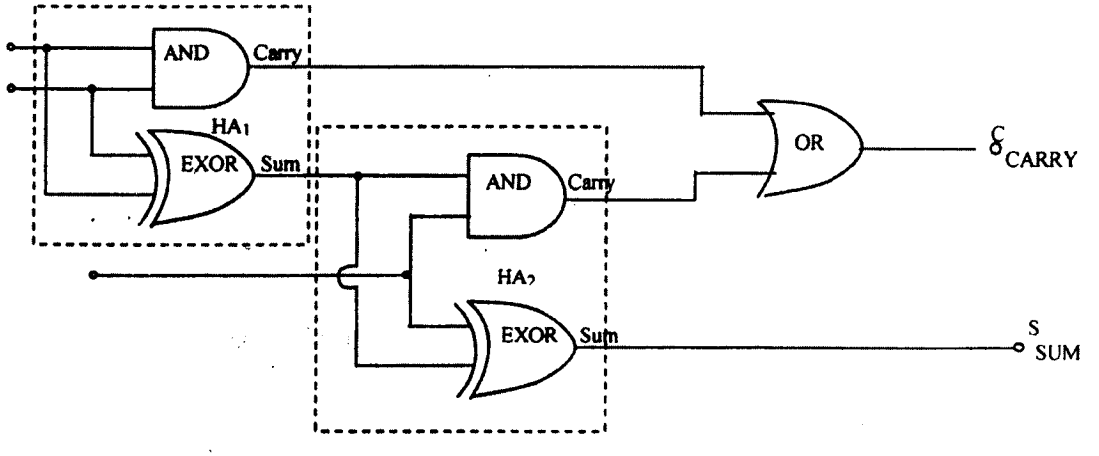


Fig.15.4a Full – adder Logic diagram

INPUTS			OUTPUTS	
A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Fig.15.4 (c) Full – adder Truth Table

15.8 Binary four bit parallel Adder:

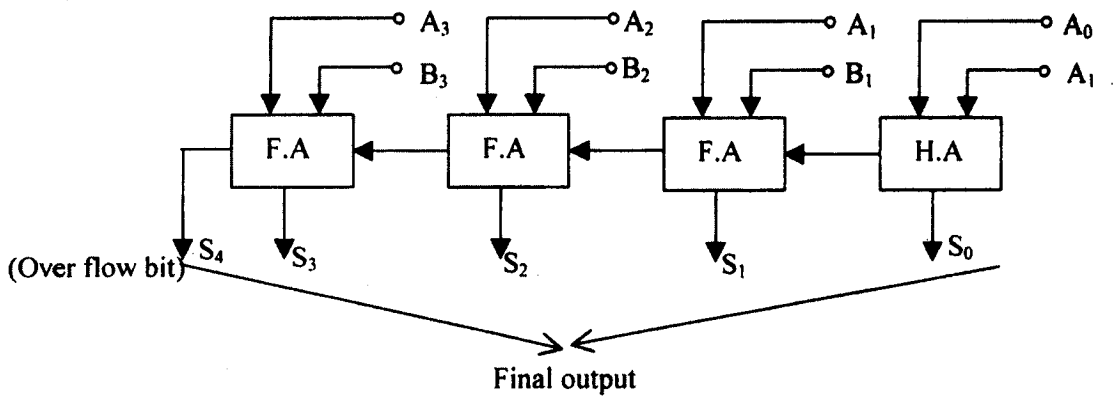


Fig.15.5

Note: In binary, the count starts from zero rather than from 1. The first bit is called S_0 rather than S_1. Similarly the nth bit is S_{n-1}.

A parallel adder produces the arithmetic sum of two n-bit binary numbers in parallel. This can be constructed by using one half adder and several full adders. The full adders are connected in cascade, with the output carry from one full adder connected to the input carry of the next full adder.

Fig.15.5 shows the logic diagram for 4-bit parallel adder circuit.

Suppose we want to add 4-bit binary numbers $A_3\ A_2\ A_1\ A_0$ and $B_3\ B_2\ B_1\ B_0$ then we get a sum $S_4\ S_3\ S_2\ S_1\ S_0$ where S_4 indicates overflow bit if the sum exceeds four bits. For adding the above two 4-bit numbers, we require three full adders and a half adder

connected in parallel. The output (carry) of each adder is connected to next adder to get a parallel adder.

15.9 DECODER

A decoder is a combinational circuit that converts binary information from 'n' input lines to a maximum of 2^n unique output lines. Decoders are available with several output configurations: active low voltage, high-sink current for direct driving of indicator lamps. Output voltage ratings range from +5V to over +150V. The decoder is used in conjunction with some code converters such as a BCD – to – 7 segment decoder, BCD – to – Decimal decoder. The decoder presented here is called n – to 2^n line decoder. Its purpose is to generate the 2^n min terms of n input variables. These decoders form a combinational circuit with n input variables and 2^n output variables. For each binary input combination of 1s and 0s, there is one and only one output line that assumes the value of 1. Figure 15.6(a) shows a 2 by 4 decoder. It has four AND gates and two inverters.

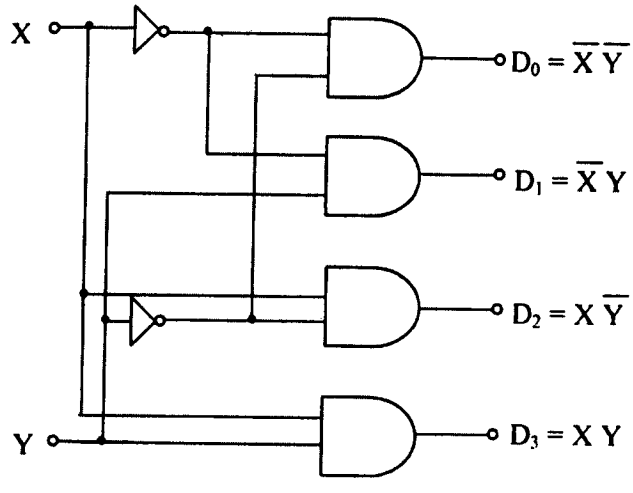


Fig.15.6(a) 2 – bit decoder

X	Y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Fig.15.6(b) 2- bit decoder Truth table

Some times an enable input may be included with a decoder to control the circuit operation. In this, all outputs will be equal to 0, if the enable input is zero. When the

enable input is 1, the circuit operates as a conventional decoder. Block diagram of a 3 to 8 decoder with enable signal is shown in Fig.15.7.

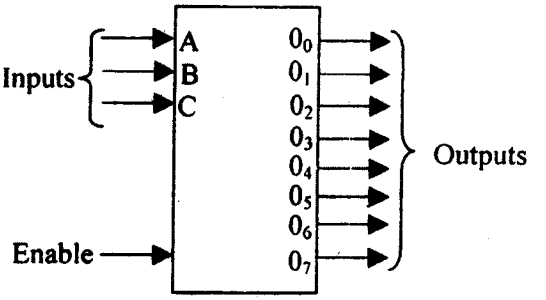


Fig.15.7 Block diagram of 3 to 8 bit decoder

15.10 DEMULTIPLEXER

A demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of a specific output line is controlled by the bit values of n selection lines. Figure 15.8 shows the block diagram of decoder and demultiplixer. The decoder with an enable input can function as a demultiplexer.

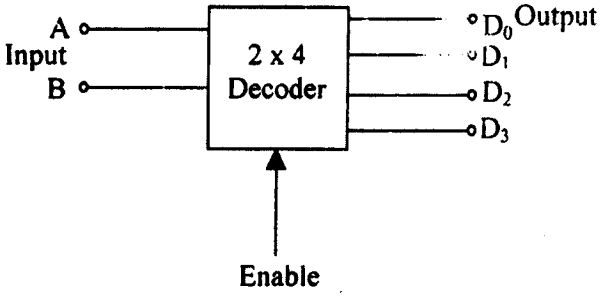


Fig.15.8(a)

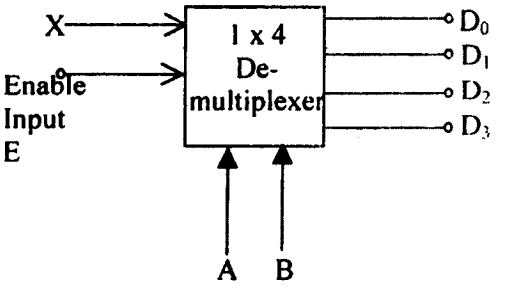


Fig.15.8(b)

The decoder of Fig 15.8(a) can function as a demultiplexer if the enable line is taken as a data input line and lines A and B are taken as the selection lines as shown in Fig 15.8(b). Out of 4 output lines, one gets link with input E depends upon the binary value

of two selection lines A and B (i.e), if AB = 01, D_1 gets connected with the input E, so that input is available at D_1 output while all other outputs are maintained at 1.

15.11 ENCODER

An encoder is a digital circuit that produces a reverse operation from that of a decoder. An encoder has 2^n input iines and n output lines. The output lines generate the binary code for the 2^n input variables. One of the encoders is shown in Fig.15.9(a). It has eight inputs, one for each of the eight digits and three outputs that generate the corresponding binary outputs that generate the corresponding binary number.

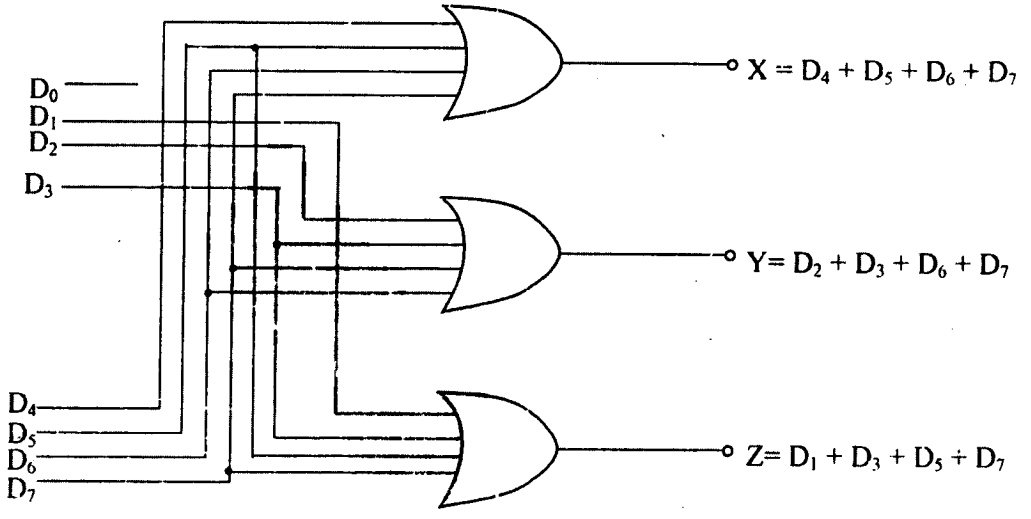


Fig.15.9(a)

INPUTS								OUTPUTS		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Truth table 15.9(b)

Fig.15.9(a) shows the octal to binary encoder. It is constructed with OR gates. It, has 8 input lines and could have 2^8 = 256 possible input combinations. Only eight of these combinations have meaning and others are don't care conditions. The output z is 1, if the input digits are odd. Output Y is 1 for octal digits 2, 3, 6 and 7. Output X is 1 for digits 4, 5, 6 or 7. It is 1 at any time. Do is not connected to any OR gate. It arises that only the highest priority input line is encoded.

15.12 Multiplexers / Data selector

It is a combinational circuit which selects binary information from one of many input lines and directs it to single outputs line. The selection of a particular input line is controlled by a set of selection lines. For 'n' bits, there are 2^n input lines and n selection lines whose bit combinations determine which inputs is selected. This means "many into one". It is used when a complex logic circuit is to be shaved by a number of input signals. Fig 15.10 shows the logic diagram, block diagram and function table of a 4 to 1 line multiplexer.

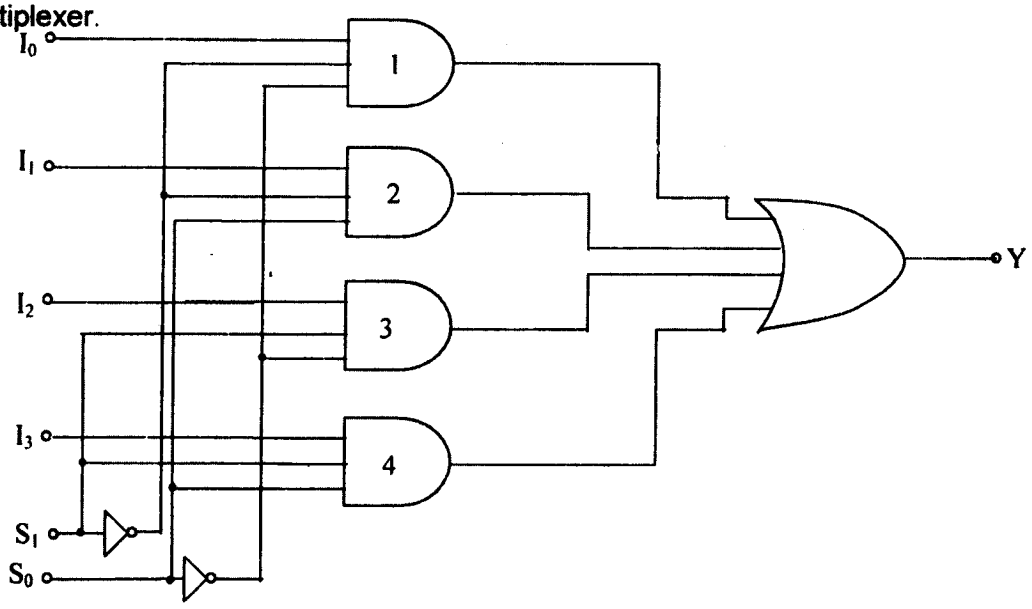
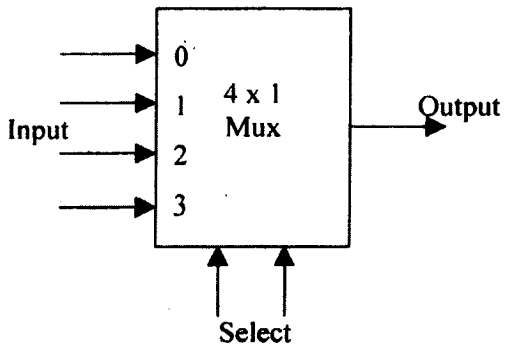


Fig 15.10(a): 4 to 1 Multiplexer

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Fig 15.10(b)



Fit 15.10(c)

A line to 1 line multiplexer has 4 inputs I_0 to I_3 and one output line. Each of the four input lines is applied to one input of a three input AND gate. The remaining two inputs of it is supplied by selection lines S_1 and S_0.

Based on the combination of S_1 and S_0, the input associated with the selected AND gate finds out the path to reach the output through OR gate. For example: when S_1S_0 = 01, it selects the AND gate 2. So the input I_1 is transferred to the output i.e OR gate output is now equal to the value of I_1. thus providing a path from the selected input to the output. The remaining AND gates have at least one input equal to 0.

As in decoders, multiplexer IC has an enable input (or) storbe input to control the operation of the unit. It can also be used to expand two or more multiplexers to a digital multiplexer with a large number of inputs.

15.13 SUMMARY

Logic circuits can be either combinational or sequential. The five basic gates (OR, AND, NOT, NAND, NOR) and their combinations – half, full and parallel adders are known as combinational logic circuits. Here there is no feedback. These have no memory elements. Their output only depends upon their present input. Thus can operate as fast as the devices of which they are made. Half and full adders are bit adders, where as parallel adder is an adder of two n – bit word. The function performed by a multiplexer is to select 1 out of N input data sources and to transmit the selected data to a single information channel. A multiplexer performs the increase process of a demultiplexer. A decoder is a system which 1 on one (and only one) of 2^m output lines. In other words, a decoder recognizes a particular code, A decodes with an enable input can function as a demultiplexer. An encoder produces reverse operation from that of a decoder. The combinational logic circuits are mainly employed in ALUs.

15.14 KEY TERMINOLOGY

Binary Adder: A logic circuit that can add two binary numbers.

Half Adder: A logic circuit that adds 2 bits.

Full Adder: A logic circuit than can add 3 bits.

Over flow: As the sum or difference that of lies outside the normal range.

ALU: ALU stands for arithmetic logic unit. It performs arithmetic one logic operations.

Encoding: The process of generating binary codes.

Decoding: The reverse process of encoding.

Demultiplexer: A combinational logic circuit, that accepts a single input and sends it to 1 out of N output lines which is selected by select lines.

15.15 SELF – ASSESSMENT QUESTIONS

1) Explain a binary addition. Give examples.
2) What is a full adder? How it adds three bits?
3) Draw a full adder circuit, without using half adders.
4) Construct a 5-bit parallel adder.
5) Implement a full adder circuit with multiplexers.
6) Explain the working of half and full adders.
7) Explain TTL and CMOS logic families and mention where they are used.
8) Draw the circuit diagram of a TTL NAND gate with totem pole output and explain its operation.
9) Draw the Half adder and Full adder circuits and explain them with suitable truth tables.

15.16 TEXT AND REFERENCE BOOKS

TEXT BOOKS

1. Integrated Electronics by Millman and Halkias
2. Principles of Digital Electronics by Malvino and Leach
3. Basic Electronics and Linear Circuits - Bhargava etc

REFERENCE BOOKS

1. Electronics fundamentals by JD Ryder
2. Digital Electronics by William H.Gothman
3. Principles of Digital Electronics – Malvino & Leach (Tata - McGraw Hill Publishers)
4. Digital Computer Electronics – Albert Paul Malvino. (Tata - McGraw Hill publishers)

SEQUENTIAL LOGIC CIRCUITS

(Flip – Flops, Registers and counters)

OBJECTIVES OF THE LESSON: This lesson explains you the concept of (i) Flip – Flops (ii) Different types of Flip Flops (iii) Shift Registers and (iv) Synchronous and asynchronous counters.

STRUCTURE OF THE LESSON

INTRODUCTION

The logic circuits whose present output depends on the past inputs are known as sequential logic circuits. These circuits store and remember information. The sequential circuits unlike combinational circuits are time dependent. Normally the current output of

a sequential circuit depends on the previous state of the circuit and on the current input to the circuit. It is a connection of flip-flops and gates. What is a flip-flop? You will find the answer in this section. There can be two types of sequential circuits.

- Synchronous
- Asynchronous

Synchronous circuits use flip-flops and their status can change only at discrete instants. The Asynchronous sequential circuits may be regarded as combinational circuits with feedback path. Since the propagation delays of output to input are small they may tend to become unstable at times.

The synchronization in sequential circuits can be achieved using a clock pulse generators. A clock synchronizes the effect of input over output. It presents a signal of the following form:

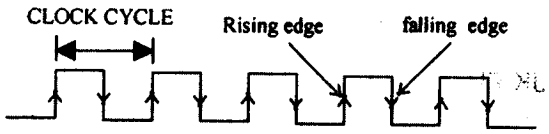


Fig.16.1 Clock signal of a Clock Pulse Generator

The signal produced by clock generator is in the form of clock pulse or clock signal. These clock pulses are distributed throughout the computer system for synchronization.

A clock can have two states, an enable or active state, otherwise a disable or inactive state. Both of these states can be related to zero or one levels of clock signals. Normally, the flip-flops change their state only at the active state of the clock pulse. In certain designs the active state of the clock is triggered, when transition from 0 to 1 or 1 to 0 is taking place in clock signal.

16.1 Flip-flop

A flip-flop is a binary cell, which can store a bit of information. It itself is a sequential circuit. A flip-flop maintains any one of the two stable states that can be treated as 1 or 0 depending on the presence or absence of output signal. The state of flip-flop can only change when clock pulse has arrived. Let us first see the basic flip – flop or a latch.

16.2 S-R Latch

The most fundamental circuit in the group of flip-flops is the S-R (set-reset) latch The basic S-R latch has two NAND gates connected back – to – back. Fig 16.2 shows, such an S-R latch. The truth table of the S-R latch is given in Table 16.1. It describes

the conditions of the flip-flops at times t_0 and t_1. The state at $t = t_0$ is called the present state (PS) and the state at $t = t_1$ is called the next state (NS).

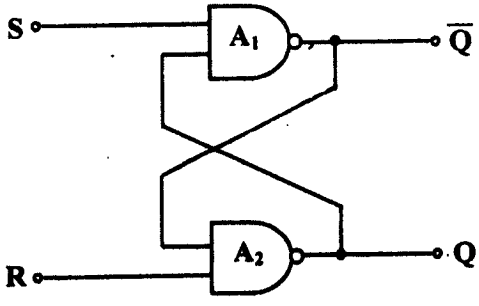


Fig 16.2 Circuit diagram of the S – R latch.

The S – R latch has two external inputs S and R, and two feed – back inputs Q and $\overline{Q}$. The present states of the inputs are S_0, R_0 and Q_0. After one clock pulse, the output will change to the next state Q_1. This changed value of the output will be the new present state of the input.

For testing the validity of the circuit, we have to test eight states corresponding to the three inputs. So, R_0 and Q_0. These states are tested by using fig 16.2 and table 16.1

Table 16.1 Truth Table of S – R latch

Present state (PS)			Next state (NS)
S_0	R_0	Q_0	Q_1
0	0	0	Not permitted
		1	
0	1	0	Reset to 0
		1	
1	0	0	Set to 1
		1	
1	1	0	0 } Q_0
		1	1 }

We shall test the outputs for the conditions: S = R = 0; S=0, R=1; S=R=1. In each of these cases, we test the state of the latch for the conditions of Q = 0, and Q = 1 respectively.

Case(i): We find that when S = R = 0 both Q and $\overline{Q}$ become 1. But this is not allowed because we want Q and $\overline{Q}$ to be complementary outputs. This state is designated as the ***forbidden state.***

Case (ii): In S = 0, R = 1 case, when S = 0, output of NAND gate A_2, i.e., $\overline{Q}$ becomes 1. Now the inputs to gate A_1. i.e., R and $\overline{Q}$, both become 1, which make its output, Q = 0. This is called the reset (to 0) state.

Case (iii): In S = 1, R = 0 case, when R = 0, A_1 produces an output of 1 i.e., Q = 1. Now, both the inputs to A_2 are 1, which makes $\overline{Q}$ = 0. This state (S = 1) making Q equal to 1 is called the set (to 1) state.

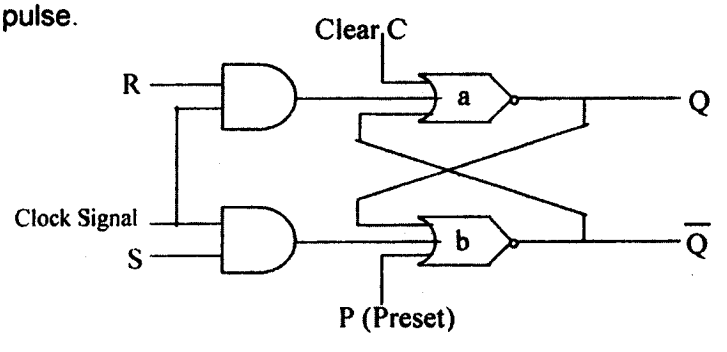
Case (iv): In S = 1, R = 1 case, both the inputs are equal to 1 . It will not produce any change in the output. Hence, for these cases, the outputs will remain as such in their previous states. This means that the present state and the next state are one and the same.

Using fig 16.2; we have described the behavior of a bi-stable multi-vibrator using NAND gates for all possible input states. Table 16.1 represents the truth table of the S-R latch. The behavior of the circuit shows that it will remain in one of the two states (i.e. 0 or 1) till an externally applied trigger pulse produces a transition in the output from 0 to 1, or 1 to 0. Thus, the circuit is able to store one bit of information in its memory. Therefore, this flip-flop is called a memory cell, we shall now discuss the clocked S-R Flip-Flop.

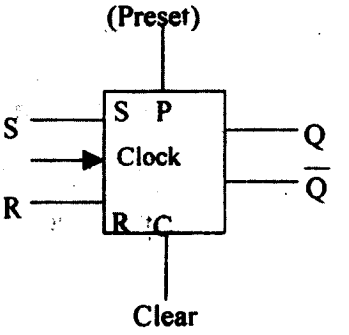
16.3 CLOCKED R-S FLIP – FLOP

The main feature in R-S Flip-Flops is the addition of a clock pulse input. In this flip-flop change in the value of R or S will change the state of the flip-flop only if the clock pulse at that moment is one. It is shown in fig 16.3a.

The excitation or characteristic table basically represents the effect of S and R inputs on the state of the flip-flop, irrespective of the current state of flip-flop. The other two inputs P(present) and C(clear) are asynchronous inputs and can be used to set the flip-flop or clear the flip-flop respectively at the start of operation, independent of the clock pulse.



16.3(a) Logic Diagram



16.3(b) Symbolic representation

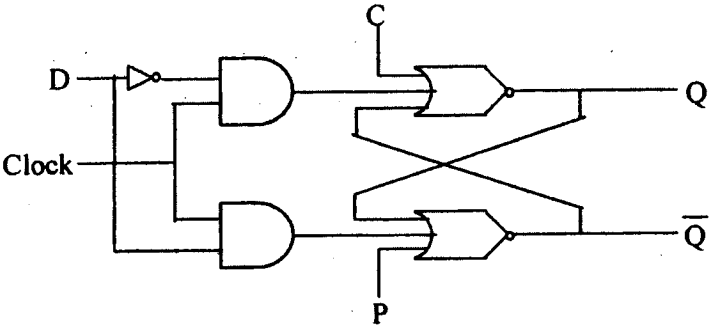
Input S	Input R	State on completion of clock cycle
0	0	No change in State
0	1	Clear the flip – flop (state 0)
1	0	Set the flip – flop (state 1)
1	1	Undesirable (Not allowed)

Fig 16.3(c) Characteristic table.

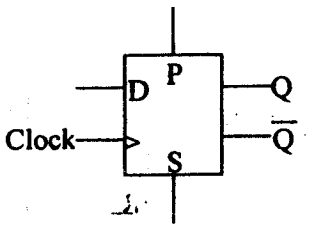
Fig 16.3: R – S flip – flop

16.4 D FLIP – FLOP

D flip-flop is a special type flip-flop and it represents the currently applied input as the state of the flip-flop. It can store 1 bit of data information and sometimes refers to as Data flip-flop. The state of flip-flop changes with the applied input. It does not have a condition where the state does not change as the case in RS flip-flop, the state of R-S flip-flop does not chan when S = 0 and R = 0. If we want that for a particular input state does not change, then either the clock is to be disabled during that period or a feedback of the output can be embedded with the D- flip-flop is also known as Delay Flip-Flop because it delays the 0 or 1 applied to its input by a single clock pulse.



16.4(a) Logic Diagram



16.4(b) Symbolic representation

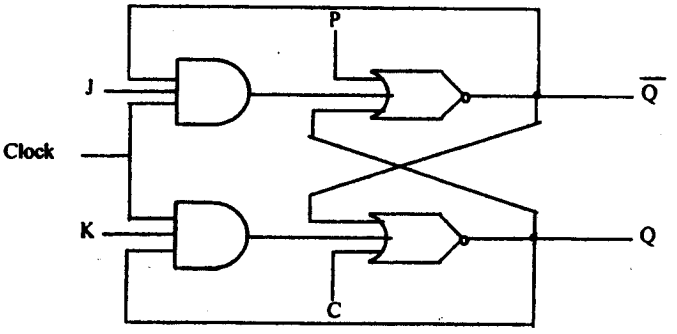
Input D	State on completion of clock cycle
0	0
1	1

Fig 16.4(c) Truth table of D-Flip-Flop.

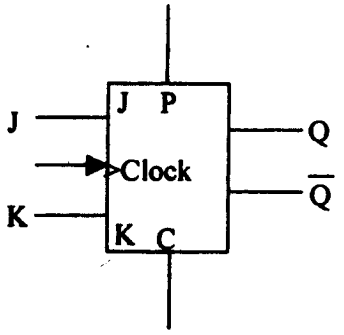
Fig 16.4: D flip – flop

16.5 J-K FLIP – FLOP

It is not possible to achieve toggling (changing the state of the output wherever the input makes a transition from 1 to 0) with the simple flip-flops described above. By using NAND gates, one can construct a flip-flop that toggles. The symbol and truth table of one such circuit, called J-K flip-flop are shown in fig 16.5



16.5(a) Logic Diagram



16.5(b) Symbolic representation

Input J	Input K	State on completion of clock cycle
0	0	No change in State
0	1	Clear the flip –f lop (state 0)
1	0	Set the flip – flop (state 1)
1	1	Complement the state of flip - flop

Fig 16.5(c) Truth table.

Fig 16.5: J – K flip – flop

A JK flip-flop is a refinement of the SR flip-flop in that the indeterminate condition of the SR type defines in the JK type. An examination of the truth table given in fig 16.5(a) reveals the following properties of the JK flip-flop.

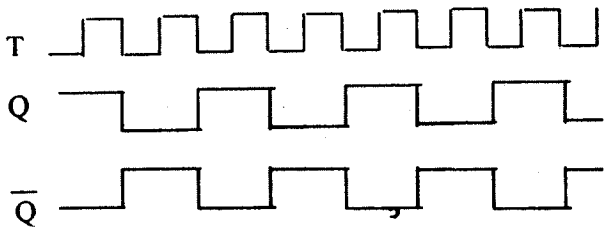
a) It retains its present state if J = 0 and K = 0

b) If J = 0, K = 1, Q = 0, it resets to zero

c) If J = 1, K = 0, Q = 1, it sets

d) If J = 1, K = 1, it Toggles.

If the first clock pulse leaves Q = 1 and $\overline{Q}$ = 0 the second clock pulse make Q = 0 and $\overline{Q}$ = 0. The third clock pulse make Q = 1 and $\overline{Q}$ = 0 again and so on as shown

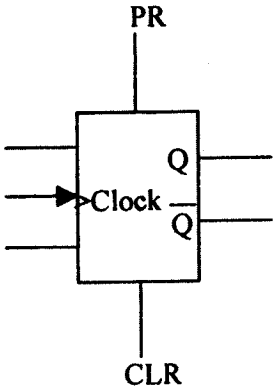


Relation between clock pulses and output JK flip-flop. When J = 1 and K = 1.

Please note Q = 1 once in every two clock pulses i.e., the output has half the frequency of the clock pulse. This property is utilized in binary counters.

Preset and Clear Inputs:

Usually, the J-K flip – flop works on the basis of the clock input. However, we can introduce two inputs called the PRESET and CLEAR in the last NAND level. As shown in fig 16.6(a) these inputs do not obey the clock pulses, and override them in action. Hence, they are called the asynchronous inputs. The working of these inputs is as given below.



16.6(a) Symbolic representation

PR	CLR	Q_0	Q_1
0	0	Forbidden	operations
0	1	0/1	1
1	0	0/1	0
1	1	Normal	operations

Fig 16.6(b) Truth table.

Fig.16.6 J – K flip – flop

Let PR = 0 and CLR = 1. Then, as and when PR = 1 and CLR = 0, Q will jump to 1 from whatever state it is in. This operation presets $\overline{Q}$ to 1. When PR = 1 and CLR = 0, the lower NAND produces 1 at its output, i.e., $\overline{Q}$ = 1. This makes Q = 0. Thus whatever be the state, Q will fall back to '0'. When both PR = CLR = 1, the NANDs are enabled and the J-K flip-flop functions in the normal way. However, the state PR = CLR = 0 is forbidden, since both Q and $\overline{Q}$ will be 1 in this state. The truth table for the PR and CLR terminals is as shown in Table 16.6a. fig 16.6b shows the symbol of J-K flip-flop.

RACE – AROUND CONDITIONS

Consider the last two rows of the truth table of the J-K flip-flop, where both the J and K inputs are connected to logic-1 state. We find that when J = K = 1, Q_0 changes to $\overline{Q}_0$. That is, if $Q_0 = 0$, $Q_1 = 1$, and if $Q_0 = 1$, $Q_1 = 0$. These transitions gives rise to what is called the race-around problem. When J = K = 1 and CK = 1 the output will toggle from '0' to '1', and 1 to 0 continuously, until the clock pulse becomes zero. The result of this toggling action is that when the clock finally becomes zero, we will not know in what state Q would be. This is called race-around problem, as it is generated due to the racing of this signal around the feedback path, and around the circuit.

16.6 Master – Slave JK Flip – Flop (Solution to the Race-Around Problem):

The race around problem can be solved using two J-K flip-flops in the master-slave mode of operation. Here two S-R flip-flops are in the J-K mode of operation. The first flip-flop in the 'master' and the second one is the 'slave'. The master is converted into J-K mode of operation.

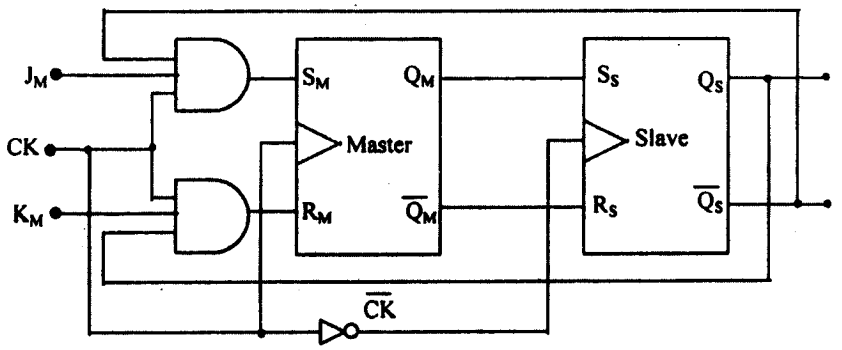


Fig 16.7 J – K master –slave flip – flop.

The slave inputs are connected to the outputs of the master. In this mode, the slave will also act as a J-K Flip – Flop. The Master is driven by clock pulse CK, while the slave is driven by $\overline{CK}$, which is obtained by inverting the CK pulses. The feedback connection can be seen to be from the Slave outputs to the master inputs.

(i) When the clock is ON, the master gets enabled and the slave gets disabled. So, the inputs appearing at input terminals S_M and R_M of the master will

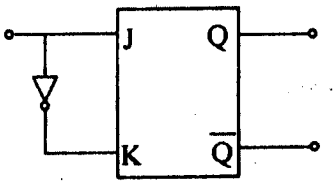
appear at its outputs Q_M and $\overline{Q}_M$. respectively, which means that the external inputs now appear at the inputs S_s and R_s of the slave.

(ii) When the CK = 0, the master is disabled, and the slave is enabled because $\overline{CK}$ = 1. Thus the inputs at S_s and R_s will appear at Q_s and $\overline{Q}_s$, respectively, and hence at the inputs J_M and K_M of the master. However, as the master is now disabled, these inputs will not appear at S_s and R_s. Hence, no feedback problem occurs. Thus, the race-around problem is eliminated.

16.7 Applications of JK Flip – Flop:

a) JK Flip - Flop as D-Flip - Flop

The 'D' flip-flop has only one input, called the delay – or D – input. The truth table will have only four entries, as shown in fig 16.8b. when D is 0, Q will become '0' after the propagation delay t_p. similarly, if D = 1, output will become 1, irrespective of the previous value of the output. We thus find that the flip-flop will always produce an output equal to the input, after a time – delay equal to t_p. By cascading a number of D- Flip - Flops, the delay time can be increased.



16.8(a) D flip – flop.

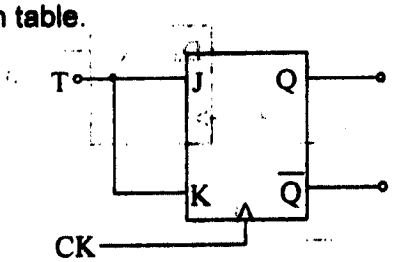
D_0	Q_0	Q_1
0	0	0
0	1	0
1	0	1
1	1	1

Fig 16.8(b) Truth Table of the D flip – flop.

Since the circuit output is produced after a time-delay, this is called the delay flip-flop. It is also called the D latch.

b) JK Flip-Flop as T-Flip- Flop

By shorting the J and K terminals, we can construct a T Flip-Flop. Usually, the T – input is tied to logical 1 . Fig 16.9a shows the circuit of the toggle flip-flop and fig 16.9b shows its truth table.



16.9(a) Toggle flip – flop.

T_0	Q_0	Q_1
0	0	0
0	1	0
1	0	1
1	1	1

Fig 16.9(b) Truth Table of the T flip – flop.

Table shows that, when T = 0, $Q_1 = Q_0$. However, if T = 1, $Q_1 = \overline{Q}_0$. T flip – flops are useful in the construction of counters.

16.8 SHIFT REGISTER

Shift registers are very important in applications involving the storage and transfer of data in digital system. A register, in general, is used solely for storing and shifting data (1s and 0s) entered into it from all external source and possesses no characteristic internal sequence of states. The storage capability of a register is one of its two basic functional characteristics and makes it an important type of memory device.

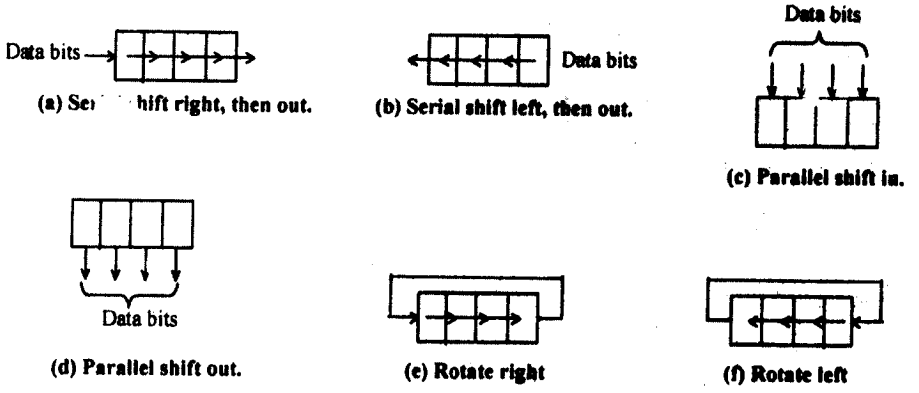


Figure 16.10 Basic data movement in registers.

Registers are commonly used for the temporary storage of data within a digital system. The shift capability of a register permits the movement of data from stage to stage within the register or into or out of the register upon application of clock pulses.

Fig.16.10 shows symbolically the types of data movement in shift register operations. The block represents any arbitrary four-bit register, and the arrow indicates the direction and type of data movement.

16.9 Serial In – Serial out Shift Register:

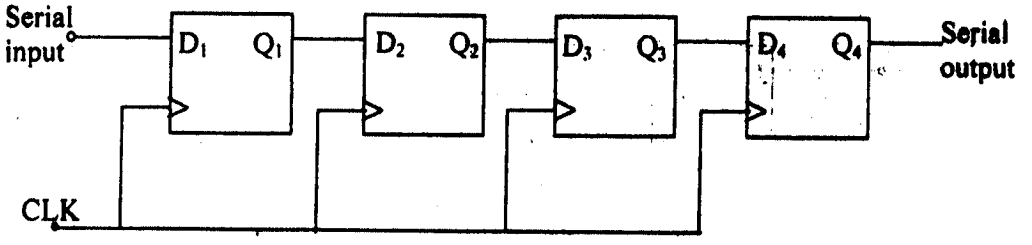


Figure 16.11 4 – bit serial – in, serial – out, shift register

This type of shift register accepts data serially, i.e. one bit at a time, and also outputs data serially. The logic diagram of a 4 – bit serial – in, serial – out, shift register is shown in fig 16.16. with four stages, i.e., four flip –flops, the register can store up to four bits of data. Serial data is applied at the D input of the first Flip-Flop (FF). The Q output of the first FF is connected to the D input of the second FF, the Q output of the second FF is connected to the D input of the third FF and the Q output of the third FF is connected to the D input of the fourth FF. The data is outputted from the Q terminal of the last FF.

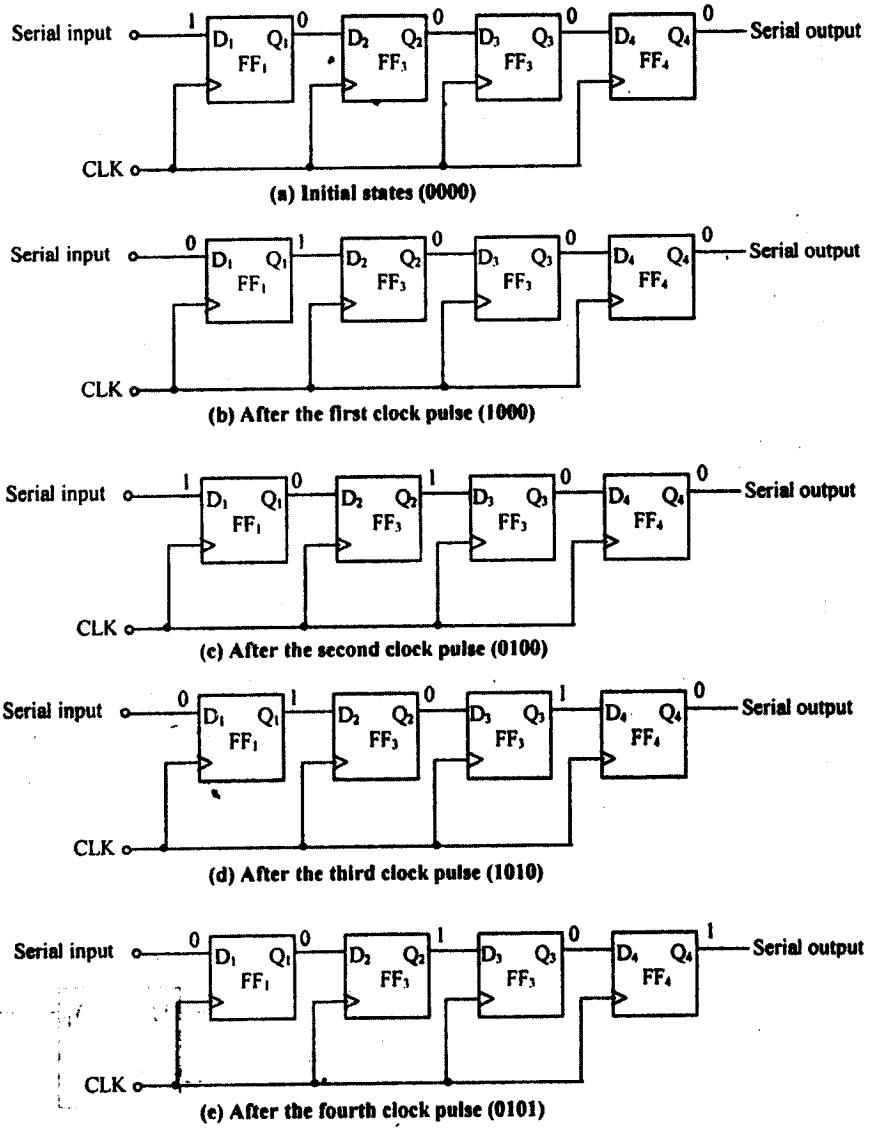


Fig16.12 Loading of the 4 – bit serial – in, serial – out, shift register

When serial data is transferred into a register, each new bit is clocked into the first FF at the positive – going edge of each clock pulse. The bit that was previously stored by the

first FF is transferred to the second FF. The bit that was stored by the second FF is transferred to the third FF, and so on. The bit that was stored by the last FF is shifted out.

Fig.16.12 and 16.13a illustrate this process to store the data bits 0101 in the register. Initially all the FFs are reset, i.e., $Q_1 = 0$, $Q_2 = 0$, $Q_3 = 0$ and $Q_4 = 0$.

Then a '0' is applied at the D_1 input of FF_1. At the positive – going edge of the second clock pulse, this '0' is shifted to Q_1 of FF_1 and the D inputs of all other FFs are also shifted to their respective outputs. Therefore $Q_1 = 0$, $Q_2 = 1$, $Q_3 = 0$ and $Q_4 = 0$, after the second clock pulse. The right most bit '1' is applied at the D_1 input of FF_1. At the positive – going edge of the first clock pulse, this '1' is shifted into FF_1 and all other FFs store their respective bits at the D inputs. Therefore, $Q_1 = 1$, $Q_2 = 0$, $Q_3 = 0$ and $Q_4 = 0$, after the first clock pulse.

Then a '1' is applied at the D_1 input of FF_1. At the positive – going edge of the third clock pulse, this '1' is shifted into Q_1 of FF_1 and the D inputs of all other FFs are also shifted to their respective outputs. Therefore, $Q_1 = 1$, $Q_2 = 0$, $Q_3 = 1$ and $Q_4 = 0$, after the third clock pulse.

Then a '0' is applied at the D_1 input of FF_1. At the positive – going edge of the fourth clock pulse, this '0' is shifted into Q_1 of FF_1 and the D inputs of all other FFs are also shifted to their respective outputs. Therefore, $Q_1 = 0$, $Q_2 = 1$, $Q_3 = 0$ and $Q_4 = 1$, after the third clock pulse, this '0' is shifted to Q_1 of FF_1 and the D inputs of all other FF_S are also shifted to their respective outputs. Therefore, $Q_1 = 0$, $Q_2 = 1$, $Q_3 = 0$ and $Q_4 = 1$, after the fourth clock pulse.

After clock pulse	Serial input	Q_1	Q_2	Q_3	Q_4	
0	1	0	0	0	0	Initial states
1	0	1	0	0	0	
2	1	0	1	0	0	
3	0	1	0	1	0	
4	–	0	1	0	1	

Fig 16.13(a) Shifting in the data 0101 serially.

This completes the serial entry of 0101 into the 4-bit register fig 16.13 shows the timing diagram of the loading of serial input 0101 into the 4-bit serial-in, serial-out, shift register.

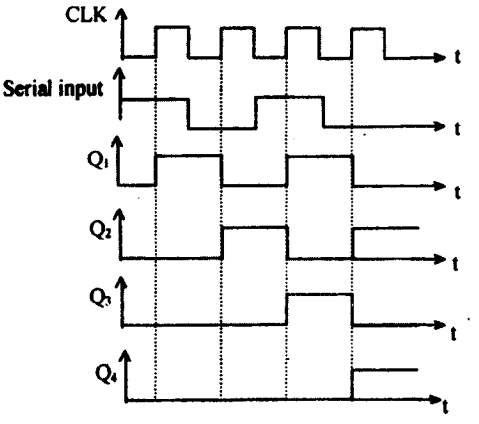


Fig 16.13(b) Timing diagram showing the loading of the serial input 0101 into the 4 – bit Serial-in, Serial-out, shift register.

The shifting out of the stored data 0101 serially from the register is illustrated in Fig. 16.14 . It requires four clock pulses to shift out the 4-bit stored data.

After clock pulse	Serial input	Q_1	Q_2	Q_3	Q_4
0	0	0	1	0	1
1	0	0	0	1	0
2	0	0	0	0	1
3	0	0	0	0	0
4	–	0	0	0	0

Fig 16.14 Shifting in the data 0101 serially.

16.10 Serial In, Parallel – out Shift Register

In this type of register, the data bits are entered into the register serially, but the data stored in the register is shifted out in parallel form. Fig 16.15 shows the logic diagram and the logic symbol of a 4-bit serial – in, parallel – out shift register.

Once the data bits are stored, each bit appears on its respective output line and all bits are available simultaneously, rather than on a bit-by-bit basis as with the serial output. The serial – in, parallel-out, shift register can be used as a serial-in, serial-out, shift register, if the output is taken from the Q terminal of the last FF.

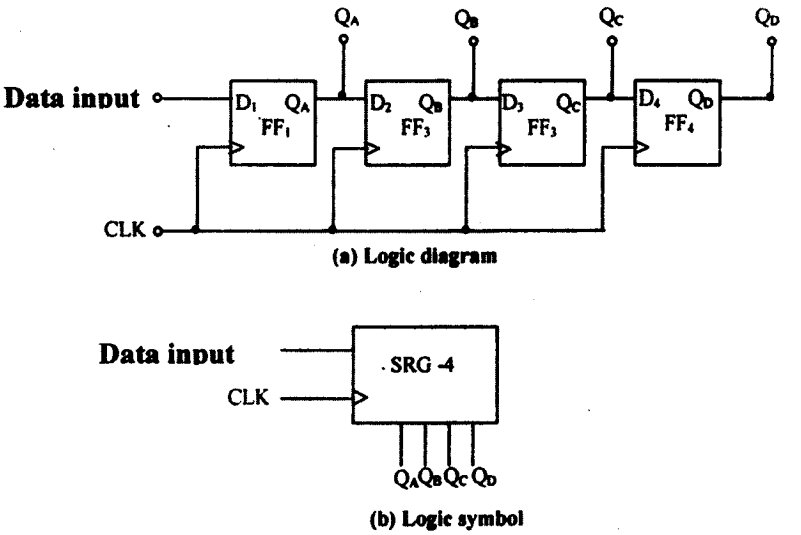


Fig 16.15 A 4 – bit serial - in, parallel - out, shift register.

16.16 Parallel In, Serial – Out Shift Register:

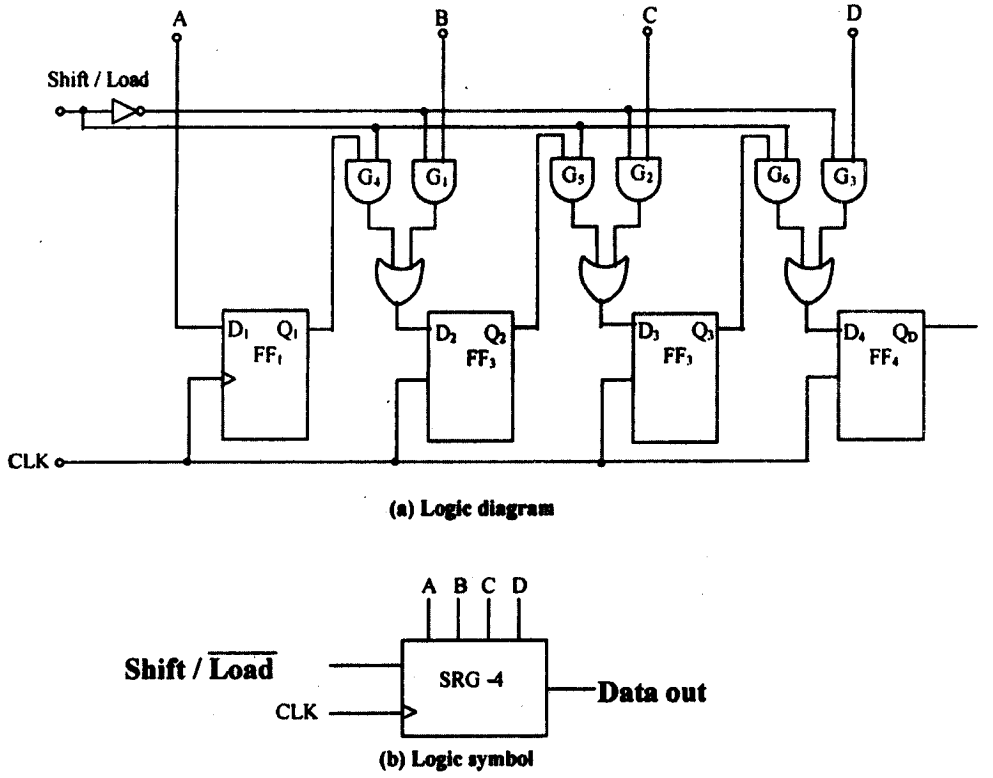


Fig 16.16 A 4-bit parallel - in, serial – out, shift register.

20

In parallel – in, serial-out, shift register, the data bits are entered simultaneously into their respective stages on parallel lines, rather than on a bit-by-bit basis on one line as with serial data inputs, but the data bits are transferred out of the register serially, i.e., on a bit-by-bit basis over a single line.

Fig 16.16 illustrates a 4-bit parallel-in, serial out, shift register using D flip-flops. There are four data lines A, B, C and D through which the data is entered into the register in parallel form. The signal shift / load allows (a) the data to be entered in parallel form into the register and (b) the data to be shifted out serially from terminal Q_4.

When Shift / Load line is high, gates G_1, G_2 and G_3 are disabled, but gates G_4, G_5 and G_6 are enabled allowing the data bits to shift – right from one stage to the next. When Shift / Load line is low, gates G_4, G_5 and G_6 are disabled, whereas gates G_1, G_2 and G_3 are enabled allowing the data input to appear at the D inputs of the respective flip-flops. When a clock pulse is applied, these data bits are shifted to the Q output terminals of the flip-flops and therefore, data is inputted in one step. The OR gate allows either the normal shifting operation or the parallel data entry depending on which AND gates are enabled by the level on the Shift / Load input.

16.12 Parallel In, Parallel – out Shift Register:

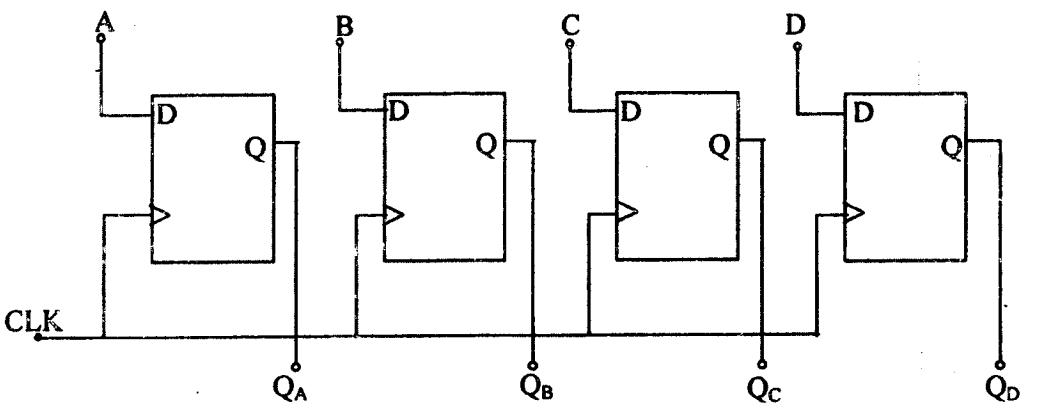


Fig.16.17 Logic diagram of a 4 – bit parallel – in, parallel – out, shift register

In a parallel – in, parallel – out, shift register, the data is entered into the register in parallel form, and also the data is taken out of the register in parallel form. Immediately following the simultaneous entry of all data bits, the bits appear on the parallel outputs.

Fig 16.17 shows a 4-bit parallel-in, parallel-out, shift register using D Flip-Flops. Data is applied to the D input terminals of the flip-flops. When a clock pulse is applied, at the positive going edge of that pulse, the D inputs are shifted in to the Q outputs of the Flip-

Flops. The register now stores the data. The stored data is available instantaneously for shifting out in parallel form.

16.13 Bi-directional Shifter:

A bidirectional shift register is one in which the data bits can be shifted from left to right or from right to left.

Fig 16.18 shows the logic diagram of a 4-bit serial-in, serial-out, bi-directional shift register. Right/Left is the mode signal.

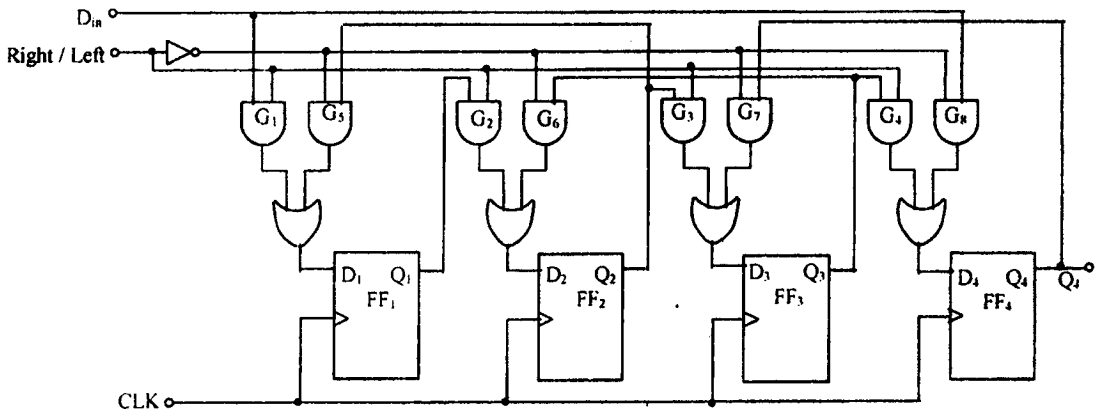


Fig 16.18 Logic diagram of a 4 – bit bi-directional shift register.

When Right / $\overline{\text{Left}}$ is a 1, the logic circuit works as a shift-right shift register. When Right / $\overline{\text{Left}}$ is a 0, it works as a shift – left register. The bidirectional operation is achieved by using the mode signal and two AND gates and one OR gate for each stage as shown in fig 16.18.

A HIGH on the Right / $\overline{\text{Left}}$ control input enables the AND gates G_1, G_2, G_3 and G_4 and disables the AND gates G_5, G_6, $G_7$and G_8 and the state of Q output of each FF is passed through the gate to the D input of the following FF. When a clock pulse occurs, the data bits are then effectively shifted one place to the right. A low on the Right / $\overline{\text{Left}}$ control input enables the AND gates G_5, G_6, $G_7$and G_8 and disables the AND gates G_1, G_2, G_3 and G_4 and the Q output of each Flip-Flop is passed to the D input of the preceding FF. When a clock pulse occurs, the data bits are then effectively shifted one place to the left. Hence, the circuit works as a bidirectional shift register.

16.14 Universal Shift Register:

A universal shift Register is a bidirectional register, whose input can be either in serial form or in parallel form and whose output also can be either in serial form or in parallel form.

Flops. The register now stores the data. The stored data is available instantaneously for shifting out in parallel form.

16.13 Bi-directional Shifter:

A bidirectional shift register is one in which the data bits can be shifted from left to right or from right to left.

Fig 16.18 shows the logic diagram of a 4-bit serial-in, serial-out, bi-directional shift register. Right/Left is the mode signal.

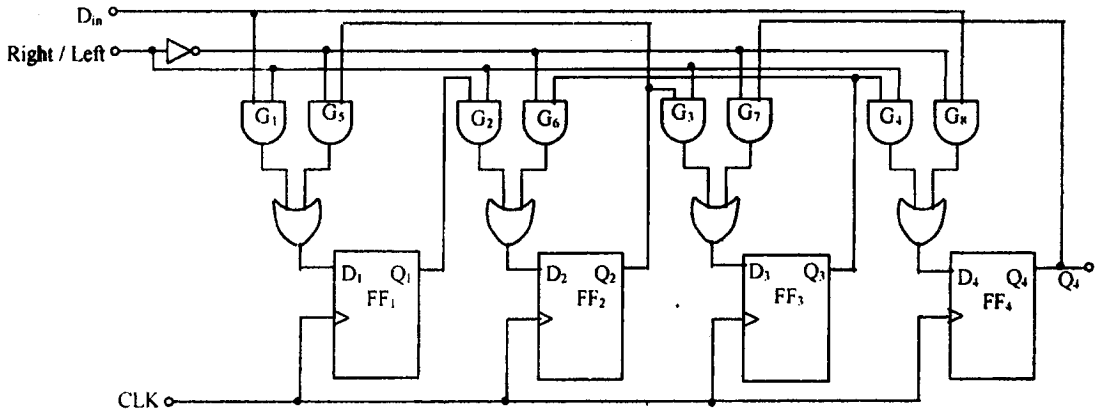


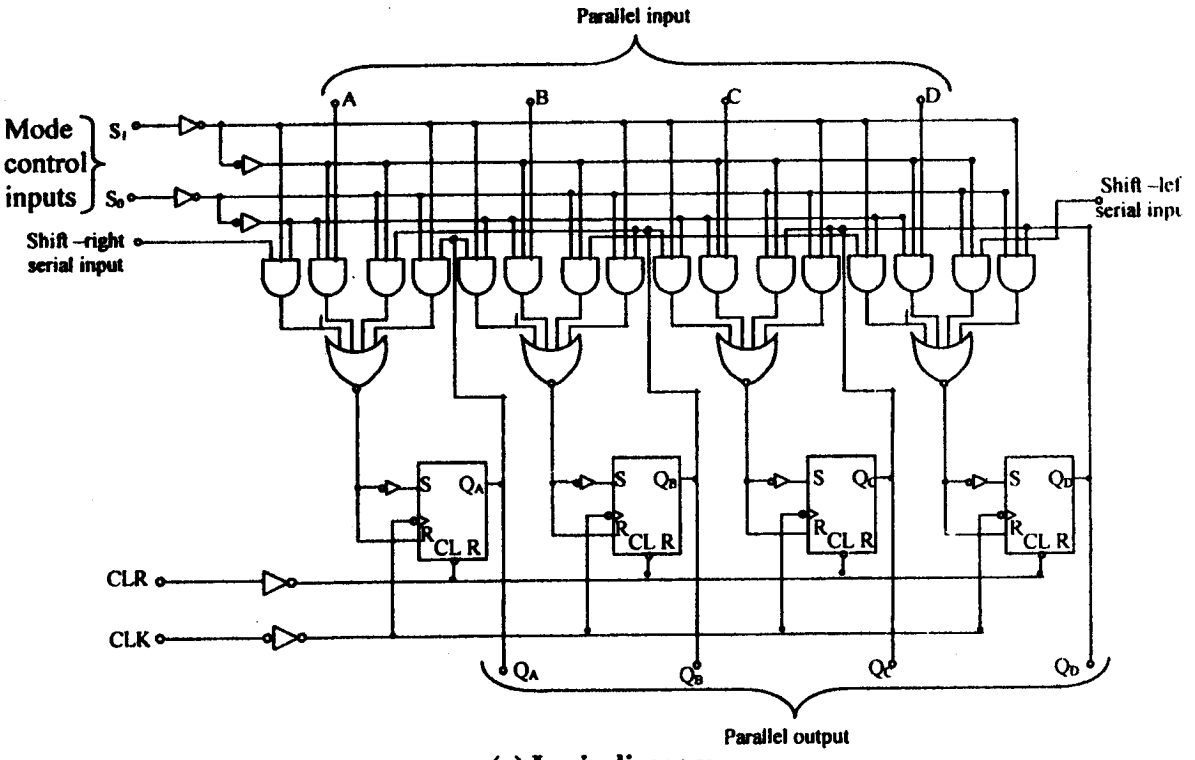
Fig 16.18 Logic diagram of a 4 – bit bi-directional shift register.

When Right / $\overline{\text{Left}}$ is a 1, the logic circuit works as a shift-right shift register. When Right / $\overline{\text{Left}}$ is a 0, it works as a shift – left register. The bidirectional operation is achieved by using the mode signal and two AND gates and one OR gate for each stage as shown in fig 16.18.

A HIGH on the Right / $\overline{\text{Left}}$ control input enables the AND gates G_1, G_2, G_3 and G_4 and disables the AND gates G_5, G_6, $G_7$and G_8 and the state of Q output of each FF is passed through the gate to the D input of the following FF. When a clock pulse occurs, the data bits are then effectively shifted one place to the right. A low on the Right / $\overline{\text{Left}}$ control input enables the AND gates G_5, G_6, $G_7$and G_8 and disables the AND gates G_1, G_2, G_3 and G_4 and the Q output of each Flip-Flop is passed to the D input of the preceding FF. When a clock pulse occurs, the data bits are then effectively shifted one place to the left. Hence, the circuit works as a bidirectional shift register.

16.14 Universal Shift Register:

A universal shift Register is a bidirectional register, whose input can be either in serial form or in parallel form and whose output also can be either in serial form or in parallel form.



(a) Logic diagram

(b)Truth Table

Inputs S_1	Inputs S_0	Clock	Action
0	0	X	No change
0	1	m	Shift-right
1	0	m	Shift-left
1	1	m	Parallel load

Fig 16.19 The 74194 4–bit universal shift register.

Fig 16.19 shows the logic diagrams of the 74194 4-bit universal shift register. The output of each flip-flop is routed through AOI logic to the stage on its right and to the stage on its left. The mode control inputs, S_0 and S_1 are used to enable the left-to-right connections. When it is desired to shift-right, and the right-to-left connections. When it is desired to Shift-Left.

The truth table (fig 16.19b) shows that no shifting occurs when S_0 and S_1 are both LOW or both HIGH. When $S_0 = S_1 = 0$, there is no change in the contents of the register, and when $S_0 = S_1 = 1$, the parallel input data A, B, C and D are loaded into the register on the rising edge of the clock pulse. The combination $S_0 = S_1 = 0$ is said to inhibit the loading of serial or parallel data, since the register contents cannot change

under that condition. The register has an asynchronous active – LOW clear input, which can be used to reset all the flip-flops irrespective of the clock and any serial or parallel inputs.

16.15 COUNTERS

A digital counter is a set of flip-flops (FFs) whose states change in response to pulses applied at the input to the counter. Thus, as its name implies, a counter is used to count pulses. A counter can also be used as a frequency divider to obtain waveforms with frequencies that are specific functions of the clock frequency. They are also used to perform the timing function as in digital watches, to create time delays, to produce non-sequential binary counts, to generate pulse trains, and to act as frequency counters, etc.

Counters may be asynchronous counters or synchronous counters. The term asynchronous refers to events that do not occur at the same time. Asynchronous counters are also called Ripple counters. The asynchronous counter has a disadvantage, in so far as the unwanted spikes are concerned. This limitation is overcome in parallel counters. Propagation delay is a major disadvantage in asynchronous counters because it limits the rate at which the counter can be clocked and creates decoding problem.

The term synchronous as applied to counter operation means that the counter is clocked such that each flip-flop in the counter is triggered at the same time.

16.16 Asynchronous counters:

In a asynchronous counter, the flip-flop output transition serves as a source of triggering other flip-flops. In other words, the CP inputs of all flip-flops are triggered not by the incoming pulses but rather by the transition that that occurs in other flip-flops. In this section, we present some asynchronous counters and explain their operation.

Four – Bit Asynchronous Binary Counter:

Four – Bit asynchronous binary counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the CP input of the next higher-order flip-flop. The flip-flop lading the least significant bit receives the incoming count pulses. The diagram of a 4 – bit binary ripple counter is shown in fig 16.2C. All J and K inputs are equal to '1'. The small circle in the CP input indicates that the flip flop complements during a negative-going transition or when the output to which it is connected goes from 1 to 0.

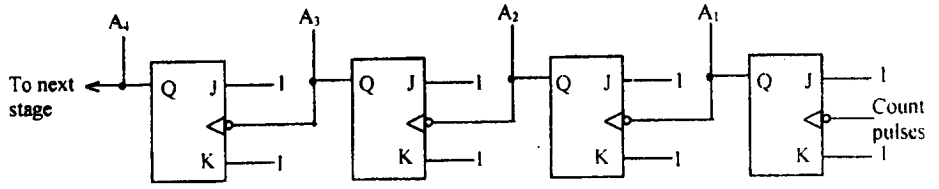


Fig 16.20 4 – bit binary ripple counter

Table 16.2 Count sequence for a binary ripple counter

Count sequence				Conditions for complementing flip-flops	
A_4	A_3	A_2	A_1		
0	0	0	0	Complement A_1	
0	0	0	1	Complement A_1	A_1 will go from 1 to 0 and Complement A_2
0	0	1	0	Complement A_1	
0	0	1	1	Complement A_1	A_1 will go from 1 to 0 and Complement A_2
					A_2 will go from 1 to 0 and Complement A_3
0	1	0	0	Complement A_1	
0	1	0	1	Complement A_1	A_1 will go from 1 to 0 and Complement A_2
0	1	1	0	Complement A_1	
0	1	1	1	Complement A_1	A_1 will go from 1 to 0 and Complement A_2
					A_2 will go from 1 to 0 and Complement A_3
1	0	0	0	and so on ...	A_3 will go from 1 to 0 and Complement A_4

To understand the operation of the binary counter, refer to its count sequence given in Table 16.2. It is obvious that the lowest order bit A_1 must be complemented with each count pulse. Every time A_1 goes from 1 to 0, it complements A_2. Every time A_2 goes from 1 to 0, it complements A_3, and so on. For example, take the transition from count 0101 to 1000. The arrows in the table emphasize the transition in this case. A_1 is complemented with the count pulse. Since A_1 goes from 1 to 0, it triggers A_2 and complements it. As a result, A_2 goes from 1 to 0, which in turn complements A_3. A_3 now goes from 1 to 0, which complements A_4. The output transition of A_4, if connected to a next stage, will not trigger the next flip-flop, since it goes from 0 to 1. The flip-flops change one at a time in rapid succession, and the signal propagates through the counter in a ripple fashion. Hence asynchronous counters are sometimes called asynchronous counters.

The 7493A Four – Bit binary counter:-

The 7493A is presented as an example of a specific integrated circuit asynchronous counter. As the logic diagram in fig 16.21 shows, this device actually consists of a single flip-flop and a three –bit asynchronous counter. This arrangement is for flexibility. It can

be used as a divide – by-2 device using only the single flip-flop, or it can be used as a modulus – 8 counter using only the three-bit counter position. This device also provides gated reset inputs, RO(1) and RO(2). When both of these inputs are HIGH, the counter is RESET to the 0000 state by $\overline{CLR}$.

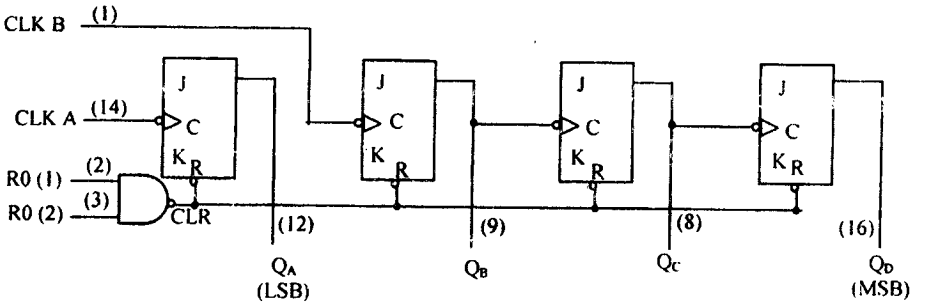
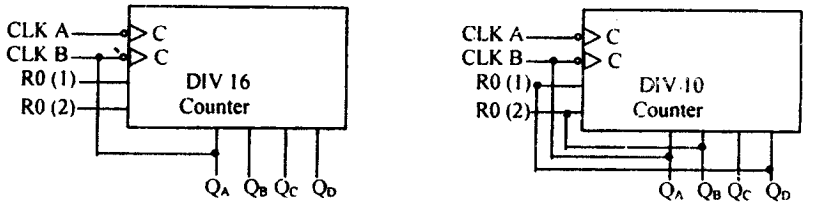


Fig 16.21 The 7493A four-bit binary counter logic diagram. (Pin numbers are in parentheses, and all J-K inputs are internally connected HIGH.

Additionally, the 7493A can be used as a four-bit modules-16 counter (counts 0 through 151) by connecting Q_A output to the CLK B input as shown in fig 16.22.



(a) 7493A connected as a modulus-16 counter

(a) 7493A connected as a decade counter

Fig 16.22 Two configurations of the 7493A asynchronous counter.

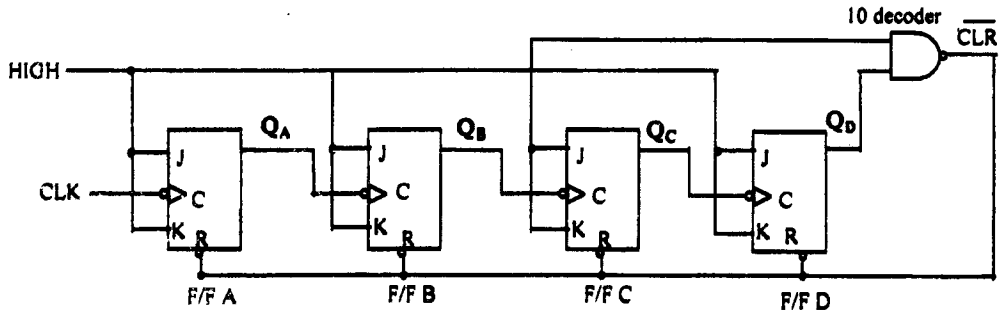
It can also be configured as a decade counter with asynchronous recycling by using the gated reset inputs for partial decoding of count 10_{10}, as shown in fig 16.22(b).

Asynchronous Decade Counters:

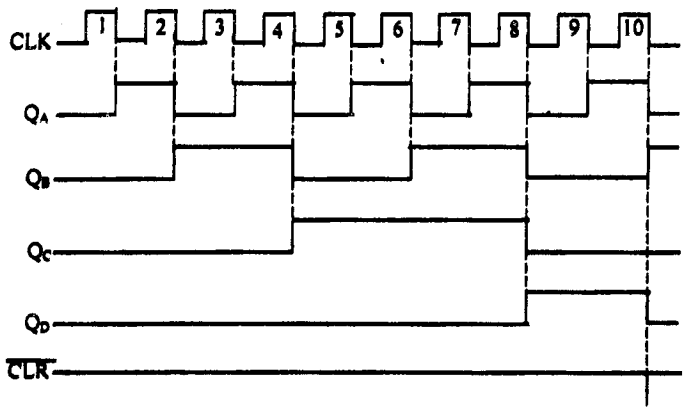
Counters with ten states in their sequence are called decade counter. A decade counter with a count sequence of 0(0000) through 9(1001) is a BCD decade counter because its ten-state sequence is the BCD code. This type of counter is very useful in display applications in which BCD is required for conversion to a decimal readout.

A decade counter requires four flip-flops. We will now take a four-bit asynchronous counter and modify its sequence in order to understand the principle of truncated

counters. One method of achieving this recycling after the count of 9 (1001) is to decode count 10_{10}(1010) with a NAND gate and connect the output of the NAND gate to the clear (CLR) inputs of the flip-flops, as shown in Fig.16.23a.



(a)



(b)

Fig 16.23 An asynchronously clocked decade counter with asynchronous recycling.

Notice that only Q_B and Q_D are connected to the NAND gate inputs. This is an example of partial decoding, in which the two unique states (Q_B = 1and Q_D = 0) are sufficient to decode the count of 10_{10} because none of the other states (0 through 9) have both Q_B and Q_D HIGH at the same time. When the counter goes into count 10_{10}(1010), the decoding gate output goes LOW and asynchronously RESETS all of the flip-flops.

The resulting timing diagram is shown in Fig.16.23 Notice that there is a glitch on the Q_B wave form. The reason for this glitch is that Q_B must first go HIGH before the count of 10_{10} can be decoded. Not until several nano seconds after the counter goes to the count of 10_{10} does the output of the decoding gate go LOW. Thus, the counter is in the 1010 state for a short time before it is RESET back to 0000, thus producing the glitch on Q_B.

16.17 SYNCHRONOUS COUNTERS

Synchronous counters are distinguished from ripple counters in that clock pulses are applied to the CP inputs of all flip-flops. The common pulse triggers all the flip-flops simultaneously, rather than one at a time in succession as in a ripple counter. The decision whether a flip-flop is to be complemented or not is determined from the values of the J and K inputs at the time of the pulse. If J = K = 0, the flip-flop remains unchanged. If J = K = 1, the flip-flop complements. In this section, we present some typical MSI synchronous counters and explain their operation.

Three – Bit Synchronous Binary counter:

Three bit synchronous binary counter is shown in fig 16.24(a) and its timing diagram in fig 16.24(b). An understanding of this counter can be achieved by a careful examination of its sequence of states as shown in Table 16.3.

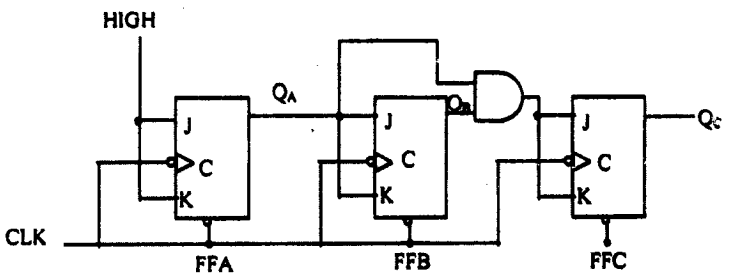


Fig 16.24(a) A three – bit synchronous binary counter.

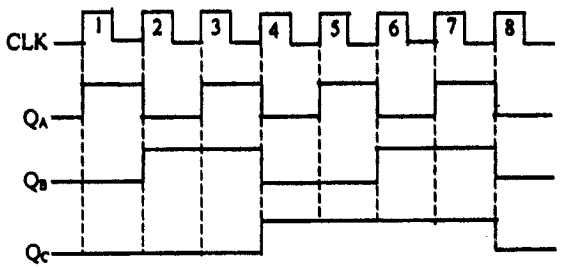


Fig 16.24(b) Timing diagram for the counter of figure.

First , let us look at Q_A. Notice that Q_A changes on each clock pulse as we progress from its original state to its final state and then back to its original state. To produce this operation, FFA must be held in the toggle mode by constant HIGH on its J and K inputs. Now let us see what Q_B does. Notice that it goes to the opposite state following each time Q_A is a 1. This occurs at CLK_2, CLK_4, CLK_6 and CLK_8. CLK_8 causes the counter to recycle. To produce this operation, Q_A is connected to the J and K inputs of FFB. When

Q_A is a 1 and a clock pulse occurs. FFB is the toggle mode and will change state. The other times when Q_A is a 0, FFB is in the no-change mode and remains in its present state.

Table 16.3 State sequence for a three-stage binary counter.

Clock Pulse	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Next, let us see how FFC is made to change at the proper times according to the binary sequence. Notice that both times Q_C changes state, it is preceded by the unique condition of both Q_A and Q_B being HIGH. This condition is detected by the AND gate and applied to the J and K inputs of FFC. Whenever both Q_A and Q_B being HIGH, the output of the AND gate makes the J and K inputs of FFC HIGH, and FFC toggle on the following clock pulse. At all other times, the J and K inputs of FFC are held LOW by the AND gate output, and FFC does not change state.

16.18 SUMMARY

- A flip-flop is the basic memory element; it can store a '0' or a '1'.
- A flip flop is known more formally as a bistable mutivibrator. It has two stable states.
- Flip-Flops are used for data storage, counting, frequency division, parallel-to – serial and serial-to-parallel data conversion, etc.
- An unclocked flip-flop is called a latch, because the output of the flip-flop latches on to a 1 or a 0 immediately after the input is applied.
- The clocked D latch is called a transparent D latch, because its output follows the input when the clock is HIGH.
- The J-K Flip-Flop is the most versatile and most widely used of all the flip-flops.
- T flip-flops are not widely available as commercial items.
- The master-slave flip-flop is made up of two flip-flops- a master and slave. It was developed to make synchronous operation of flip-flops more predictable by overcoming the problem of race in clock flip –flops.

- A register is a set of FFs used to store binary data.
- A register in which shifting of data takes place is called a shift register.
- In a serial - in, serial - out, shift register, data is fed in serially, that is one bit at a time on a single line and data is also shifted out serially.
- In a serial-in, parallel-out, shift register, data is fed in serially but data is shifted out in parallel form, that is all bits at a time.
- In a parallel-in, serial-out, shift register, data is fed in, in parallel form but shifted out in serial form.
- In a parallel – in, parallel – out, shift register, data is both fed in and shifted out in parallel form.
- In a universal shift register, data can be shifted from left – to – right or right –to – left and also data can be shifted in or shifted out in serial form or in parallel form.
- Shift registers are used in digital system to provide time delays. They are also used for serial / parallel data conversion and in construction of ring counters.
- A digital counter is a set of FFS whose states change in response to pulses applied at the input to the counter.
- Counters may be asynchronous counters or synchronous counters.
- Asynchronous counters are also called ripple counters.
- In asynchronous counters, all the FF s do not change states simultaneously. They are serial counters.
- In synchronous counters, all the FF s change state simultaneously. They are parallel counters.
- In asynchronous counters if the clock frequency is very high owing to accumulation of propagation delay, skipping of states may occur.
- In synchronous counters, the propagation delays of individuals FF s do not add together.
- Synchronous counters have the advantages of high speed and less severe decoding problems, but the disadvantage of more circuitry than that of asynchronous counters.
- Generation of pulse trains using indirect logic has the advantage that any counter (ripple or synchronous) with the correct number of states can form the generator.

16.19 KEY TERMINOLOGY

Flip – Flop: A memory device capable of storing a logic level.

D flip-flop: A type of bit table , multi vibrator in which the output follows the state of the D Input.

Register: A group of flip –flops capable of storing data.

Shift Register: A digital circuit capable of storing and shifting binary data.

Universal shift register: Shift – right, shift – left, shift register which can input and output data either serially or parallely.

Counter: A digital circuit capable of counting electronic events, such as pulses, by processing through a sequence of binary states.

Asynchronous counter: A type of counter in which the external clock signal is applied only to the first FF and the output of each FF serves as the clock input to the next FF in the chain.

Synchronous counter: A counter in which the circuit out puts can change state only on the transitions of a clock.

Binary counter: A counter in which the states of FF s represent the binary number equivalent to the number of pulses that have occurred at the input of the counter.

Ripple counter: A counter in which the external clock signal is applied to the first FF and then the clock input to every other FF is the output of the preceding FF.

16.20 SELF – ASSESSMENT QUESTIONS

1. Distinguish between combinational and sequential switching circuits
2. How do you build a latch using universal gates?
3. Explain the operation of clocked SR flip-flop.
4. List the different types of latches and flip-flops. Name the applications of each type.
5. How does a J-K flip –flop differ from an S-R flip-flop in its basic operation? What is its advantage over an S-R flip – flop?
6. What do you mean by toggling?
7. What is a serial-in, serial-out, shift register? Explain the operation of it.
8. What is a parallel-in, serial-out, shift register? Explain the operation of circuit.
9. What is a serial – in, parallel-out, shift register? Explain the operation of the circuit.
10. What is a parallel – in, Parallel – out, shift register? Explain the operation of the circuit.
11. What is a universal shift register? Explain the operation of the circuit.

12. What is the basic difference between a counter and a shift register?
13. What is the advantage of a synchronous counter over asynchronous counter? What is its disadvantage?
14. Explain the operation of 4-bit Asynchronous Binary counter.
15. Explain the operation of Decade counter.
16. What is synchronous counter? Explain the operation of 3-bit synchronous binary counters.
17. Explain the operation of synchronous decade counter.

16.21 TEXT AND REFERENCE BOOKS

1 Digital Logic and Computer Design – M. Morris Mano, Prentice Hall Inc,.

2 Digital Fundamentals – 3rd Edition – Floyd, UBS Publishers.

3 Digital Electronics: An Introduction to Theory and Practice, 2nd edn., Prentice – Hall of India, New Delhi, 1987.

4 Switching and Finite Automatic Theory, 2nd edn., Tata -McGraw – Hill, New Delhi, 1978.

5 Tokheim, T., Digital Principles, Tata -McGraw – Hill, New Delhi, 1988.